International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 02, February-2015

Low Power Memory Architecture Design Techniques

Suganya. S
Electronics and Communication Engineering
Mahendra Engineering college(Autonomous), mahendrapuri
Namakkal(Dt), Tamilnadu, India.

***Abstract*: In this work, Reduction of power consumption has become important parameter in the field of Integrated Circuits. Managing the clock logically when applied to the flip flop is proposed in this clock. Clock given individually to the each and every flip flop is managed by clock gating, clock tree minimization and voltage supply devices. In this work D-type flip flops are considered based on the following factors. One is Concentrating Flip Flops previous and present stages. Second is Assigning a common clock to a group of Flip Flops. The logical model of above methods are implemented and compared with pulsed Flip Flop with respect to the clock tree. Finally power consumed is compared and less utilization of power will be considered as best approach.**

***Index Terms* : Clock tree migration, pulse generator, pulsed latch, modelsim, Altera Quartus II.**

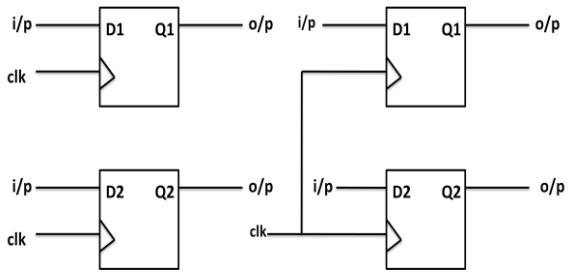
I.INTRODUCTION

Power consumption has become a crucial issue in high-performance circuits because the number of transistors has increased substantially. Several techniques are proposed to reduce total power of a chip, such as multiple supply voltages, clock gating, and clock-tree minimization. Because of heavy pipeline designs and high-frequency signal switching, a clock tree is known to be a major contributor to power dissipation. The clock tree accounts for a significant portion of total power consumption and consumes of total power. Therefore, the chip power can be greatly reduced by decreasing the clock-tree power.

The power dissipation of a clock pulse can be reduced by reducing the total clock pulses. However, existing methods of clock-tree minimization are primarily based on both pulsed latch and flip-flops. In current circuit designs, the most common storage element is a D-type flip-flop that consists of two latches (master and slave) triggered by a clock signal. This type of design makes it easier to apply static timing analysis (STA) for timing verification. As transistor counts of a flip-flop are two times than that of a single latch, latches are superior to flip-flops in terms of area, transition time, and power dissipation. However, it is difficult to perform STA on latch-based circuits because of data transparency.

II.PULSED LATCH UTILIZATION FOR CLOCK TREE

In this method uses flip flop and latch alone to reduce the power and increase the speed of memory. This method uses the algorithm clock tree minimization and network flow. This is handled by two methods. In first method two different types are used such as two different flip flop with different clock pulses, two different flip flop with same clock pulses. In these two types the clock pulses consumes large amount of power. In below fig.(a) shows separate clock pulse is given to each flip flops. And the given input also in separate manner. The fig.(b) shows same clock pulse is given as input for different flip flops. For this process I use D-type Flip Flop. The input is given to data1 and output has been taken from the port Q1. The same will be carried for all flip flops and the data value increased as consecutive numbers. i.e., It will appear for n number of flip flops. It consumes large amount of power.



(a) **(b)**

Fig:1.1 (a) Two different Flip Flops with different clocks. (b) Two different Flip Flops with same clocks.

III. CLOCK TREE MINIMIZATION TECHNIQUE

So I move on to the method Clock Tree Minimization to reduce the power consumption as in smaller and also memory is in faster manner.

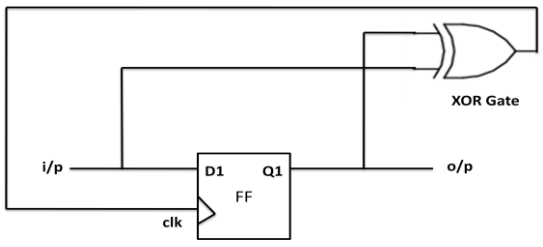


Fig:1.2 Clock Tree Minimization Technique

In Clock Tree Minimization Technique, consider flip flop and a XOR Gate. The output of the flip flop given as input for the XOR gate. The input as D1 and clock pulse is given to flip flop. After processing the input the FF produce output as Q1. This will given as one of the input for Xor gate and another input will be taken from the one of the input of FF. Here two type of state will be occurred. That are, If input and output are same xor gate gives zero. So clock is zero. When clock is zero 'No Change' state occur in the Flip Flop.

If input and output are different xor gate gives one as output. So the clock is +ve(one). When clock is +ve and gives change of input and output. If input and output are same Xor gate gives zero. So clock is zero. When clock is zero 'No Change' state occur in the Flip Flop. If input and output are different Xor gate gives one as output. So the clock is +ve(one). When clock is +ve and gives change of input and output.

The main purpose of Clock Tree Minimization technique which enable the gate whenever the Changes occurred in the input and output. In these cases we reduce the consuming power as compared to existing method. From these reason which is used wherever we require faster memory with less power this method is useful.

IV. SIMULATION

For two methods in existing system the barrel shifter is used. In that Behavior level program is used. For barrel shifter the two input port are w and s. port w takes the input as w downto 0 and port s takes 1 downto 0. Both w and s are unsigned bits. Consider w will be 1000 and s will be 00, 01, 10, and11. The value of w will be depends on the value of s. That is, when s value is given, the position of the w will move one from right to left. And this will provide no change when s as 00.

The barrel shifter act as a intermediating device for two logic. This barrel shifter programmed into the testdum as the entity name. In all simulation type the entity name will be our choice shown in fig:1.1(a). The following will be the output of above input. Here I use modelsim 6.5e for simulation process. The output for the part of first method is given below.

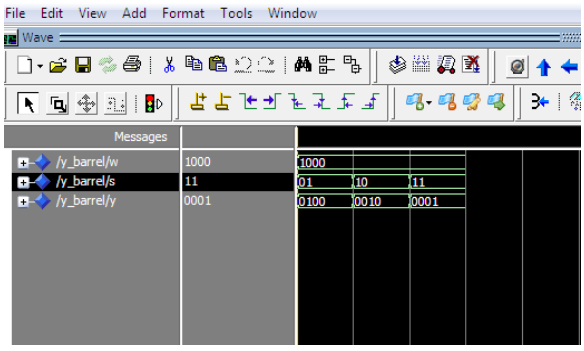


Fig:1.3 Output of Two different flip flops with different clock pulses

The second method of existing system is two different flip flop with same clock pulses shown in fig:1.1(b). In this way somewhat type we minimize the power, But the memory not work as a faster manner. Because, the clock enable for all the signals. In this type the input gives as a tree manner. If give 00 means it process and produce 0001. Likewise for 01the output will be 0011, for 10 the output will be 0111 and for 11 the output is 1111. It process with the input of barrel shifter. When it from right to left, the value in the positions are interchanged and when it moves from left to right the values in the last position carried to each s value of the barrel shifter. The output of above detail is shown as below.

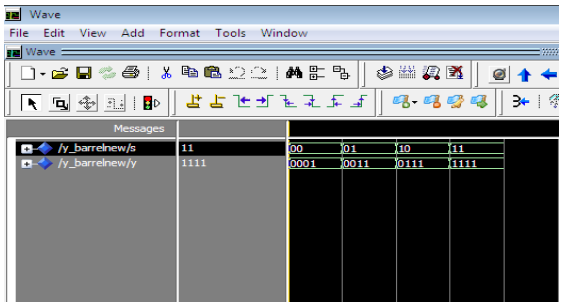


Fig:1.4 Output of Two different flip flops with same clock pulses

The proposed system use flip flop alone. Generally flip flop is clock sensitive. In Clock Tree Minimization technique Xor gate and flip flop and clock are used as required. First input and clock pulse is given to flip flop and which provide Q1 as a output. The input is given as one of the input for xor gate. Another input is taken from the output of flip flop. The output of xor gate again given to the input of flip flop as clock portion. If the changes occurred in the clock pulse means no change in the output. But if the changes happened in the output of xor gate means the output of FF also changes. i.e., the clock pulse will enable whenever the two inputs of the xor gate is different. So whenever the input changes occur at the time only the power be consumed. This will helpful to reduce the power consumption while same clock pulses used for previous and working time of FF. The output of clock tree minimization technique will shown below.

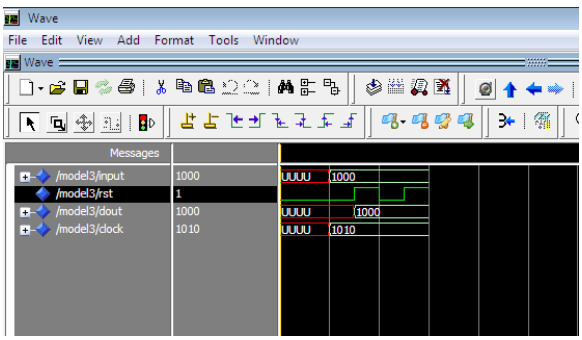


Fig:1.5 Output of Clock Tree Minimization Technique

V. SYNTHESIS

For synthesis I use Altera Quartus II with the family name is Cyclone II and which is device EP2C20F484C7. After simulating the program in this family, processing is carrying. The synthesis is followed for above all methods. This will provide output of the previous and my work such as Timing part and power consumption part. These are shown as below.

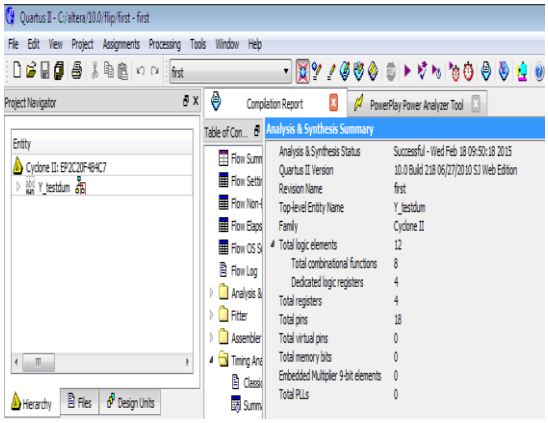


Fig:1.6 Total logic function and total pins for two different FF with different clock pulses

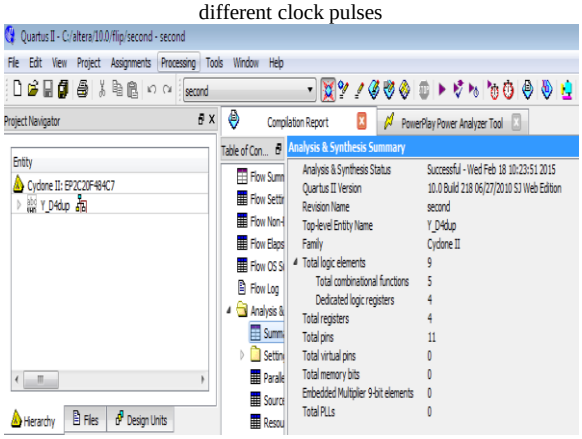


Fig:1.7 Total logic function and total pins for two different FF with same clock pulses

The above diagram is the output of the total logic function and total pins in the methods.

Timing Analyzer Summary

Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
Worst-case tsu	N/A	None	5.859 ns	dkcom	dk3	--	E[1]	0
Worst-case tco	N/A	None	8.687 ns	q4	dataout4	E[0]	--	0
Worst-case th	N/A	None	-2.580 ns	datain4	q4	--	E[0]	0
Total n...d paths								0

Fig:1.8 Timing Analysis for for two different flip flops with same clock pulses

The timing analysis of the two flip flops are shown as above.

PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Wed Feb 18 10:24:26 2015
Quartus II Version	10.0 Build 218 06/27/2010 SJ Web Edition
Revision Name	second
Top-level Entity Name	Y_D4dup
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	67.94 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	20.59 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig:1.9 Power play power analyzer for two different flip flops with same clock pulses

PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Wed Feb 18 10:39:03 2015
Quartus II Version	10.0 Build 218 06/27/2010 SJ Web Edition
Revision Name	third
Top-level Entity Name	model3
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	67.71 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	20.36 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig: 1.10 Power Play power analyzer for Clock Tree Minimization

Form the power play power analyzer of two different FF with different clock pulses and the clock tree minimization are reduced as interms of power and memory.

VI. RESULT

From the analysis of simulation and synthesis method it produce power in the unit in mW. The obtained power will be the output of four flip flops taken as a input. If increase the number flip flops means the obtain power also reduced as much manner. The power for Clock Tree Minimization is 0.23mW. And also it will produce memory as in the faster manner.

VII.REFERENCES

[1] Hong-Ting Lin, Yi-Lin Chuang, Zong-Han Yang, and Tsung-Yi Ho, Senior Member, IEEE" Pulsed-Latch Utilization for Clock-Tree Power Optimization" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 4, APRIL 2014.

[2] Q. Wu, M. Pedram, and X. Wu, "Clock-gating and its application to low power design of sequential circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 47, no. 3, pp. 415–420, Mar. 2000.

[3] J. Oh and M. Pedram, "Gated clock routing for low-power microprocessor design," IEEE Trans. Comput. Aided Design, vol. 20, no. 6, pp. 715–722, Jun. 2001.

[4] R. S. Shelar, "An efficient clustering algorithm for low power clock tree synthesis," in Proc. Int. Symp. Phys. Design, Mar. 2007, pp. 181–188.

[5] Y. L. Chuang, S. Kim, Y. Shin, and Y. W. Chang, "Pulsed-latch-aware placement for timing-integrity optimization," in Proc. 47th ACM/IEEE Design Autom. Conf., Jun. 2010, pp. 280–285.

[6] S. Kim, I. Han, S. Paik, and Y. Shin, "Pulser gating: A clock gating of pulsed-latch Circuits," in Proc. Asia South Pacific Design Autom. Conf., 2011, pp. 190–195.