

LOW POWER, LOW-TRANSITION RANDOM PATTERN GENERATOR

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Abstract

In this project test patterns generated by the Low-transition random pattern generator (LT-RTPG) detect Easy-to-detect faults. This LT-RTPG's are normally used in Built In Self Tests (BIST). This project also presents a novel low-transition linear feedback shift register (LFSR) that is based on some new observations about the Output sequence of a conventional LFSR. The proposed design, called Bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2×1 Multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain Input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. The proposed LT-RTPG can significantly reduce switching activity during BIST. These techniques have a substantial effect on average- and peak-power reductions with negligible effect on fault coverage or test application time. Experimental results on ISCAS'89 benchmark circuits show up to 65% and 55% reductions in average and peak power, respectively.

Index Terms — Built-in self-test (BIST), linear feedback shift register (LFSR), low-power test, pseudorandom pattern generator

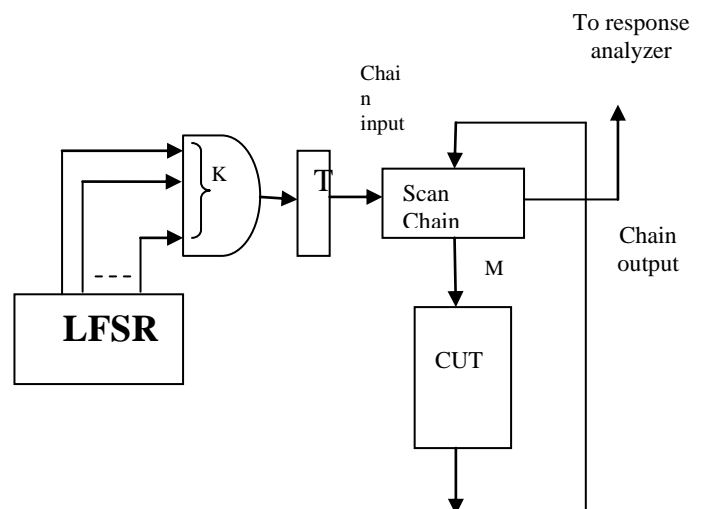
1. Introduction

The LT-RTPG reduces switching activity during BIST by reducing transitions at scan inputs during scan shift operations. An example LT-RTPG is shown in Fig. The LT-RTPG is comprised of an r-stage LFSR, a K-input AND gate, and a toggle flip-flop (T flip-flop). Hence, it can be implemented with very little hardware. Each of K inputs of the AND gate is connected to either a normal or an inverting output of the LFSR stages. If large K is used, large sets of neighbouring state inputs will be assigned identical values in most test patterns, resulting in the decrease fault coverage or the increase in test sequence length. In this project, LT-RTPGs with only K=2 or 3 are used since a T- flip-flop holds previous values until the input of the T flip-flop is assigned a 1, the same value v, where $v \in \{0,1\}$, is repeatedly scanned into the scan chain until the value at the output of the AND gate. Hence, adjacent scan flip-

flops are assigned identical values in most test patterns and scan inputs have fewer transitions during scan shift operations. Since most switching activity during scan BIST occurs during scan shift operations. The LT-RTPG can reduce heat dissipation during overall scan testing. This paper presents a new TPG, called the bit-swapping linear feedback shift register (BS-LFSR), that is based on a simple bit swapping technique applied to the output sequence of a conventional LFSR and designed using a conventional LFSR and a 2×1 multiplexer. The proposed BS-LFSR reduces the average and instantaneous weighted switching activity (WSA) during test operation by reducing the number of transitions in the scan input of the CUT.

2. Existing system:

This system consists of LFSR, AND gate, T flip-flop and circuit under test. In our project we are replacing LFSR with Bit-Swapping LFSR (BS-LFSR) so that we can reduce power consumption up to 55-65%.



3. Proposed approach to Design the LT-RTPG:

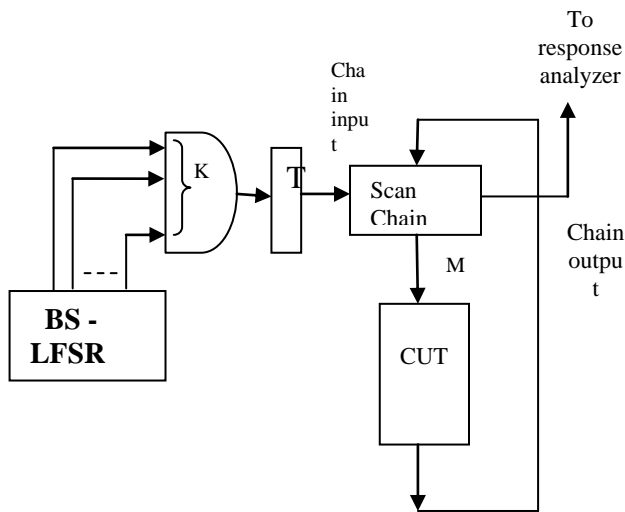


Fig: PROPOSED LT-RTPG

It has been observed that many faults that escape random patterns are highly correlated with each other and can be detected by continuously complementing values of a few inputs from a parent test vector. These observations are exploited and improve fault coverage for circuits that have large numbers of RPRFs. We have also observed that tests for faults that escape LT-RTPG test sequences share many common input assignments. This implies that RPRFs that escape LT-RTPG test sequences can be effectively detected by fixing selected inputs to binary values specified in deterministic test cubes for these RPRFs and applying random patterns to the rest of inputs. This technique is used in the 3-weight WRBIST to achieve high fault coverage for random pattern resistant circuits. The proposed LT-RTPG is as follows.

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Bit-swapping LFSR:

In recent years, the design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power consumption of new VLSI systems. However, most of these methods focus on the power consumption during normal mode operation, while test mode operation has not normally been a predominant concern. However, it has been found that the power consumed during test mode operation is often much higher than during normal mode operation. This is because most of the consumed power results from the switching activity in the nodes of the circuit under test (CUT), which is much higher during test mode than during normal mode operation.

Several techniques that have been developed to reduce the peak and average power dissipated during scan-based tests. A direct technique to reduce power consumption is by running the test at a slower frequency than that in normal mode. This technique of reducing power consumption, while easy to implement, significantly increases the test application time. Furthermore, it fails in reducing peak-power consumption since it is independent of clock frequency.

Another category of techniques used to reduce the power consumption in scan-based built-in self-tests (BISTs) is by using scan chain-ordering techniques. These techniques aim to reduce the average-power consumption when scanning in test vectors and scanning out captured responses. Although these algorithms aim to reduce average-power consumption, they can reduce the peak power that may occur in the CUT during the scanning cycles, but not the capture power that may result during the test cycle (i.e., between launch and capture). The design of low-transition test-pattern generators (TPGs) is one of the most common and efficient techniques for low-power tests. This project presents a new TPG, called the bit-swapping linear feedback shift register (BS-LFSR), that is based on a simple bit swapping technique applied to the output sequence of a conventional LFSR and designed using a conventional LFSR and a 2×1 multiplexer.

The introduced BS-LFSR reduces the average and instantaneous weighted switching activity (WSA) during test operation by reducing the number of transitions in the scan input of the CUT.

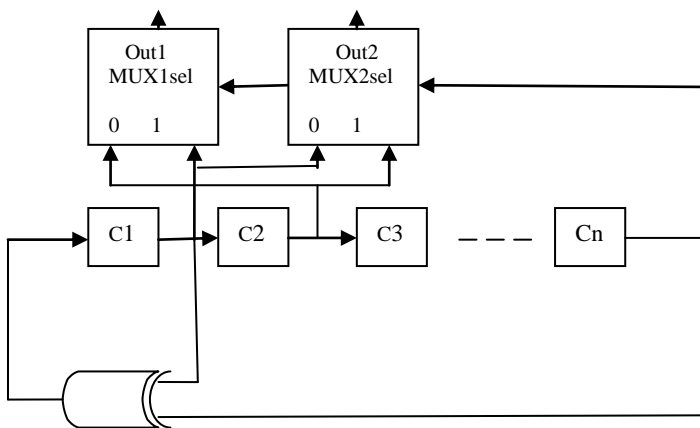


Fig (A): BIT-SWAPPING LFSR

The introduced BS-LFSR for test-per-scan BISTs is based upon some new observations concerning the number of transitions produced at the output of an LFSR.

Definition: Two cells in an n -bit LFSR are considered to be adjacent if the output of one cell feeds the input of the second directly (i.e., without an intervening XOR gate).

Approach: Each cell in a maximal-length n -stage LFSR will produce a number of transitions equal to $2n-1$ after going through a sequence of $2n$ clock cycles.

Proof: The sequence of 1s and 0s that is followed by one bit position of a maximal-length LFSR is commonly referred to as an m -sequence. Each bit within the LFSR will follow the same m -sequence with a one-time-step delay. The m -sequence generated by an LFSR of length n has a periodicity of $2^n - 1$. It is a well-known standard property of an m -sequence of length n that the total number of runs of consecutive occurrences of the same binary digit. The beginning of each run is marked by a transition between 0 and 1; therefore, the total number of transitions for each stage of the LFSR is $2^n - 1$. This approach can be proved by using the toggle property of the XOR gates used in the feedback of the LFSR.

IMPORTANT PROPERTIES OF THE BS-LFSR:

There are some important features of the BS-LFSR that make it equivalent to a conventional LFSR. The most important properties of the BS-LFSR are the following.

1) The BS-LFSR generates the same number of 1s and 0s at the output of multiplexers after swapping of two adjacent cells; hence, the probabilities of having a 0 or 1 at a certain cell of the scan chain before applying the test vectors are equal. Hence,

the proposed design retains an important feature of any random TPG. Furthermore, the output of the multiplexer depends on three different cells of the LFSR, each of which contains a pseudorandom value. Hence, the expected value at the output can also be considered to be a pseudorandom value.

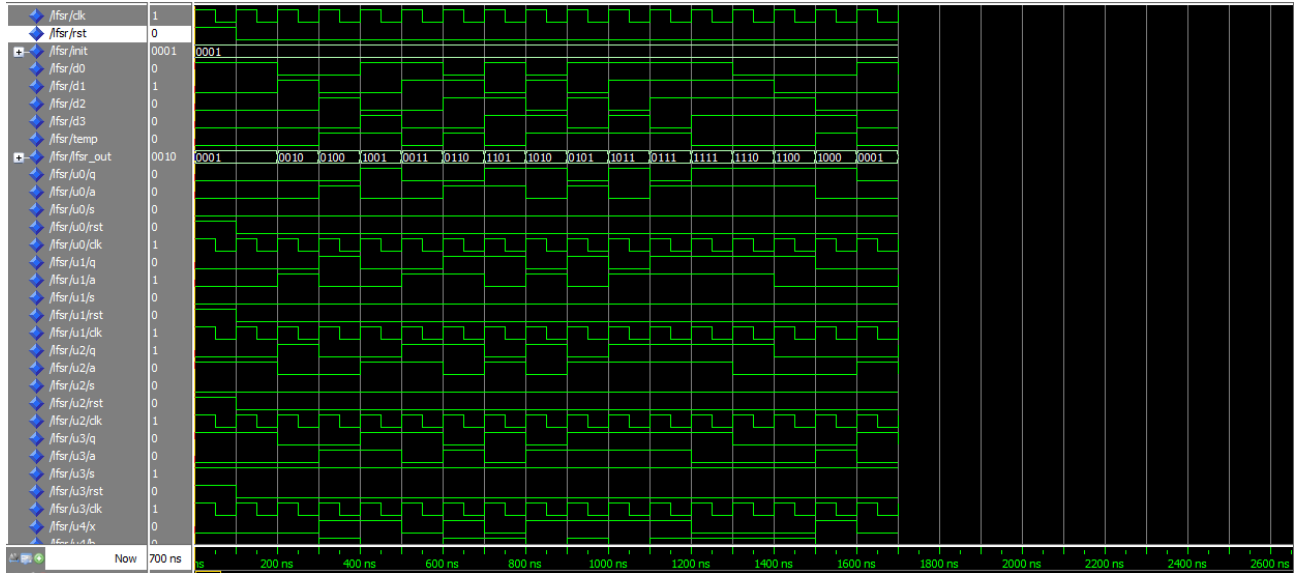
2) If the BS-LFSR is used to generate test patterns for either test per- clock BIST or for the primary inputs of a scan-based sequential circuit (assuming that they are directly accessible) as shown in Fig. 3, then consider the case that $c1$ will be swapped with $c2$ and $c3$ with $c4, \dots, cn-2$ with $cn-1$ according to the value of cn which is connected to the selection line of the multiplexers (see Fig. A). In this case, we have the same exhaustive set of test vectors as would be generated by the conventional LFSR, but their order will be different and the overall transitions in the primary inputs of the CUT will be reduced by 25%. The different transition values of LFSR and BS-LFSR are shown in below table I.

LFSR output					BS - LFSR output				
1	0	1	0	(10)	0	1	1	0	(6)
0	1	0	1	(5)	0	1	0	1	(5)
1	0	1	1	(11)	1	0	1	1	(11)
0	1	1	1	(7)	0	1	1	1	(7)
1	1	1	1	(15)	1	1	1	1	(15)
1	1	1	0	(14)	1	1	1	0	(14)
1	1	0	0	(12)	1	1	0	0	(12)
1	0	0	0	(8)	0	1	0	0	(4)
0	0	0	1	(1)	0	0	0	1	(1)
0	0	1	0	(2)	0	0	1	0	(2)
0	1	0	0	(4)	1	0	0	0	(8)
1	0	0	1	(9)	1	0	0	1	(9)
0	0	1	1	(3)	0	0	1	1	(3)
0	1	1	0	(6)	1	0	1	0	(10)
1	1	0	1	(13)	1	1	0	1	(13)
1	0	1	0	(10)	0	1	1	0	(6)
8	(8)	8	8	No of transitions	8	(4)	8	8	

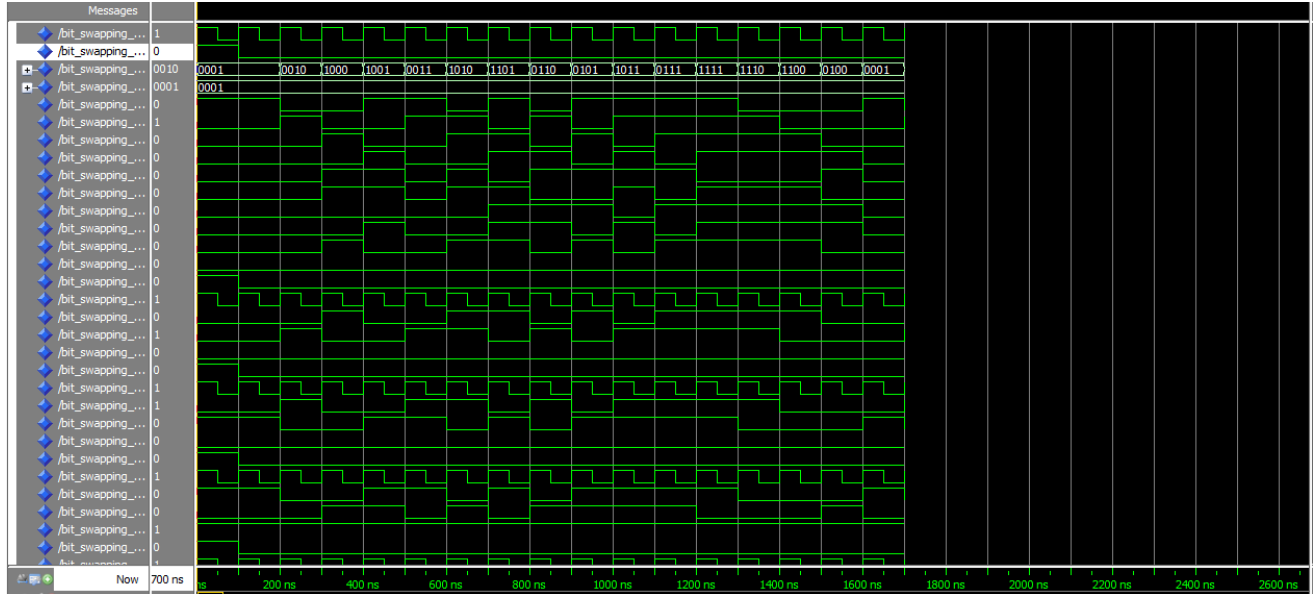
TABLE I
COMPARISON BETWEEN LFSR &BS-LFSR:

4. Experimental results and comparison:

SIMULATION RESULTS OF LFSR:



SIMULATION RESULTS OF BS-LFSR:



COMPARISON BETWEEN POWER CONSUMPTION OF LFSR AND BS-LFSR:

Xilinx XPower Analyzer - lfsr.ncd - [Table View]

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Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.102	1	---	---
Logic	0.000	9	33280	0.0
Signals	0.000	19	---	---
IOs	0.000	15	309	4.9
Total Quiescent Power	0.180			
Total Dynamic Power	0.222			
Total Power	0.402			

Views Table View

Xilinx XPower Analyzer - Bit_swapping_lfsr.ncd - [Table View]

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Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.079	1	---	---
Logic	0.000	3	33280	0.0
Signals	0.000	8	---	---
IOs	0.000	6	309	1.9
Total Quiescent ...	0.179			
Total Dynamic P...	0.199			
Total Power	0.378			

Views Table View

5. Conclusion:

A low-transition TPG that is based on some observations about transition counts at the output sequence of LFSRs has been presented. The proposed TPG is used to generate test vectors for test-per scan BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. The effect of the proposed design in the fault coverage, test-application time, and hardware area overhead is negligible. Comparisons between the proposed design and other previously published methods show that the proposed design can achieve better results for most tested benchmark circuits.

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REFERENCES:

- [1] P. H. Bard ell, W. H. McAnney, and J. Savir, *Built-In Test for VLSI: Pseudorandom Techniques*. New York: Wiley, 1987.
- [2] S. Hellebrand, J. Rajski, S. Tarnick, S. Venkataraman, and B. Courtois, "Built-In test for circuits with scan based on reseeding of multiple polynomial linear feedback shift registers," *IEEE Trans. Compute.*, vol. 44, no. 2, pp. 223–233, Feb. 1995.
- [3] N. Zachariah, J. Rajski, and J. Tyszer, "Decompression of test data using variable-length seed LFSRs," in *Proc. IEEE 13th VLSI Test Symp.*, 1995, pp. 426–433.
- [4] S. Hellebrand, S. Tarnick, and J. Rajski, "Generation of vector patterns through reseeding of multiple-polynomial linear feedback shift registers," in *Proc. IEEE Int. Test Conf.*, 1992.
- [5] P. Hortensius, R. McLeod, W. Pries, M. Miller, and H. Card, "Cellular automata-based pseudorandom generators for built-in self test," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 8, no. 8, pp. 842–859, Aug. 1989.
- [6] A. Stroele, "A self test approach is using accumulators as test pattern generators," in *Proc. Int. Symp. Circuits Syst.*, 1995, pp. 2120–2123.

- [7] H. J. Wunderlich, "Multiple distributions for biased random test patterns," in *Proc. IEEE Int. Test Conf.*, 1988, pp. 236–244.
- [8] I. Pomeranz and S. M. Reddy, "3 weight pseudo-random test generation based on a deterministic test set for combinational and sequential circuits," *IEEETrans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 12, no. 7, pp. 1050–1058, Jul. 1993.
- [8] Y. Zorian, "A distributed BIST control scheme for complex VLSI devices," in *Proc. 11th IEEE VTS*, Apr. 1993, pp. 4–9.
- [9] A. Hertwig and H. J. Wunderlich, "Low power serial built-in self-test," in *Proc. IEEE Eur. Test Workshop*, May 1998, pp. 49–53.
- [10] P. Girard, "Survey of low-power testing of VLSI circuits," *IEEE Des. Test Comput.* vol. 19, no. 3, pp. 80–90, May/Jun. 2002.
- [11] K. M. Butler, J. Saxena, T. Fryars, G. Hetherington, A. Jain, and J. Lewis, "Minimizing power consumption in scan testing: Pattern generation and DFT techniques," in *Proc. Int. Test Conf.*, 2004, pp. 355–364.
- [12] J. Saxena, K. Butler, and L. Whetsel, "An analysis of power reduction techniques in scan testing," in *Proc. Int. Test Conf.*, 2001, pp. 670–677.