Low power Design and Analysis of Low Noise Amplifiers for RF receiver front end using 90nm CMOS

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Abstract

This letter presents the design of low-noise amplifiers for wireless receiver front ends. Several low noise amplifier topologies are implemented namely: (1) cascaded common-source amplifier, (2) folded cascode amplifier, (3) shunt feedback amplifier and (4) Current-Reuse $g_m$ boosted CG LNA. The amplifiers were implemented in a standard 90-nm CMOS process and were operated with a 1-V supply voltage. Low-noise amplifier measurements were taken for parameters such as power gain, noise figure, input matching, output matching, reverse isolation, stability, and linearity. Based on the employed figure-of-merit, the cascaded common-source low-noise amplifier achieved the best performance among the four with a simulated gain of 13.8 dB and noise figure of 1.7 dB, which makes it comparable to previously available works.

Keywords - CMOS Process; Low-noise amplifier; Figure of Merit.

I. Introduction

The overwhelming technological advances in CMOS scaling and RF CMOS circuit design techniques in the past few years have made it possible to integrate all the elements of a transceiver on a single chip. Now a days most of the systems uses battery operated devices. So it must consume very low power. Low power, less expensive CMOS technologies have been used successfully to implement all the necessary RF functionality for existing and emerging wireless area network standards, such as Bluetooth Wi-Fi and WiMAX [1]. A CMOS system-on-chip (SOC) solution to enable a single-chip cell phone, with the analog and digital basebands, power management, and the RF transceiver are fully integrated on a single monolithic CMOS IC, has been reported [2].

WiMAX is a wireless communication standard which stands for Worldwide Interoperability for Microwave Access. It belongs to the IEEE 802.16 family of standards, which provides wireless broadband access. It provides data rates of up to 100 Mbps (in a 20 MHz channel using 64QAM ¾ code rate) [3]. It has a very large coverage area of around 10 km from a WiMAX base station for point-to-multipoint, non-line-of-sight (see following pages for illustrations and definitions) service. There are two types of WiMAX systems: Fixed WiMAX and Mobile WiMAX. The fixed WiMAX system doesn’t allow handoff mechanism between base stations whereas Mobile WiMAX provides both mobile and fixed services [4].

The rest of the letter organized as follows: Section 2 of this letter describes the topologies of the implemented low noise amplifiers. Section 3 presents the circuit design. The simulation results are presented in section 4 followed by the conclusion in section 5.

II. Low Noise Amplifiers

The low-noise amplifier (LNA) is the first block in the receiver chain of a communications system, connected directly to the antenna. Its noise figure (NF) performance has the most impact to the overall receiver system. Its job is to amplify the weak signals coming from the antenna while adding as little noise as possible. NF is a crucial design specification which trades off with additional design parameters like third order input intercept point (IIP3), second order input intercept point (IIP2), power consumption and gain.

a. Cascoded Common Source Low Noise Amplifier

The most frequently used architecture for LNA design today is the cascaded amplifier with inductive source degeneration shown in the Fig 1.A cascode stage was employed to improve isolation between Input and Output and increase the gain of the LNA. This type of cascode amplifier is called the telescopic cascode amplifier since the cascode transistor is the same type as the input transistor. On the other hand, a folded cascode amplifier has a cascode transistor with a different type from the input transistor [5]. The
cascode topology results in a higher gain, due to the increase in the output impedance by \((g_{o2} + g_{o2b})r_{o2}r_{o1}\), as well as better isolation between the input and output ports. The cascode transistor Q2 reduces the voltage gain of Q1 so that it reduces the Miller capacitance of Q1 thereby increasing the reverse isolation [6]. On the other hand Q2 transfers the current \(I_{D1}\) to \(R_L\) by keeping the overall gain equal to the basic common source cell and it reduces Miller effect. It also improves the high frequency operation of the amplifier by suppressing the parasitic capacitances.

The shunt-feedback LNA is shown in Fig. 3. The resistive shunt-feedback provides wideband input and output match with small noise figure (NF) degradation by reducing the \(Q\)-factor of the narrowband LNA input and flattens the passband gain. It is able to attain a very high linearity [8]. The linearity of the amplifier improves since the gain, which is largely set by feedback, becomes less sensitive to the gain of the amplifier. The feedback elements are composed of a resistor in series with a capacitor which linearize the gain and increase the bandwidth of the amplifier. Using feedback is also suited for the CMOS LNA since the input impedance of MOSFETs is large and mostly capacitive, which means that the input impedance can be controlled and set by feedback. To progress the high frequency performance, an additional inductor can be placed in series with the capacitor and resistor [8].
d. Current Reuse Common Gate Low Noise Amplifier

The current reuse Common Gate LNA as shown in Fig 4. The CG LNA has better reverse isolation and robustness than CS LNA. The use of a CG input stage improves stability over the design of CS LNA. It achieves noise and gain performance comparable to a CS-CS current-reuse LNA, and consumes considerably less power and chip area. Current reuse technique improves the Transconductance while keeping the current constant. Otherwise it reduces the current by half while keeping the Transconductance constant to consume less power.

![Fig 4. Current Reuse CG UWB LNA](image)

A resistive current reuse and dual inductive degeneration techniques are implemented in the first stage for broadband simultaneous noise and input impedance matching [6]. An inductive peaking technique is implemented in the second stage for bandwidth enhancement. Combining a NMOS and a PMOS transistor between the two supply rails, the current reuse technique allows it to be low voltage compatible. The resistive current reuse amplifier boosts circuit Transconductance and utilizes DC current reuse to save power consumption.

III. CIRCUIT DESIGN

WiMAX receiver performance requirements are specified in Table 1. These receiver specifications are based on IEEE 802.16. The next part of the design includes the mapping of the specifications from the IEEE standard to relevant system level parameters such as Bit Error Ratio (BER), Signal-to-Noise Ratio (SNR), and receiver sensitivity. These system level specifications are then mapped into block-level using link budget analysis [10].

### Table 1: Performance requirements of WiMAX Receiver

<table>
<thead>
<tr>
<th>Parameter</th>
<th>WiMAX Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radio Technology</td>
<td>MIMO-SOFDMA</td>
</tr>
<tr>
<td>Range</td>
<td>30 miles(50km)</td>
</tr>
<tr>
<td>Speed</td>
<td>70Mbps</td>
</tr>
<tr>
<td>Frequency range</td>
<td>2 to</td>
</tr>
<tr>
<td>Receiver maximum input level on channel reception tolerance</td>
<td>&gt;=30dBm</td>
</tr>
<tr>
<td>Rx max. input level on-channel damage tolerance</td>
<td>&gt;= 0 dBm</td>
</tr>
<tr>
<td>Channel Bandwidth</td>
<td>2 to 20 MHz</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>&lt;=7dB</td>
</tr>
<tr>
<td>1st adjacent channel rejection</td>
<td>&gt;=4dBm</td>
</tr>
<tr>
<td>2nd adjacent channel rejection</td>
<td>&gt;=23dBm</td>
</tr>
</tbody>
</table>

The block level specifications for LNA are listed in Table 2. The LNA should be able to achieve high gain and low noise figure to ease the gain requirement of the mixer. At the same time LNA gives low noise figure to whole receiver. The noise figure also decides the minimum input signal that can be determined by the LNA while the linearity decides the maximum input signal level that will not cause nonlinear operation. The LNA should have finite reverse isolation and it is directly connected to the antenna, require a good input and output match to prevent signals from leaking back to the antenna and getting retransmitted which causes unwanted interference.

### Table 2: Receiver front end block level specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>20 dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>3 dB</td>
</tr>
<tr>
<td>Linearity</td>
<td>-10 dBm</td>
</tr>
<tr>
<td>Input and Output Matching</td>
<td>&lt; -10dB</td>
</tr>
</tbody>
</table>

A. Cascoded common source amplifier

The input impedance of the cascaded common-source LNA is given in (1) where $g_m$, $C_{gs}$, $L_2$, and $L_3$ are the input transistor’s Transconductance, input transistor gate-to-source capacitance, gate inductance, and source inductance respectively. The input impedance reduces to (3) at the resonant frequency given in (2). The width of the input transistor $Q1$ that will give the required Transconductance was set based on (2). The degenerating inductor $L_3$, gives the real input impedance of LNA, was computed based on (3).

With the value of $L_3$ determined, the value of the gate inductance $L_2$, that will set the resonant
frequency, can be calculated. The width of the cascode transistor $Q_2$ was set equal to the width of the input transistor to take advantage of the reduced junction capacitance in the layout. Finally, the output matching network, composed of the drain inductor, $L_1$, and the output capacitors, $C_1$ and $C_2$, can be designed. Fig. 4 shows the final schematic design of the cascoded common-source with device.

$$Z_{in} = \frac{g_m}{C_{gs}} \cdot L_3 + \frac{1}{s \cdot C_{gs}} + s \cdot (L_2 + L_3)$$ (1)

$$\omega_0 = \frac{1}{\sqrt{(L_2+L_3) \cdot C_{gs}}}$$ (2)

$$Z_{in} = \frac{g_m}{C_{gs}} \cdot L_3 \text{ (At Resonance)}$$ (3)

The design of the folded cascode LNA is analogous to the design of the telescopic cascode LNA. The real input impedance decided by source inductance $L_s$ while the gate inductance $L_g$ is computed based on the resonance frequency. The inductor $L_D$ resonates with the drain junction capacitance of $Q_1$ and the source junction capacitance of $Q_2$. The inductor $L_{Load}$ and capacitors $C_1$ and $C_2$, make up the output matching network. Fig. 5 shows the final schematic design of the folded cascode LNA.

C. Shunt Feedback Amplifier

Power Gain can adjusted by the value of feedback resistor in shunt feedback LNA is given in equation (4) where $R_f$, $Z_0$, and $S_{21}$ are the values of the feedback resistor, output impedance, and the transducer gain. Inductor $L_s$ is added for simultaneous noise and input output matching and $L_g$ is placed for impedance matching between $R_s$ and input of the LNA. A small inductor $L_3$ is placed at the gate of the transistor $Q_4$ to aid in matching. Here $R_f$ acts as shunt feedback resistor while $L_{load}$ is used as shunt peaking inductor at output. The value of the feedback capacitor is used for biasing purposes should be adjusted as large as enough to avoid the effect of feedback. A load inductor $L_{load}$ was placed at the drain of the transistor to tune out the junction capacitances. The capacitances $C_f$, $C_1$ and $C_2$ is used for a.c coupling purpose. The schematic design of shunt feedback amplifier is given Fig 6.

$$R_f = Z_0 (1 + |S_{21}|)$$ (4)
D. Current Reuse Common Gate Low Noise Amplifier

Resistive current reuse amplifier utilizes DC current reuse to save power consumption in the circuit and it increases the transconductance. The total equivalent transconductance is increased from $g_{mn}$ to $g_{mn} + g_{mp}$ for the same biasing current. The schematic diagram of current reuse CG LNA, including the biasing circuit is shown in Fig 7. It is composed of two simple amplifiers with an inter-stage inductor connected. The first stage of Amplifier is to increase the voltage gain and with low DC power supply voltage, it adopts a current reuse topology (QN and QP) with the self-biasing by a feedback resistor RF as shown in Fig 7. The main problem with the use of resistive current reuse in the LNA is that the parasitic capacitances due to the Miller effect which causes degradation of input impedance and the −3 dB bandwidth at high frequency. To overcome this problem, dual source degenerated inductors (Ls1 and Ls2) and inter-stage inductor L2 are proposed for the tuning of the parasitic capacitances. LC network (L1 and C1) combined with the dual degenerated inductors (Ls1 and Ls2) for input matching and the intrinsic capacitances of current reuse topology to form a multisection LC ladder network to achieve a wideband matching characteristic to 50Ω. The total transconductance $g_{mnT}$ in this stage is

$$g_{mnT} = g_{mn} + g_{mp} \frac{1+j\omega Ls1}{1+j\omega Ls1}$$  (5)

The voltage gain $A_{V1}$ of the first stage LNA

$$A_{V1} = g_{mnT} \frac{(1+j\omega Ls1)R_{mp}}{(1+j\omega Ls2)Zin}$$  (6)

The input impedance $Zin$ of LNA

$$Zin = \frac{j\omega Ls1}{Z_{in}}$$  (7)

Where $\omega$ is the operation frequency, $R_{mp}$ and $R_{mp}$ are the output resistances of QN and QP, $Z_{in}$ is the input impedance from the dual source inductive degeneration technique, and $Z_{in}$ is the input impedance from the shunt feedback technique. In the proposed LNA topology, the use of dual inductive degeneration through LS1 and LS2 with current reuse configuration is also beneficial to low noise design. In this design, the inductors L1, Ls1, and Ls2 are chosen to be the same as 0.45 mH, the feedback resistor RF is chosen as 900Ω and the width of QN (QP) is set to 90 nm.

IV. RESULTS

Standard 90nm CMOS process is used to design the LNA topologies. The low noise amplifiers were designed to operate at the Unlicensed National Information Infrastructure (U-NII) band of 5.75 GHz to 5.85 GHz. Measurement is taken at 5.8GHz.

Fig 7. Current Reuse Common Gate LNA

The simulation results and plots are shown in the figures below. Fig. 8 shows the plot of the Noise Figure. The shunt feedback amplifier achieved the highest gain with 19.792 dB followed by the cascaded common-source with 13.796 dB and the folded cascode achieved the lowest gain with a gain of 12.893 dB. As can be seen on the plot of the power gain, the shunt feedback amplifier has a relatively wideband characteristic compared to the cascode amplifiers. The linearizing effect of feedback gives the shunt feedback amplifier its wideband characteristic compared to the narrowband characteristic of the cascode amplifiers. The plot of the total DSB noise figure is shown in Fig. 8. The extracted noise figures of the LNA topologies are as follows: 1.7 dB for the cascoded common-source, 1.79 dB for the folded cascode, and 2.63 dB for the shunt feedback amplifier. All the LNA topologies achieved a noise figure below 3 dB. As with the power gain plot, the shunt feedback amplifier achieved the most linear noise figure plot among the three. The plot of the stability factor is shown in Fig. 9. The three amplifiers are unconditionally stable with stability factor greater than 1 at the frequency of interest. Table 3 summarizes the simulation results for input voltage reflection coefficient (S11), output voltage reflection coefficient (S22), and reverse isolation or reverse gain (S12).
Stability factor plot is shown in figure 10. The four amplifiers are unconditionally stable with stability factor greater than 1 at the frequency of interest.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Frequency (GHz)</th>
<th>Pdc (mW)</th>
<th>Gain (dB)</th>
<th>IIP3</th>
<th>NF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cascoded CS</td>
<td>5.8</td>
<td>19.3</td>
<td>13.82</td>
<td>-7.42</td>
<td>1.7</td>
</tr>
<tr>
<td>Folded Cascode</td>
<td>5.8</td>
<td>47.4</td>
<td>12.94</td>
<td>-6.18</td>
<td>1.8</td>
</tr>
<tr>
<td>Shunt feedback</td>
<td>5.8</td>
<td>55.5</td>
<td>20.11</td>
<td>-5.11</td>
<td>2.7</td>
</tr>
<tr>
<td>Current Reuse CG</td>
<td>5.8</td>
<td>16.1</td>
<td>17.6</td>
<td>-7.34</td>
<td>1.8</td>
</tr>
</tbody>
</table>

The summary of various parameters for the four designed low noise amplifiers is shown in Table 4. The folded cascode LNA was presented in while the shunt feedback amplifier was presented in [8]. It is seen that the cascoded common-source LNA achieved the highest FOM among the three and its FOM is comparable to previously published works. Due to the high gain and high linearity of the shunt feedback amplifier, we decided to use it in the implementation of a receiver front-end.
FOM = |Gain| IIP3 (mw) * f_c (GHz) / |NF-1|* PDC (mw)
Where NF stands for Noise Figure, IIP3 stands for third order input intercept point, f_c is the operating frequency and PDC is the DC power dissipation.

V. CONCLUSION
Various low noise amplifiers are presented to design the RF front end of WiMAX receiver. The four low-noise amplifier topologies are: the cascaded common-source amplifier, the folded cascode amplifier, the shunt feedback amplifier, and the current reuse CG LNA. A standard 90nm CMOS technology with 1-V supply voltage is used to design these LNAs. The target operating frequency is in the U-NII band of 5.7 GHz to 5.8 GHz. The cascaded commonsource amplifier attained the lowest noise figure among the four due to better input matching using inductive degeneration. The folded cascode amplifier also bonds this topology, attains low noise figure. The cascaded common source amplifier also accomplished the lowest power dissipation because it contains only one current branch. Due to low voltage operation of folded cascode amplifier reduces power dissipation thus it will used in low power applications. The shunt feedback amplifier attained the highest gain by changing the value of the feedback resistor. The current reuse topology proposed in narrow band LNA designs can successfully extended to UWB applications. The two stage ultra wideband LNA provides higher power gain, wideband input matching and high figure of merit among four amplifier configurations. The current reuse CG LNA amplifier good linear performance makes a very good choice in the implementation of a wideband receiver. Its only disadvantage is that it has a higher noise figure compared to the other three LNAs.

REFERENCES:
[8] Lee J H, Chen C C, Lin Y S. 0.18 _m 3.1–10.6 GHz CMOS UWB LNA with 11.4 _ 0.4 dB gain and 100.7 – 17.4 ps group-delay, Electron Lett. 2007, 43(24): 1359.