Low power Design and Analysis of Low Noise Amplifiers for RF receiver front end using 90nm CMOS

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Abstract

This letter presents the design of low-noise amplifiers for wireless receiver front ends. Several low noise amplifier topologies are implemented namely: (1) cascaded common-source amplifier, (2) folded cascode amplifier, (3) shunt feedback amplifier and (4) Current-Reuse g_m boosted CG LNA. The amplifiers were implemented in a standard 90-nm CMOS process and were operated with a 1-V supply voltage. Low-noise amplifier measurements were taken for parameters such as power gain, noise figure, input matching, output matching, reverse isolation, stability, and linearity. Based on the employed figure-of-merit, the cascoded common-source low-noise amplifier achieved the best performance among the four with a simulated gain of 13.8 dB and noise figure of 1.7 dB, which makes it comparable to previously available works.

Keywords - CMOS Process; Low-noise amplifier; Figure of Merit.

I. Introduction

The overwhelming technological advances in CMOS scaling and RF CMOS circuit design techniques in the past few years have made it possible to integrate all the elements of a transceiver on a single chip. Now a days most of the systems uses battery operated devices. So it must consume very low power. Low power, less expensive CMOS technologies have been used successfully to implement all the necessary RF functionality for existing and emerging wireless area network standards, such as Bluetooth Wi-Fi and WiMAX [1]. A CMOS system-on-chip (SOC) solution to enable a single-chip cell phone, where the analog and digital basebands, power management, and the RF transceiver are fully integrated on a single monolithic CMOS IC, has been reported [2].

WiMAX is a wireless communication standard which stands for Worldwide Interoperability for Microwave Access. It belongs to the IEEE 802.16 family of standards, which provides wireless broadband access. It provides data rates of up to 100 Mbps (in a 20 MHz channel using 64QAM ¾ code rate) [3]. It has a very large coverage area of around 10 km from a WiMAX base station for point-to-multipoint, non-line-of-sight (see following pages for illustrations and definitions) service. There are two types of WiMAX systems: Fixed WiMAX and Mobile WiMAX. The fixed WiMAX system doesn't allow handoff mechanism between base stations whereas Mobile WiMAX provides both mobile and fixed services [4].

The rest of the letter organized as follows: Section 2 of this letter describes the topologies of the implemented low noise amplifiers. Section 3 presents the circuit design. The simulation results are presented in section 4 followed by the conclusion in section 5.

II. Low Noise Amplifiers

The low-noise amplifier (LNA) is the first block in the receiver chain of a communications system, connected directly to the antenna. Its noise figure (NF) performance has the most impact to the overall receiver system. Its job is to amplify the weak signals coming from the antenna while adding as little noise as possible. NF is a crucial design specification which trades off with additional design parameters like third order input intercept point (IIP3), second order input intercept point (IIP2), power consumption and gain.

a. Cascoded Common Source Low Noise Amplifier

The most frequently used architecture for LNA design today is the cascode amplifier with inductive source degeneration shown in the Fig 1.A cascode stage was employed to improve isolation between Input and Output and increase the gain of the LNA. This type of cascode amplifier is called the telescopic cascode amplifier since the cascode transistor is the same type as the input transistor. On the other hand, a folded cascode amplifier has a cascode transistor with a different type from the input transistor [5]. The

cascode topology results in a higher gain, due to the increase in the output impedance by $(g_{Q2}+g_{Qb2}) r_{o2}.r_{o1}$, as well as better isolation between the input and output ports. The cascode transistor Q2 reduces the voltage gain of Q1 so that it reduces the Miller capacitance of Q1 thereby increasing the reverse isolation [6]. On the other hand Q2 transfers the current I_{D1} to R_L by keeping the overall gain equal to the basic common source cell and it reduces miller effect. It also improves the high frequency operation of the amplifier by suppressing the parasitic capacitances.
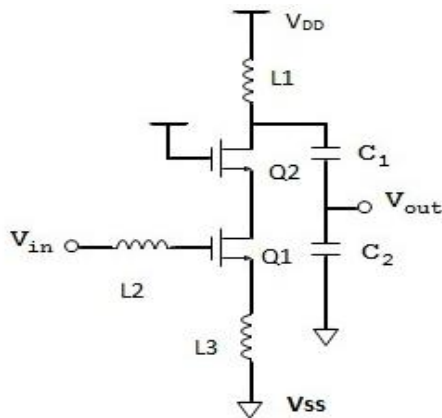

Fig 1. Cascoded Common Source Amplifier

b. Folded Cascode Amplifier

Folded cascode topology is fit if the LNA is recommended for very low-voltage application as shown in Fig 2. It is operated with low supply voltages as the PMOS and NMOS transistors are placed in parallel between the supply and ground rail, compared to the telescopic cascode amplifiers. The PMOS cascode transistor Q2 diminishes the input capacitance and offers good reverse isolation and improves stability [7].The projected amplifier
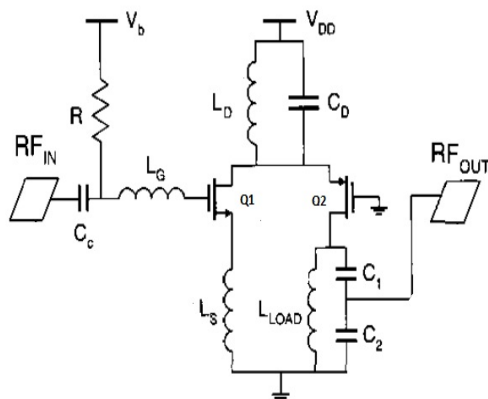

Fig 2. Folded Cascode Amplifier

provides the same performance as that of the conventional symmetric folded cascode amplifier while consuming only 60% the power. This is attained by recycling the bias current of idle devices, with enhanced Transconductance, gain and slew rate.

c. Shunt Feedback Low Noise Amplifier

The shunt-feedback LNA is shown in Fig. 3. The resistive shunt-feedback provides wideband input and output match with small noise figure (NF) degradation by reducing the *Q*-factor of the narrowband LNA input and flattens the passband gain. It is able to attain a very high linearity [8]. The linearity of the amplifier improves since the gain, which is largely set by feedback, becomes less sensitive to the gain of the amplifier. The feedback elements are composed of a resistor in series with a capacitor which linearize the gain and increase the bandwidth of the amplifier. Using feedback is also suited for the CMOS LNA since the input impedance of MOSFETs is large and mostly capacitive, which means that the input impedance can be controlled and set by feedback. To progress the high frequency performance, an additional inductor can be placed in series with the capacitor and resistor [8].
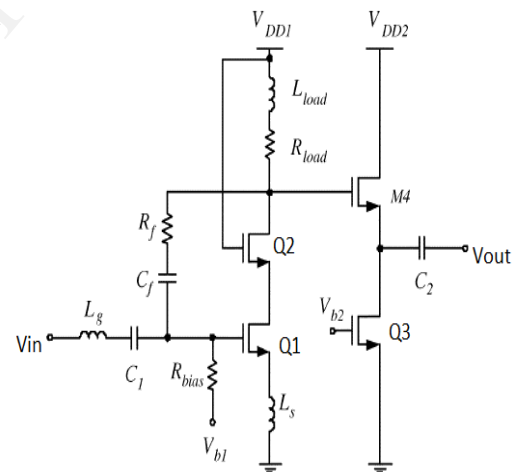

Fig 3. Shunt Feedback Amplifier

The band pass filter based topology includes the input impedance of the cascode amplifier as a part of the filter, and gives good performance while dissipating small amounts of dc power. The adoption of the filter at the input produces a number of reactive elements, which could lead to a larger chip area and NF degradation in the case of on-chip implementation, or the additional external components.

d. Current Reuse Common Gate Low Noise Amplifier

The current reuse Common Gate LNA as shown in Fig 4. The CG LNA has better reverse isolation and robustness than CS LNA. The use of a CG input stage improves stability over the design of CS LNA. It achieves noise and gain performance comparable to a CS-CS current-reuse LNA, and consumes considerably less power and chip area. Current reuse technique improves the Transconductance while keeping the current constant. Otherwise it reduces the current by half while keeping the Transconductance constant to consume less power.
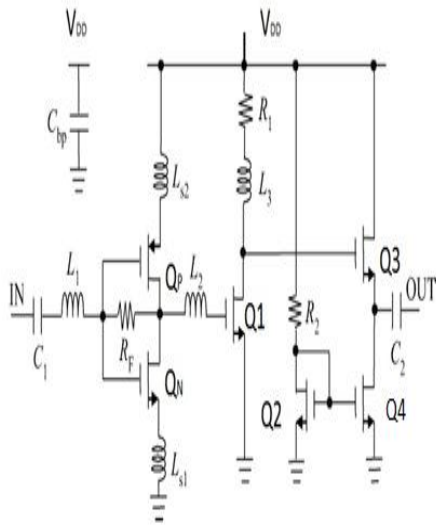

Fig 4. Current Reuse CG UWB LNA

A resistive current reuse and dual inductive degeneration techniques are implemented in the first stage for broadband simultaneous noise and input impedance matching [6]. An inductive peaking technique is implemented in the second stage for bandwidth enhancement. Combining a NMOS and a PMOS transistor between the two supply rails, the current reuse technique allows it to be low voltage compatible. The resistive current reuse amplifier boosts circuit Transconductance and utilizes DC current reuse to save power consumption.

III. CIRCUIT DESIGN

WiMAX receiver performance requirements are specified in Table 1. These receiver specifications are based on IEEE 802.16. The next part of the design includes the mapping of the specifications from the IEEE standard to relevant system level parameters such as Bit Error Ratio (BER), Signal-to- Noise Ratio (SNR), and receiver sensitivity. These system level specifications are then mapped into block-level using link budget analysis [10].

Table 1: Performance requirements of WiMAX Receiver

Parameter	WiMAX Specification
Radio Technology	MIMO-SOFDMA
Range	30 miles(50km)
Speed	70Mbps
Frequency range	2 to
Receiver maximum input level on channel reception tolerance	>=30dBm
Rx max. input level on-channel damage tolerance	>= 0 dBm
Channel Bandwidth	2 to 20 MHz
Noise Figure	<=7dB
1st adjacent channel rejection	>=4dBm
2nd adjacent channel rejection	>=23dBm

The block level specifications for LNA are listed in Table 2. The LNA should be able to achieve high gain and low noise figure to ease the gain requirement of the mixer. At the same time LNA gives low noise figure to whole receiver. The noise figure also decides the minimum input signal that can be determined by the LNA while the linearity decides the maximum input signal level that will not cause nonlinear operation. The LNA should have finite reverse isolation and it is directly connected to the antenna, require a good input and output match to prevent signals from leaking back to the antenna and getting retransmitted which causes unwanted interference.

Table 2: Receiver front end block level specifications

Parameter	LNA
Gain	20 dB
Noise Figure	3 dB
Linearity	-10 dBm
Input and Output Matching	< -10dB

A. Cascoded common source amplifier

The input impedance of the cascoded common-source LNA is given in (1) where gm, Cgs, L2, and L3 are the input transistor's Transconductance, input transistor gate-to-source capacitance, gate inductance, and source inductance respectively. The input impedance reduces to (3) at the resonant frequency given in (2). The width of the input transistor Q1 that will give the required Transconductance was set based on (2). The degenerating inductor L3, gives the real input impedance of LNA, was computed based on (3). With the value of L3 determined, the value of the gate inductance L2, that will set the resonant

frequency, can be calculated. The width of the cascode transistor Q2 was set equal to the width of the input transistor to take advantage of the reduced junction capacitance in the layout. Finally, the output matching network, composed of the drain inductor, L1, and the output capacitors, C1 and C2, can be designed. Fig. 4 shows the final schematic design of the cascoded common-source with device.

$$Zin = \frac{gm}{Cgs} \cdot L3 + \frac{1}{s.Cgs} + s.(L2 + L3) \quad (1)$$

$$\omega_0 = \frac{1}{\sqrt{(L2+L3).Cgs}} \quad (2)$$

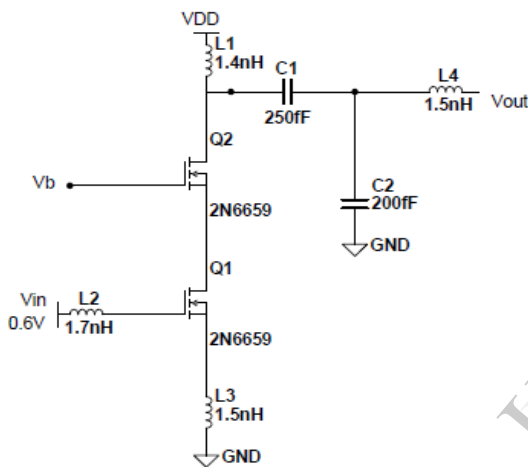$$Zin = \frac{gm}{Cgs} \cdot L3 \text{ (At Resonance)} \quad (3)$$

Fig 4. Cascoded Common Source Amplifier Schematic
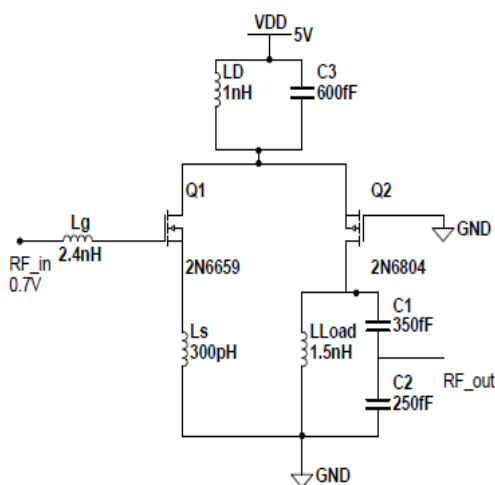
B. Folded Cascode Amplifier

Fig 5. Folded Cascode Amplifier schematic

The design of the folded cascode LNA is analogous to the design of the telescopic cascode LNA. The real input impedance decided by source inductance L_S while the gate inductance L_G is computed based on the resonance frequency. The inductor L_D resonates with the drain junction capacitance of Q1 and the source junction capacitance of Q2. The inductor L_{Load} and capacitors C1 and C2, make up the output matching network. Fig 5 shows the final schematic design of the folded cascode LNA.

C. Shunt Feedback Amplifier

Power Gain can adjusted by the value of feedback resistor in shunt feedback LNA is given in equation (4) where Rf, Zo, and S21 are the values of the feedback resistor, output impedance, and the transducer gain. Inductor Ls is added for simultaneous noise and input output matching and Lg is placed for impedance matching between Rs and input of the LNA.A small inductor L3 is placed at the gate of the transistor Q4 to aid in matching. Here Rf acts as shunt feedback resistor while Lload is used as shunt peaking inductor at output. The value of the feedback capacitor is used for biasing purposes should be adjusted as large as enough to avoid the effect of feedback.A load inductor Lload was placed at the drain of the transistor to tune out the junction capacitances. The capacitances Cf, C1 and C2is used for a.c coupling purpose. The schematic design of shunt feedback amplifier is given Fig 6.
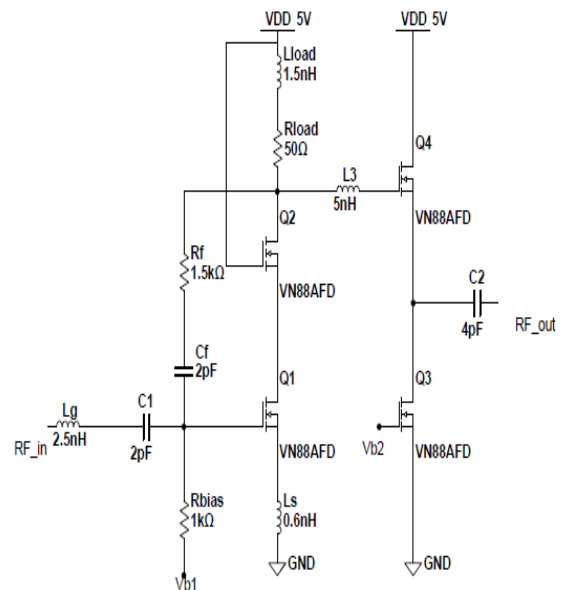
$$R_f = Z_0 (1+|S_{21}|) \quad (4)$$

Fig 6: Schematic of Shunt Feed Back Amplifier

D. Current Reuse Common Gate Low Noise Amplifier

Resistivecurrent reuse amplifier utilizes DC current reuse to save power consumption in the circuit and it increasesthe Transconductance. The total equivalent transconductance isincreased from g_{mn} to $g_{mn}+g_{mp}$ for the same biasing current.The schematic diagram of current reuse CG LNA,including the biasing circuit is shown in Fig 7.It composedof two simple amplifiers with an inter-stage inductorconnected. The first stage of Amplifier is to increasethe voltage gain and with low DC power supply voltage, it adopts a current reuse topology (QN and QP) with the self-biasing by a feedback resistor RF as shown in Fig 7. The main problem with theuse of resistive current reuse in the LNA is that the parasiticcapacitances due to the Miller effect which causes to degradation of inputimpedance and the −3 dB bandwidth at high frequency.To overcome this problem, dual source degenerated inductors(Ls1 and Ls2/ and inter-stage inductor L2 are proposed for thetuning of the parasitic capacitances.LC network (L1 andC1) combinedwith the dual degenerated inductors (Ls1 and Ls2)for input matching and the intrinsiccapacitances of current reuse topology to form a multisectionLC ladder network to achieve a wideband matching characteristic to 50Ω. The total transconductancegmT in this stage is

$$g_m T = \frac{gmn}{1+j\omega Ls\,1.gmn} + \frac{gmp}{1+j\omega Ls\,2.gmp} \qquad (5)$$

The voltage gainAV1 of the first stage LNA

$$A_{V1}=g_mT.\,[(1+j\omega Ls1.g_{mn}).R_{on}//\,(1+j\omega Ls2.g_{mp}).R_{op}//Zin]\,(6)$$

The input impedance Zin of LNA

$$Zin = j\omega L1 + Z_{sd}// Z_{fb} \qquad (7)$$

Where ω is the operation frequency, $R_{on}$and R_{op} are the outputresistances of QN and QP, Z_{sd} is the input impedance from the dual source inductive degeneration technique, and Z_{fb} is the input impedance from the shunt feedback technique. In the proposedLNA topology, the use of dual inductive degeneration throughLS1 and LS2 with current reuse configuration is also beneficialto low noise design. In this design, the inductors L1, LS1 andLS2 are chosen to be the same as 0.45 nH, the feedback resistorRF is chosen as 900Ω and the width of QN (QP) is set to90 nm.

IV. RESULTS

Standard 90nm CMOS process is used to design the LNA topologies. The low noise amplifiers weredesigned to operate at the Unlicensed National InformationInfrastructure (U-NII) band of 5.75 GHz to 5.85 GHz. Measurement is taken at 5.8GHz.
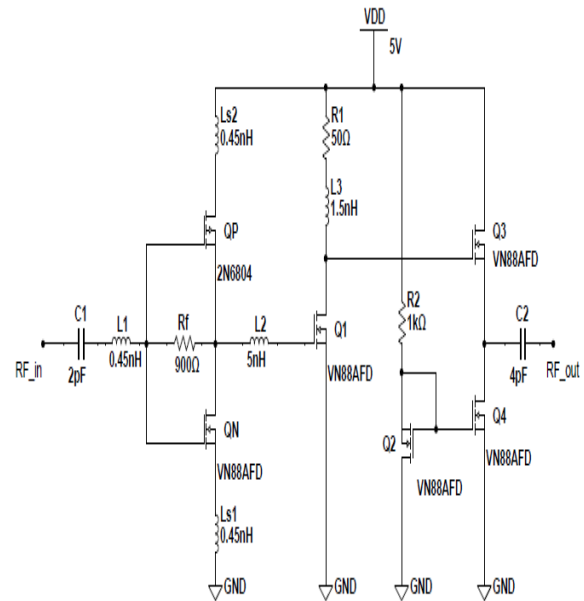

Fig 7.Current Reuse Common Gate LNA

The simulation results and plots are shown in the figures below. Fig. 8 shows the plot of the Noise Figure. The shunt feedback amplifier achieved the highest gain with 19.792 dB followed by the cascoded common-source with 13.796 dB and the folded cascode achieved the lowest gain with a gain of 12.893 dB. As can be seen on the plot of the power gain, the shunt feedback amplifier has a relatively wideband characteristic compared to the cascode amplifiers. The linearizing effect of feedback gives the shunt feedback amplifier its wideband characteristic compared to the narrowband characteristic of the cascode amplifiers. The plot of the total DSB noise figure is shown in Fig. 8. The extracted noise figures of the LNA topologies are as follows: 1.7 dB for the cascoded common-source, 1.79 dB for the folded cascode, and 2.63 dB for the shunt feedback amplifier. All the LNA topologies achieved a noise figure below 3 dB. As with the power gain plot, the shunt feedback amplifier achieved the most linear noise figure plot among the three. The plot of the stability factor is shown in Fig. 9. The three amplifiers are unconditionally stable with stability factor greater than 1 at the frequency of interest. Table 3 summarizes the simulation results for input voltage reflection coefficient (S11), outputvoltage reflection coefficient (S22), and reverse isolation or reverse gain (S12).

──── Folded Cascode LNA
──── Cascoded Common source LNA
Shunt feedback LNA
──── Current reuse Common gate LNA

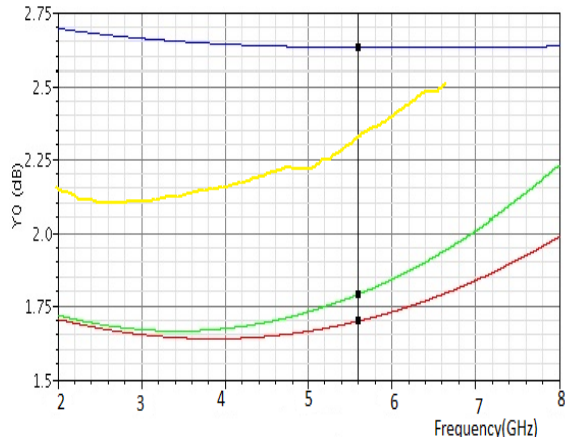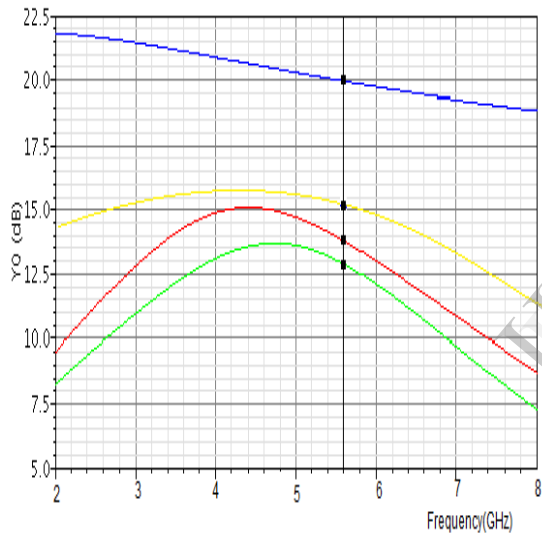

Fig 8.Noise Figure

Fig 9.Power Gain

Stability factor plot is shown in figure 10.The four amplifiers are unconditionally stable with stabilityfactor greater than 1 at the frequency of interest.

Table 3:S-parameters

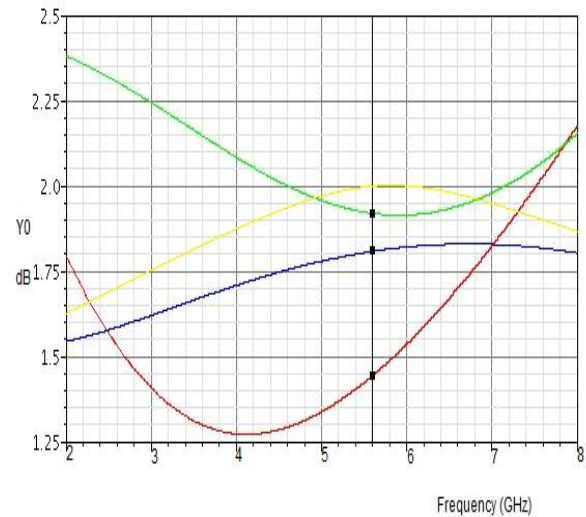| Circuit	S11	S22	S12
Target	-10	-10	-20
Cascoded CS	-9.55	-14.5	-23.8
Folded Cascode	-12.4	-9	-26.03
Shunt feed back	-11.36	-23.96	-31.24
Current Reuse CG	-9.7	-10.24	-46

Fig 10:Stability factor

All the amplifiersachieved a reverse isolation better than -20 dB. The current reuse CG LNA achieves the best reverse isolation with 46dB. The amplifier's linearity can be measured using the inputreferredthird-order intercept point (IIP3). This figure-of-merit is calculated bygain to dc power consumption. Figure of merit which incorporates linearity in the form of theinput-referred third-order intercept point (IIP3), and theoperating frequency (fc).

Table 4:Comparison of Various Parameters

Circuit	Frequency(GHz)	P_{DC}(mW)	Gain(dB)	IIP3	NF
Cascoded CS	5.8	19.3	13.82	-7.42	1.7
Folded Cascode	5.8	47.4	12.94	-6.18	1.8
Shunt feed back	5.8	55.5	20.11	-5.11	2.7
Current Reuse CG	5.8	16.1	17.6	-7.34	1.8

The summary of various parameters for the four designed low noiseamplifiers is shown in Table 4. The folded cascode LNAwas presented in while the shunt feedback amplifier waspresented in [8]. It is seen that the cascoded common-source LNA achieved the highest FOM among the three and its FOM is comparable to previously published works. Due to the high gain and high linearity of the shunt feedback amplifier, we decided to use it in the implementation of a receiver front-end.

$$FOM = \{|Gain|* IIP3\ (mw) * f_c\ (GHz)\}/\ |NF-1|* P_{DC}\ (mw)$$

Where NF stands for Noise Figure, IIP3 stands for third order input intercept point, fc is the operating frequency and P_{DC}isthe DC power dissipation.

V. CONCLUSION

Various low noise amplifiers are presented to design the RF front end of WiMAX receiver. The four low-noise amplifier topologies are: the cascoded common-source amplifier, the folded cascode amplifier, the shunt feedback amplifier, and the current reuse CG LNA. A standard 90nm CMOS technology with 1-V supply voltage is used to design these LNAs. The target operating frequency is in the U-NII band of 5.7 GHz to 5.8 GHz. The cascoded commonsource amplifier attained the lowest noise figure among the four due to better input matching using inductive degeneration. The folded cascode amplifier also bonds this topology, attains low noise figure. The cascoded common source amplifier also accomplished the lowest power dissipation because it contains only one current branch. Due to low voltage operation of folded cascode amplifier reduces power dissipation thus it will used in low power applications.The shunt feedback amplifier attained the highest gain by changing the value of the feedback resistor. The current reuse topology proposed in narrow band LNA designs can successfully extended to UWB applications. The two stage ultra wideband LNA provides higher power gain, wideband input matching and high figure of merit among four amplifier configurations. The current reuse CG LNA amplifier good linear performance makes a very good choice in the implementation of a wideband receiver. Its only disadvantage is that it has a higher noise figure compared to the other three LNAs.

REFERENCES:

[1] Wikipedia Contributors. WiMAX (2009, April).InWikipedia, the free encyclopedia.*Retrieved July 2009*, fromhttp://en.wikipedia.org/wiki/WiMAX.

[2] Kalantari, Fatemeh, Masoumi et al., A Low Power 90 nm LNA with an Optimized Spiral Inductor Model for WiMax Front End. Circuits and Systems, 2006.MWSCAS '06.49th IEEE International Midwest Symposium on.

[3] Low-power 5 GHz LNA and VCO in 90 nm RF CMOS Interuniv. Microelectron. Center, Leuven, Belgium Aspemyr, L. ; Jeamsaksiri, W. ; Ramos, J. ; Mercha, A. ; Jenei, S. ; Thijs, S. ; Garcia, R. ; Jacobsson, H. ;Wambacq, P. ; Donnay, S. ; Decoutere, S.

[4] IEEE standard 802.16. "Air interface for Fixed BroadbandWireless Access Systems", part 16, Oct. 1, 2004.

[5] Lee, T., "The Design of CMOS Radio-Frequency Integrated Circuits," Cambridge: Cambridge University Press, 1998.Atallah, J. G., Rodriguez, S., Zheng, L.-R., Ismail, M.

[6] A Direct Conversion WiMAX RF Receiver Front-End in CMOS Technology. Signals, Circuits and Systems, 2007. ISSCS 2007. International Symposium on.Volume 1, 13- 14July 2007 Page(s):1 – 4.

[7] IEEE standard 802.16. "Air interface for Fixed Broadband Wireless Access Systems", part 16, Oct. 1, 2004.

[8] Lee J H, Chen C C, Lin Y S. 0.18 _m 3.1–10.6 GHz CMOS UWB LNA with 11.4 _ 0.4 dB gain and 100.7 _ 17.4 ps group-delay. Electron Lett, 2007, 43(24): 1359.

[9] Wang R L, Lin M C, Lin C C, et al. A 1 V full-band cascoded UWB LNA with resistive feedback. *IEEE International Workshop on Radio-Frequency Integration Technology, 2007: 188.*

[10] Lu Y, Yeo K S, Cabuk A, et al. A novel CMOS low-noise amplifier design for 3.1-to-10.6-GHz ultra-wide-band wireless receivers. *IEEE Trans Circuits*Syst I: Regular Papers, 2006, 53(8):1683

[11] Ismail A, Abidi A A. A 3–10-GHz low-noise amplifier with wideband LC-ladder matching network. *IEEE J Solid-State Circuits,* 2004, 39(12): 2269

[12] Razavi, B. (2001). Design of Analog CMOS Integrated Circuits. Boston: McGraw Hill.

[13] Johns, D.Ken Martin, K., "Analog Integrated Circuit Design," *Wiley*, 1996.

[14] R. Brederlow et al., "A mixed signal design readmap", IEEE Design & Test of Computers, Vol.18,No.6, nov.-Dec. 2001 pp.34-36.