Low Power Comparator Design Using Reversible Logic Gates- Adiabatic Circuits

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***Abstract*—In digital electronics, the major problem faced is about the power dissipation and the demand for reducing the power for devices is increasing day by day. In VLSI design, Power consumption plays a major role. Reversible and Adiabatic Logic gates are gaining more interest due to low power dissipation. This paper presents a novel design of reversible comparator using the reversible logic gates and adiabatic logic circuits. Minimizing the power dissipation is noticeable. The proposed designs are implemented using custom design flow of 180nm technology. All the components have been modeled and functionally verified using Cadence Software .**

Keywords—Power dissipation, VLSI design, Reversible logic gates, Adiabatic logic circits, custom design flow, Cadence software.

I. INTRODUCTION

During the operation of Conventional combinational logic circuits heat is dissipated for every bit of information. Therefore, the information lost cannot be recovered in any way. To overcome this difficulty reversible logic gates and adiabatic circuits are designed. This reversible circuits (gates) that have one to-one mapping between vectors of inputs and outputs; thus the input can be recovered by the output where the reversible is justified. Rolf Landauer, 1961. Used a logically irreversible gate and concluded that energy is dissipated to the environment. The loss of information is associated with laws of physics requiring that one bit of information lost dissipates k T ln 2 of energy, where k is Boltzmann‘ constant and T is the temperature of the system. Interest in reversible computation arises from the desire to reduce heat dissipation, thereby allowing:

- higher densities
- higher speed

Later Bennett, in 1973, showed that the construction of the reversible-adiabatic logic circuits avoids the KTln2 joules of Energy dissipation. A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs

Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in close proximity. One of the emerging applications of reversible logic is in quantum computers [3, 4]. A quantum computer consists of quantum logic gates. The quantum logic gates perform elementary unitary operation on one, two or more two– state quantum systems called qubits. In quantum computing qubit represents the elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible in nature and hence quantum computers must be built from reversible logical components.

An important constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed. A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit must produce minimum number of garbage outputs; also they must use minimum number of constant inputs [2].

II. DEFINATIONS

A. Reversible logic gates

Reversible are circuits (gates) that have one-to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states.

B. Comparator:

Comparing two binary words for equality is a commonly used operation in computer systems and device interfaces. A circuit that compares two binary words and indicates whether they are equal is called a comparator.

Some comparators interpret their input words as signed or unsigned numbers and also indicate arithmetic key relation between the words.

C. Adiabatic logic circuits:

The adiabatic logic is the term given to the low power electronics circuits that implement reversible logic. The term comes from the fact that an adiabatic process is the one in which the total het or energy in the system remains constant.

III. EXISTING COMPARATOR

The conventional one-bit irreversible numerical comparator, which consists of two NOT gates, two AND gates and one NOR gate as shown in fig 1.

$$\begin{cases} F_{A>B} = A\bar{B} \\ F_{A<B} = \bar{A}B \\ F_{A=B} = \overline{A \oplus B} \end{cases}$$

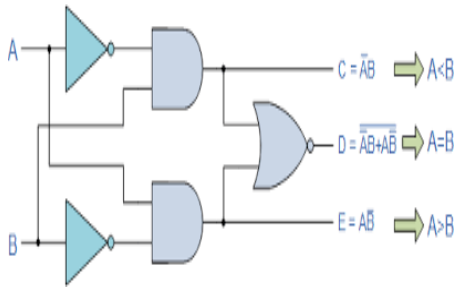

Fig. 1. One bit Comparator using basic gates

IV. REVERSIBLE GATES

These gates are defined as follows-

A. *Feynman Gate*

This gate is widely used for fan-out purposes. This Gate is 2*2 gate that means two to two mapping. This Feynman gate is also called as Controlled NOT and the input of this gate is A&B and output are P=A, Q= A ⊕B as shown in fig 2.

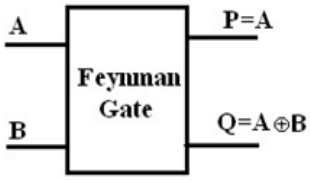

Fig. 2. Feynman Gate

B. *Peres Gate*

The Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs P = A , Q = A^B, R = AB^C , shown in fig 3.

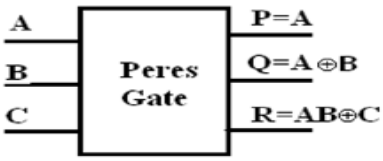

Fig. 3. Peres Gate

C. *Fredkin Gate*

The Fredkin gate which is a 3*3 gate with inputs (A, B, C) and outputs are P=A, Q=A'B+AC, R=AB+A'C as shown in fig 4.

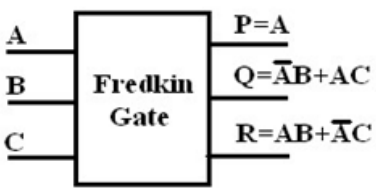

Fig. 4. Fredkin Gate

D. *R Gate*

The R-gate which is a 3*3gate with inputs (A,B,C) and outputs are P= A^B, Q= A, R = C'^AB shown in fig 5

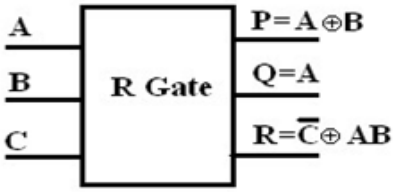

Fig. 5. R Gate

E. *Tr Gate*

The TR gate is a 3*3 gate with inputs (A, B, C) and outputs are P=A, Q=A^B, R= AB'^C shown in fig 6

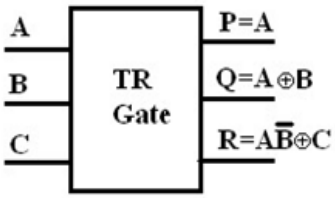

Fig. 6. TR Gate

F. *Urg gate*

The URG gate which is a 3*3 gate with inputs (A, B, C) and outputs are P= (A+B) ^ C, Q= B, R = ABC shown in fig 7.

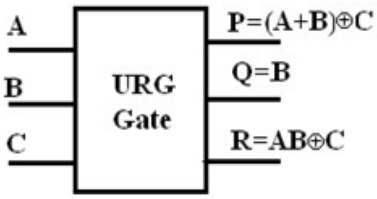

Fig. 7. URG Gate

G. *Bjn Gate*

BJN Gate is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=B, R =(A+B) ^ C as shown in fig 8

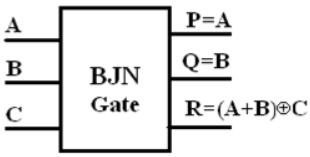

Fig. 8. BJN Gate

H. *Toffoli Gate*

Toffoli gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=B, R=AB^C as shown in the fig 9.

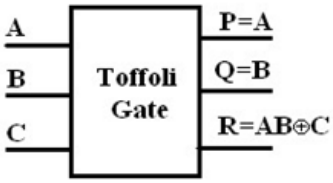

Fig. 9. Toffoli Gate

V. COMPARATOR DESIGNS

All the gates mentioned in section 2 can be used for the construction of reversible comparators.

A. One- bit comparator using Peres and BJN gate

The one bit comparator is implemented with Feynman gate and Peres gate and BJN gate as shown in fig 10. The number of garbage outputs are two and represented as G1 and G2, it uses three constant inputs one logic '0' and two logic '1'.

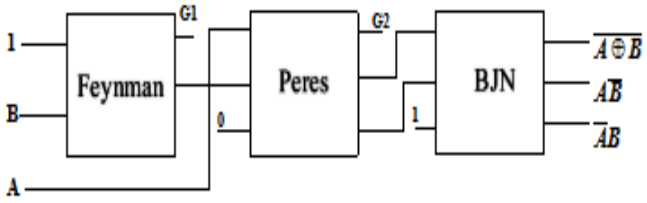

Fig. 10. one bit comparator using Peres gate

B. One bit comparator using Toffoli and BJN gate

The one bit comparator is implemented with Feynman gate and Toffoli gate as shown in fig 11. The number of garbage outputs are two and represented as G1 and G2, it uses three constant inputs , one logic '0' and two logic '1' it requires one Feynman gate and two Toffoli gates.

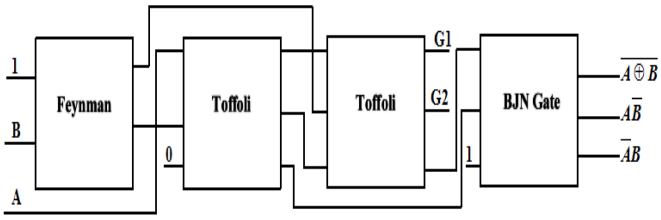

Fig. 11. one bit comparator using Toffoli Gate

C. One bit comparator using R and BJN gate

The one bit comparator is implemented with Feynman gate and R gate as shown in fig 12. The number of garbage outputs is two and represented as G1, it uses two constant logic '1' input. It requires one Feynman gate and one R gate.

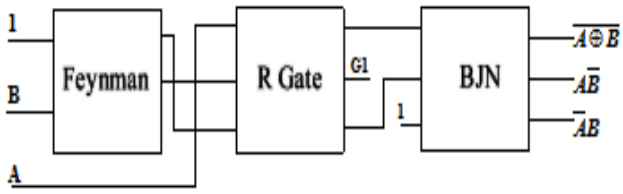

Fig. 12. one bit comparator using R gate

D. One bit comparator using URG and BJN gate

The one bit comparator is implemented with Feynman gate and URG gate as shown in fig.13. The number of garbage outputs are three and represented as G1,G2 and G3.It uses Four constant inputs two logic '0' and two logic '1'. It requires one Feynman gate and two URG gates and one BJN gate

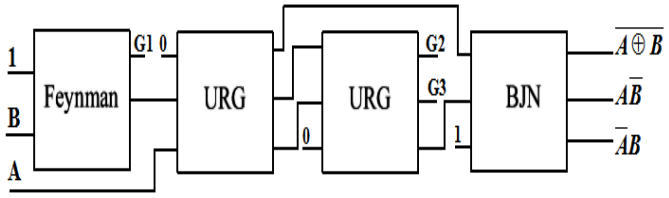

Fig. 13. One bit comparator using URG and BJN gates

E. One bit comparator using Fredkin and BJN gate

The one bit comparator is implemented with Feynman gate and Fredkin gate and BJN gate is as shown in fig. 14. The number of garbage outputs are six and represented with G1 to G6, it uses seven constant inputs, four logic '0' and three logic '1'. Two Feynman gates are used for fan-out purpose in the input part.

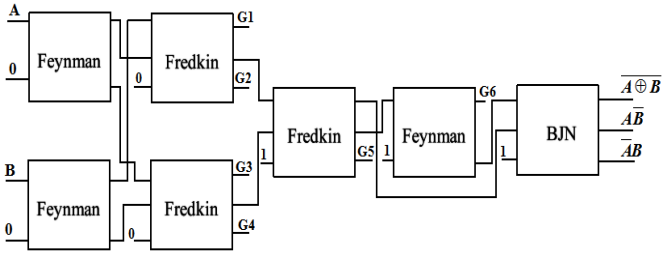

Fig. 14. one bit comparator using Fredkin and BJN gate

F. One bit comparator using TR and BJN gate

The one bit comparator is implemented with Feynman gate and TR gate and BJN gate as shown in fig.15. The number of garbage outputs are two and represented with G1 and G2, it uses three constant inputs, one logic '0' and two logic '1'.

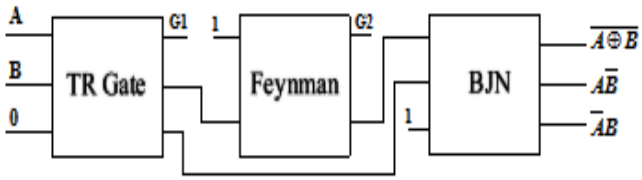

Fig. 15. One bit comparator using TR and BJN gate

VI. RESULTS AND DISCUSSIONS

A one bit comparators are designed with the help of reversible logic gates by using adiabatic(ecrl) circuit. The conventional comparator is designed and its power dissipated is found to be 72.68uW.

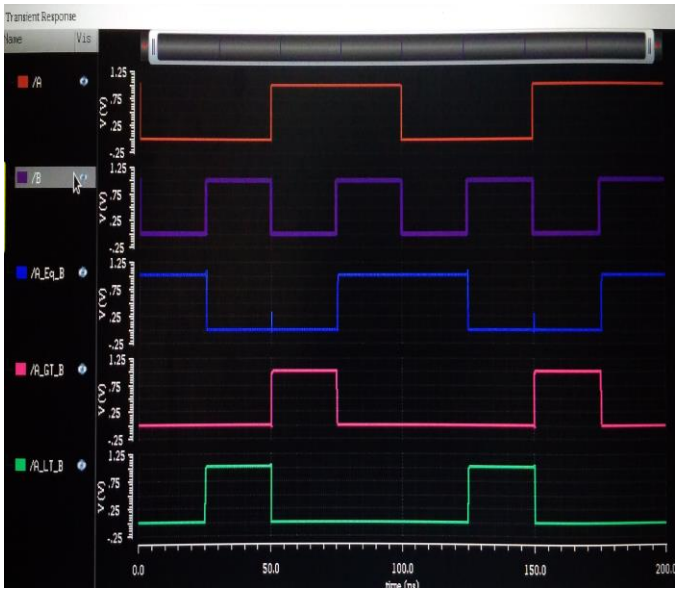

Fig. 16. Output Waveform

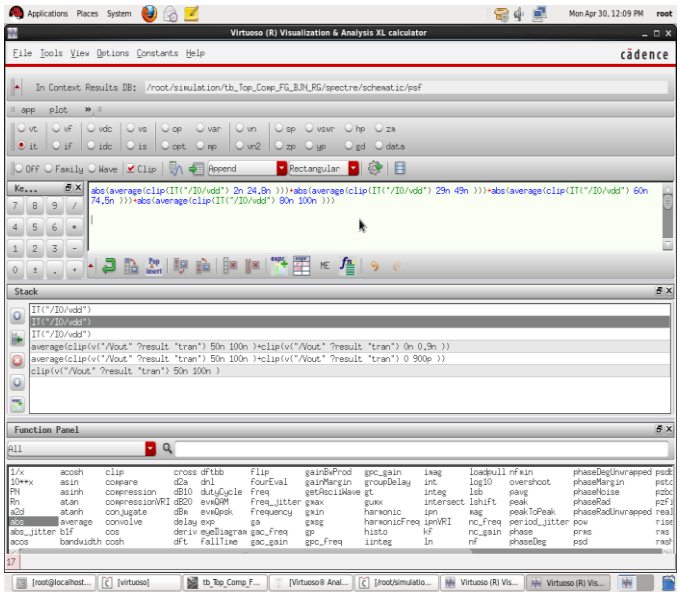

Fig. 17. Calculation of power

TABLE 1. POWER COMPARISON OF GATES DESIGNED USING REVERSIBLE AND ADIABATIC CIRCUITS

GATES	REVERSIBLE	ECRL
FEYNMAN	49.46uW	366.2nW
TOFFOLI	42.6uW	246.9nW
FREDKIN	139.6uW	72.87nW
PERES	90.88uW	514nW
TR	117uW	861.9nW
R	107.3UW	862.9nW
URG	139.9uW	820.2nW
BJN	60.4uW	718.9nW

TABLE 2. POWER COMPARISON OF COMPARATOR DESIGNED USING REVERSIBLE AND ADIABATIC CIRCUITS

COMPARATOR	REVERSIBLE	ADIABATIC
FG_PG_BJN	0.82793mW	2.072uW
FG_TG_BJN	0.805mW	2.424uW
FG_RG_BJN	0.8043mW	2.147uW
FG_URG_BJN	1.21mW	3.352uW
FG_FDK_BJN	0.33mW	4.07uW
FG_TR_BJN	0.982mW	1.917uW

VII. CONCLUSION AND FUTURE SCOPE

In this paper an optimized reversible one bit comparator is presented using adiabatic circuits. The results of simulation and evaluation of performance comparison shows that the consumption of the power in the conventional comparator is higher than the designed adiabatic one bit comparator. The design is very useful for the future computing techniques like ultra low power digital circuits and quantum computers.

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