Low Power CMOS OTA Design for Biomedical Applications

M V Sai Meena
M.Tech Scholar
Department of ECE, AVNIET,
Hyderabad.

Somashekhar Malipatil
Assistant Professor
Department of ECE, AVNIET,
Hyderabad.

D Santhosh Kumar
Assistant Professor
Department of ECE, AVNIET,
Hyderabad

Abstract – In this paper designing of MOS Transistors in two stages OTA has been done and simulated in 120nm technology. Layout has done using Microwind 2 and schematic is designed using DSCH software. A comparison has been made between scaled voltage supply and power consumption. The simulation results show that the designed two stages OTA achieves the low power consumption

Keywords– Operational transconductance amplifier (OTA), CMOS, Power consumption, 120nm Technology, Microwind 2, DSCH 2.

I. INTRODUCTION

Operational transconductance amplifier is the differential amplifier with single stage. OTA is having two high input impedance nodes. OTA is a device which converts input voltage to output current. Primarily these are called voltage to current amplifiers. It is denoted as gm. The output current is the difference between the inverting and non inverting voltages is shown in the equation 1.

$$Io=gm(V+-V-)\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 1$$

OTA are mainly used in video applications, intermediate frequency, radio frequency. Other additional applications for OTA are sample and hold, timers, multiplexers broadcast equipment and high speed data acquisition devices.

operational transconductance amplifier

In this paper the two stage transconductance amplifier is designed for lower applications like suitable for biomedical applications by using voltage scaling. In the

first stage the difference amplifier has designed as shown in fig.1.

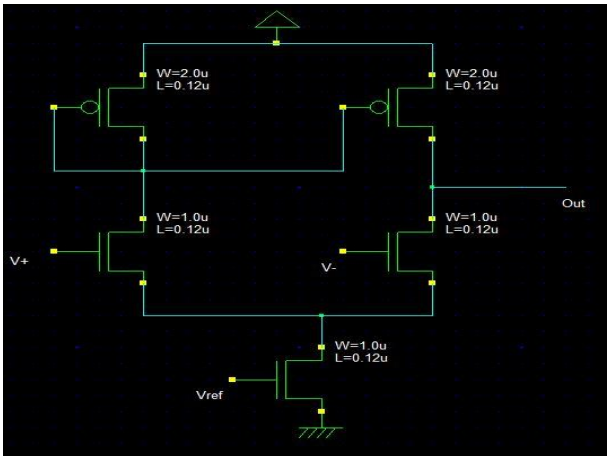


Fig.1 CMOS Differential Amplifier

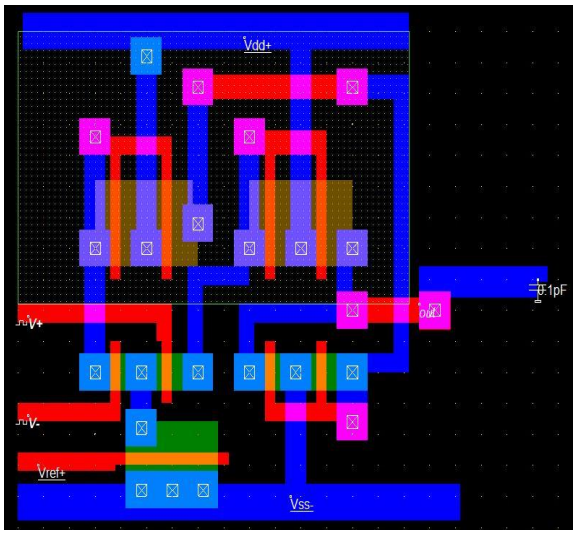


Fig 2. Differential Amplifier Layout

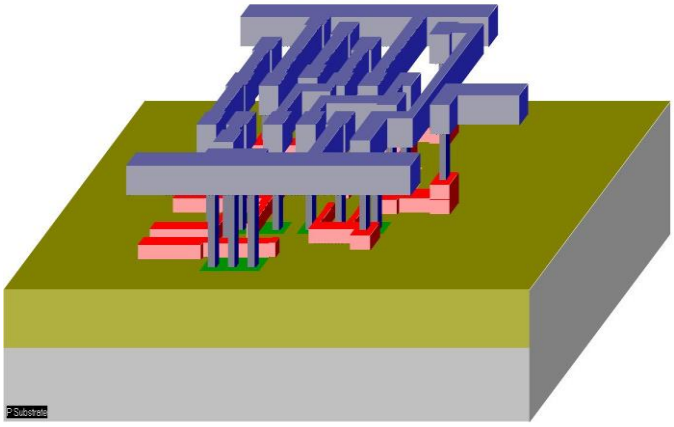


Fig 3. Differential amplifier 3D process view

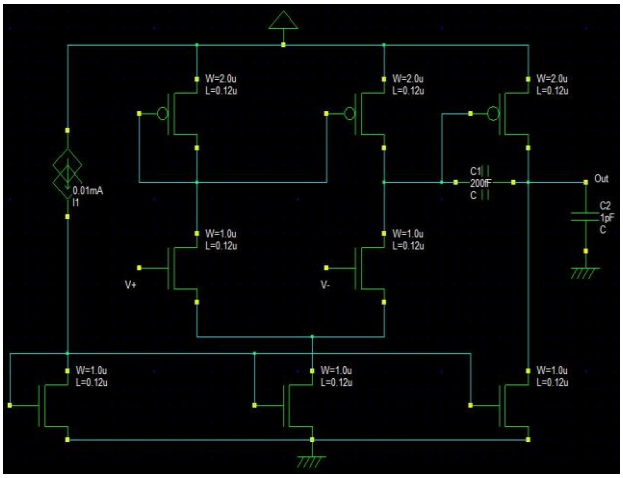


Fig 4. CMOS OTA

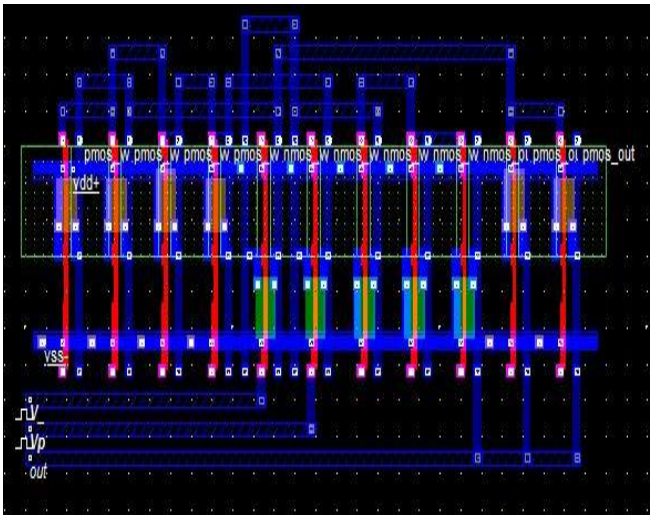


Fig 5. OTA Layout

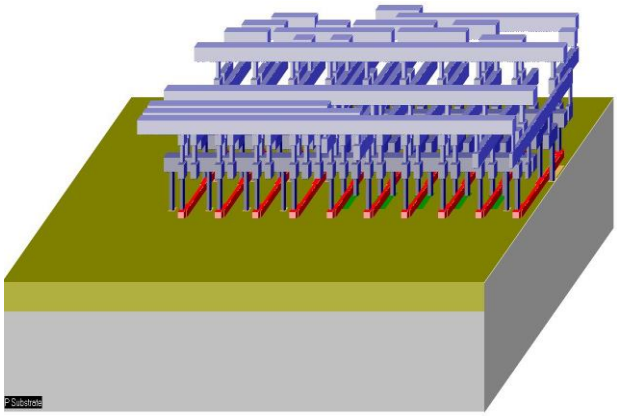


Fig 6. OTA 3D process view

In this operational transconductance amplifier supply voltage is reduced to 1.2V.

II. RESULTS

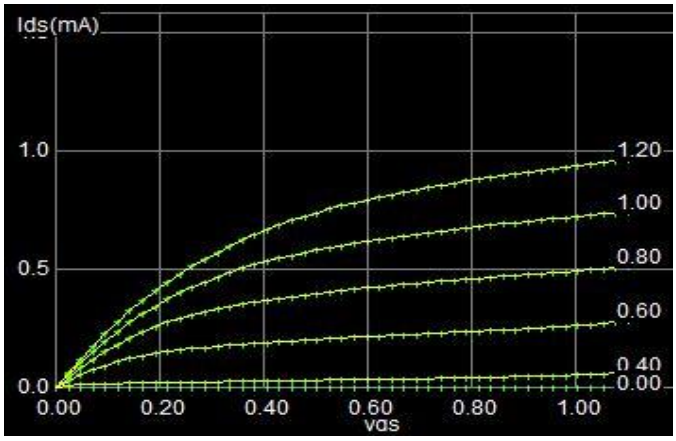


Fig 7. Ids versus Vds characteristics of OTA

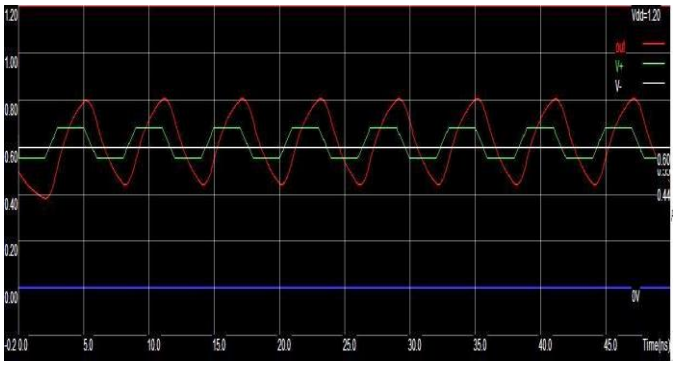


Fig 8. Voltage versus current

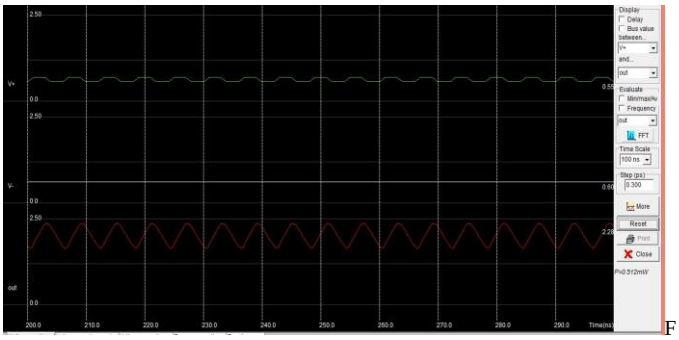


Fig 9. Amplifier simulation waveform at Vdd 2.5V

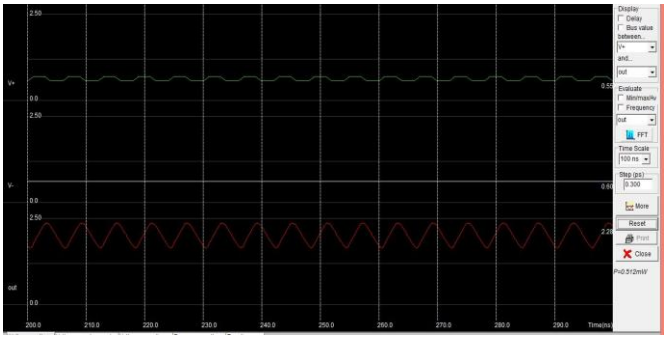


Fig 10. Amplifier simulation waveform at Vdd 1.8V

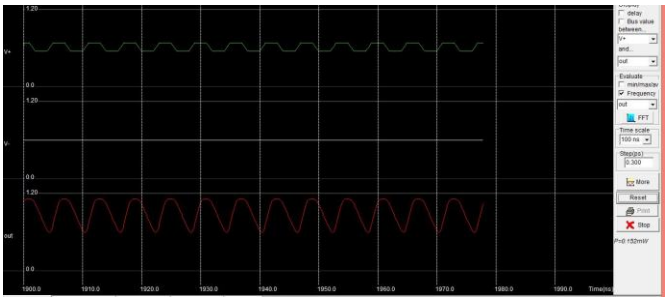
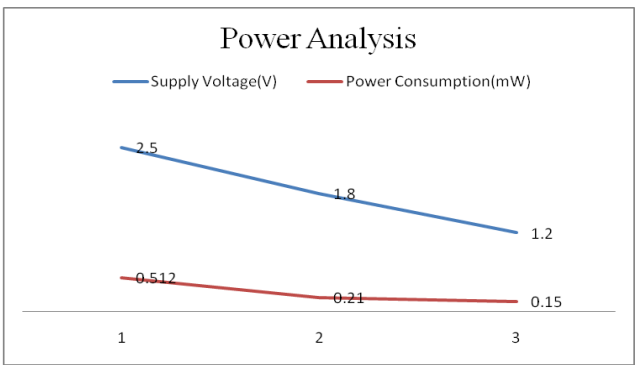


Fig 11. Amplifier simulation waveform at Vdd 1.2V

Table 1: Power analysis

Supply Voltage	Power Consumption
2.5V	0.512mW
1.8V	0.21mW
1.2V	0.15mW



Graph 1. Power analysis

III. CONCLUSION

In this design low power Operational transconductance amplifier has designed by using voltage scaling down and observed reduction in power consumption as follows when supply voltage 2.5V, 1.8v and 1.2 V applied, the power consumption is 0.512mW, 0.21mW, 0.15mW respectively.

REFERENCES

[1] Siddesh Gaonkar, Sushma P.S.,"Modeling, Design and Analysis of High CMRR Two Stage Gate Driven Operational Transconductance Amplifier using 0.18 µm CMOS Technology," International Conference on Computing for Sustainable Global Development (INDIACom) 2016.

[2] Siti Nur Syuhadah Baharudin1, Asral Bahari Jambek2 and Rizalafande Che Ismail3, "Design and Analysis of a Two-Stage OTA for Sensor Interface Circuit," 2014 IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE), April 7 - 8, 2014, Penang, Malaysia.

[3] G. Palmisano, G. Palumbo and S. Pennisi, "Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial," Analog Integrated Circuits and Signal Processing, 27, 179–189, 2001.

[4] Malipatil, Somashekhar.(2017). Review and Analysis of Glitch Reduction for Low Power VLSI Circuits. International Journal for Research in Applied Science & Engineering Technology (IJRASET) ISSN: 2321-9653.

[5] Nandyala Naveena, Nimmagadda Poojitha, Pallewar Rageshwari, Somashekhar Malipatil, "Low Power Digital Circuits Design using 120nm Technology" International Journal of Scientific & Technology Research (IJSTR), Volume 9, Issue 4, April 2020, ISSN 2277-8616.

[6] Malipatil, Mr Somashekhar, And Ashwini Patil. "Design of a Low Power Flip-flop Using MTCMOS Technique in Cadence Tool." International Journal of Ethics in Engineering & Management Education Website: www.ijeee.in (ISSN: 2348-4748, Volume 1, Issue 4, April 2014).

[7] Naveena, Nandyala, Nimmagadda Poojitha, Pallewar Rageshwari, and Somashekhar Malipatil. "Low Power & Area Efficient Digital Circuits Design for Portable Devices using GDI." Journal of Xidian University VOLUME 14, ISSUE 6, 2020, https://doi.org/10.37896/jxu14.6/212.

[8] Somashekhar, "Design of a Low Power D-Flip Flop using AVL Technique", International Journal of Advanced Research in Computer and Communication Engineering, Vol. 4, Issue 9, September 2015, DOI 10.17148/IJARCCE.2015.4962.