Low Power CMOS Full Adder Design with Sleep Transistor for Submicron VLSI Technologies

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Abstract: Any computational circuit is incomplete without the use of an adder. Addition is one of the primary operations in arithmetic circuits. These adder cells commonly aimed to reduce power consumption and delay. These studies have also investigated different approaches realizing adders using CMOS technology. The designer's concern for the level of leakage current is mainly aimed at minimizing power dissipation. For portable electronic devices this equates to maximizing battery life. When a mobile phone is in standby mode, certain portions of the circuitry are shut down. Even though de-activated, these circuits have some leakage current flowing through them. Even if the leakage current is much smaller than the normal operating current of the circuit, it depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. In this project leakage power and the ground bounce noise is considerably reduced by the use of sleep transistor in full adder design. Size of the sleep transistor is determined by transistor resizing approach. 4 bit adder is implemented using 1 bit adder as reference. The simulation shows that, the 1 bit and 4 bit adders are efficient in terms of standby leakage power, active power and ground bounce noise. Simulations have been performed by using 130 nm CMOS. Electric Tool is used to design the schematic and layout level diagrams of our project. The LT-SPICE Tool will be used for simulation of the Spice code which tests the functionality of our generated layout and schematic blocks.

Keywords: Low leakage power, Ground Bounce, Sleep transistor, adder cell.

I. INTRODUCTION

Any computational circuit is incomplete without the use of an adder. Addition is one of the primary operation in arithmetic circuits [1], [2]. These adder cells commonly aimed to reduce power consumption and delay. These studies have also investigated different approaches realizing adders using CMOS technology [3], [4]. The designer's concern for the level of leakage current is mainly aimed at minimizing power dissipation. For portable electronic devices this equates to maximizing battery life. For example, mobile phones need to be powered for extended periods (known as standby mode, during which the phone is able to receive an incoming call), but are fully active for much shorter periods (known as talk or active mode, while making a call). When a mobile phone is in standby mode, certain portions of the circuitry are shut down. Even though de-activated, these circuits have some leakage current flowing through them. Even if the leakage current is much smaller than the normal operating current of the circuit, it depletes the

battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate [5], [6]. In addition to the sub threshold leakage current, gate tunneling current also increases due to the scaling of gate oxide thickness. Each new technology generations results nearly a 30xincrease in gate leakage [7], [8]. There are several techniques to reduce leakage power. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground) [8]. This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance [9], [10] and further reduction of peak of ground bounce noise is possible with used novel technique.

II. FULL ADDER CIRCUITS

Static logic style gives robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Multiplexers and XOR based circuits are advantageous in pass transistor logic [4]. On the other hand, dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability [4]. The conventional CMOS 28 transistor adder [7], as shown in Figure 1, is considered as Base case throughout this paper. All comparisons are done with Base case. Transistor sizes are specified as a ratio of Width/Length (W/L). It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter. This ratio proves inefficient in when simulated below 90nm process. Hence, the gate resized adder circuits are used as shown in Figure 1, 2, 3. Further, power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. The smallest transistor considered for 90nm technology has a width of 120nm and a length of 100nm and for 65nm technology has a width of 78nm and a length of 65nm which gives WIL ratio of 1.2. The WIL ratio of NMOS is fixed at 1.2 and WIL of PMOS is 3.8 which is 3.1 times that of NMOS in Design1 (Figure 2). The sizing of each block is based on the following assumption. These sizing will reduce the standby leakage current greatly because sub-threshold current is directly proportional to the Width/Length ratio of transistor. On the other hand, these reduced sizes reduce the area occupied by the circuit. This will reduce the silicon chip area and in turn reduction in the cost.

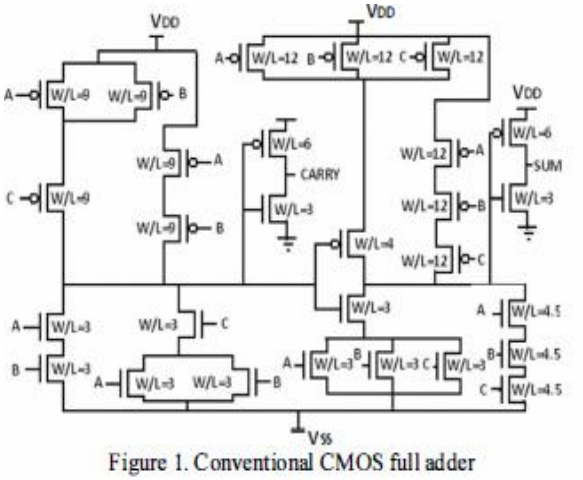


Figure 1. Conventional CMOS full adder

Modified adder circuit of Design 2 shown in Figure 3, the W /L ratio of PMOS is 1.5 times that of W /L ratio

of NMOS and each block has been treated as an equivalent inverter. The goal of this design is to reduce the standby leakage power. Further compared to the Base case, Design 1 and Design 2, ground bounce noise produced when a circuit is connected to sleep transistor is reduced.

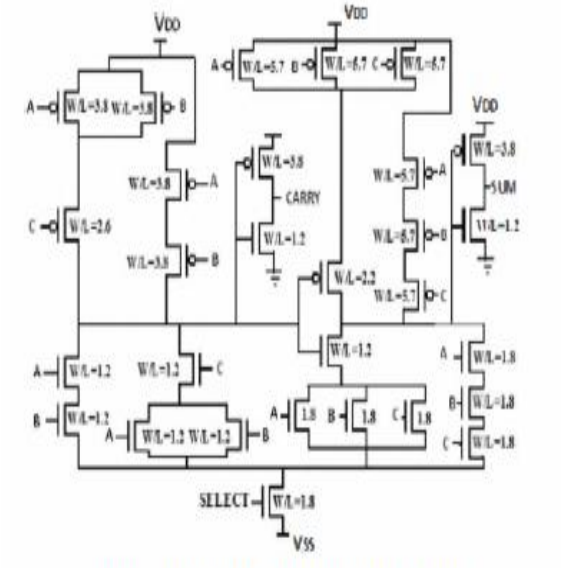
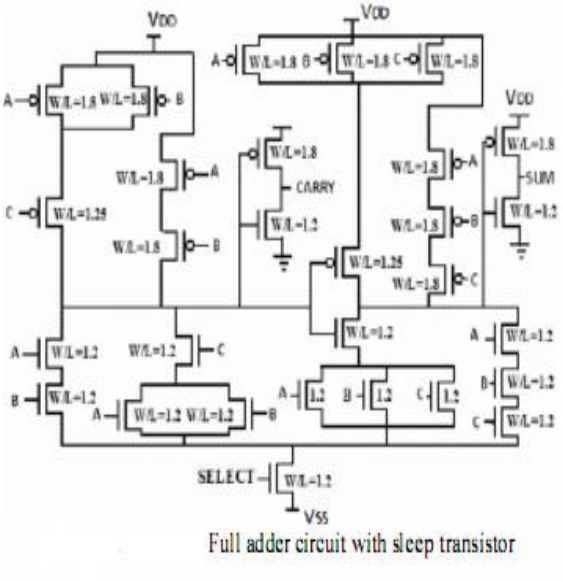


Figure 2. Full adder (Design1) circuit with sleep transistor



Full adder circuit with sleep transistor

III. PERFORMANCE ANALYSIS.

Simulations have been performed in T-Spice and the technology being employed is 130nm with a supply voltage of 5v for power analysis of 1 bit and 4 bit adders and a supply of 5v and 3.3v for ground bounce noise analysis.

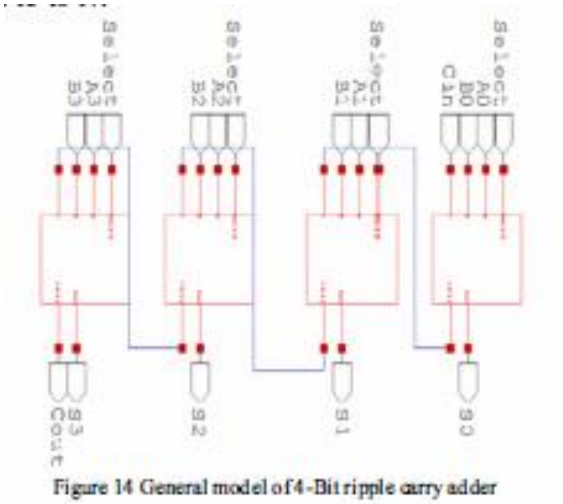


Figure 14 General model of 4-Bit ripple carry adder

A. Active Power

Power dissipated by the circuit when the circuit is in active state is termed as Active power. Input vectors are fed into the circuit and the average power dissipation is measured. Here, considered simulation time for active power is 50ns. Almost all of the input combinations are considered for simulation. Same input vector combinations have been given to the all three designs- Base case, Design 1 and Design2, and a comparison has been made for the 130nm technology.

B. Standby leakage power

Standby leakage power is measured when the circuit is in standby mode. Sleep transistor is connected to the pull down network of 1 bit full adder circuit. Sleep transistor is off by asserting an input 0v. Size of a sleep transistor is equal to the size of largest transistor in the network (pull up or pull- down) connected to the sleep transistor. The sleep transistor size in Design 1 and Design2 is reduced due to the resizing of the adder cells in proposed circuit.

Standby leakage power is measured by giving different input combinations to the circuit. Standby leakage is greatly reduced in both Design 1 and Design2 and for 130nm.

C. Improved Ground bounce noise reduction

Figure shows the design for peak of ground bounce noise reduction in mode transition [10]. All three designs, Base case, Design 1, Design2 are considered to apply the proposed noise reduction technique.

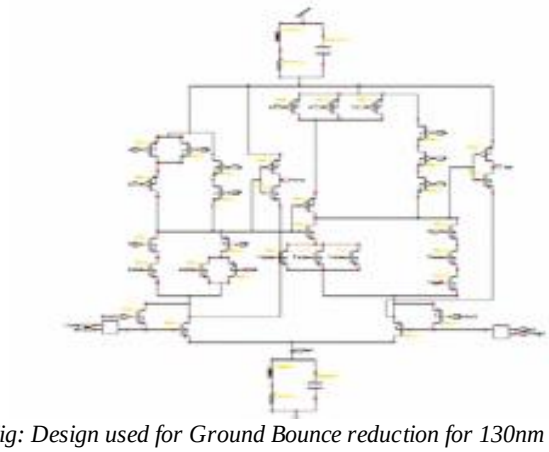
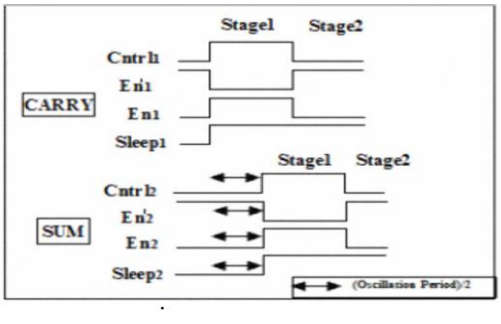


Fig: Design used for Ground Bounce reduction for 130nm

One bit full adder is divided into two separate but cascaded blocks. The first is the carry generation block and the following is the sum generation block. Separate sleep transistors are added at the bottom of the blocks. The proposed technique works as follows. The applied signals are shown in this Figure.

For carry part, during stage1 transmission gate is off by giving proper enable signals and at the same time control transistor is turned on to make the sleep transistor working as a diode.



The stored charge in carry generation block is discharged through sleep transistor.

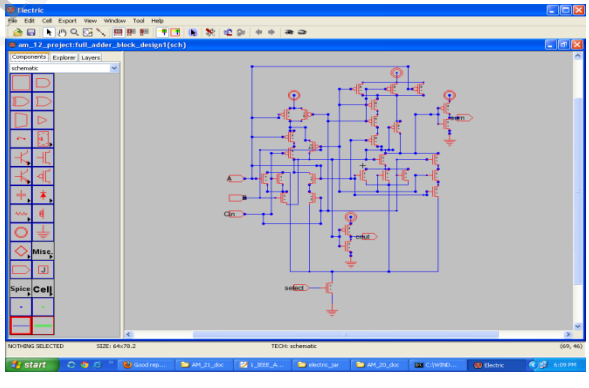
Same signals are applied to sum generation part also but with duration of half of the oscillation period. As a result, noise cancellation occurs once the second sleep transistor (ST2) turns on due to phase shift between the noise induced by the second sleep transistor and hence the reduction in peak of the ground bounce noise as shown.

IV.EXPERIMENTAL RESULTS

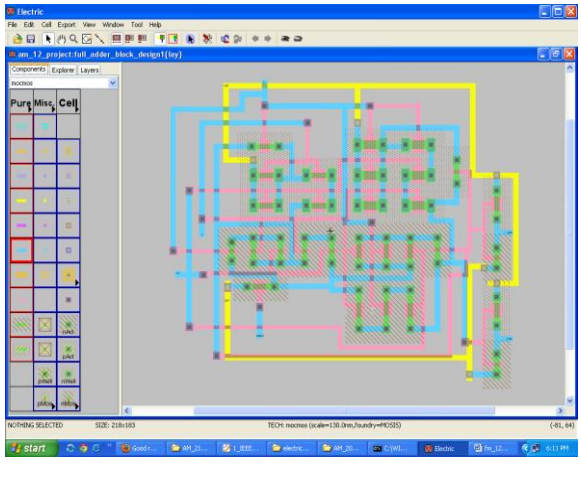
The experimental results were observed using Electric Tool and LT-Spice Tool. Electric Tool was used to design the schematic and the layout level of the full-adder circuits for all the three designs.

LT-Spice Tool is used to simulate the SPICE deck which is produced form the designs.

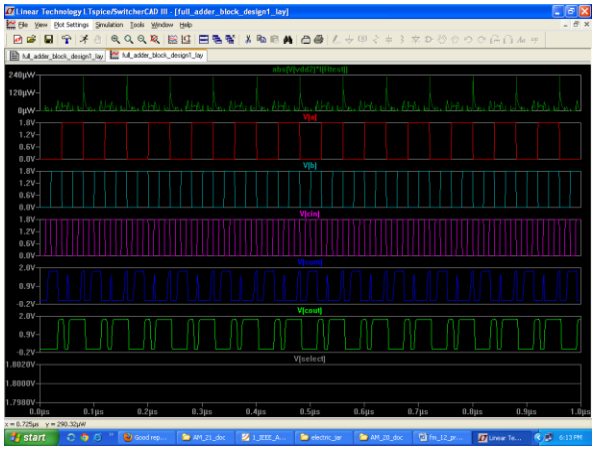
Result snapshots for Design1:



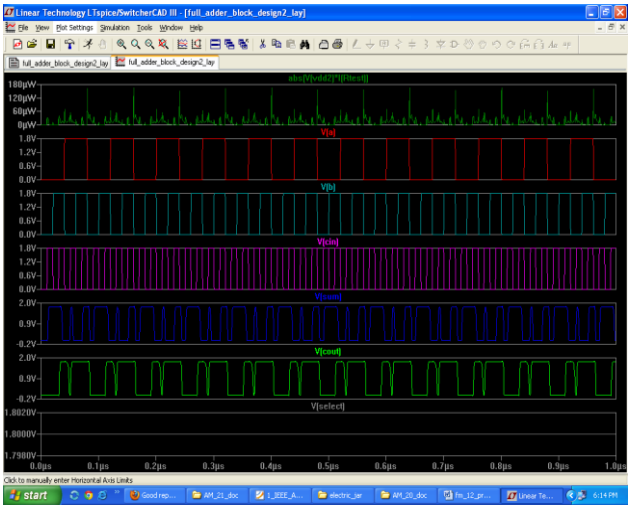
Schematic for Design1



Layout for Design1

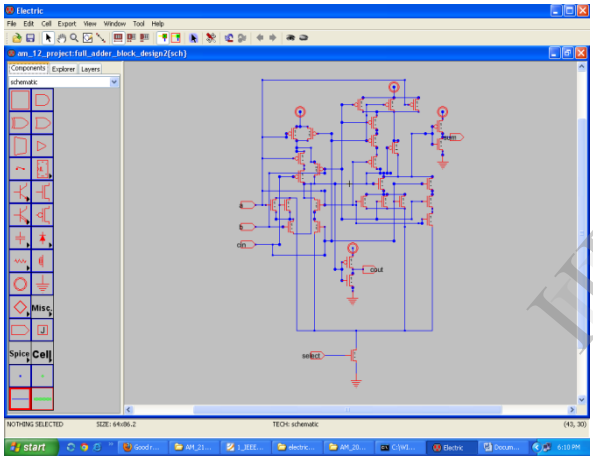


Layout results for Design1

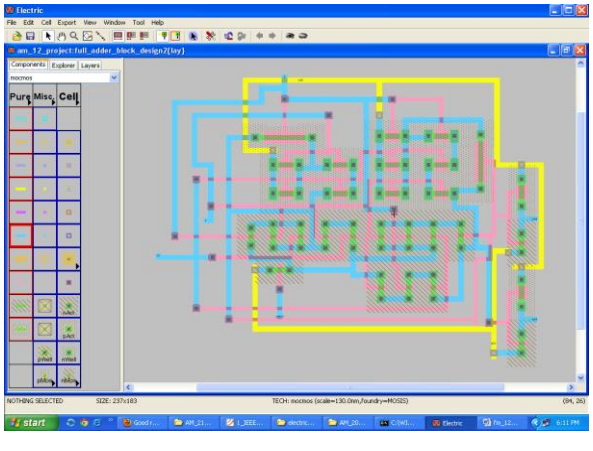


Layout results for Design2

Similarly for Design2:



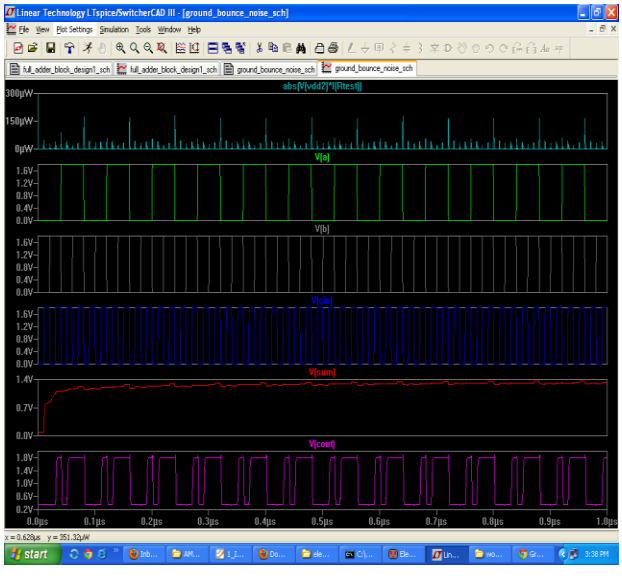
Schematic for Design2



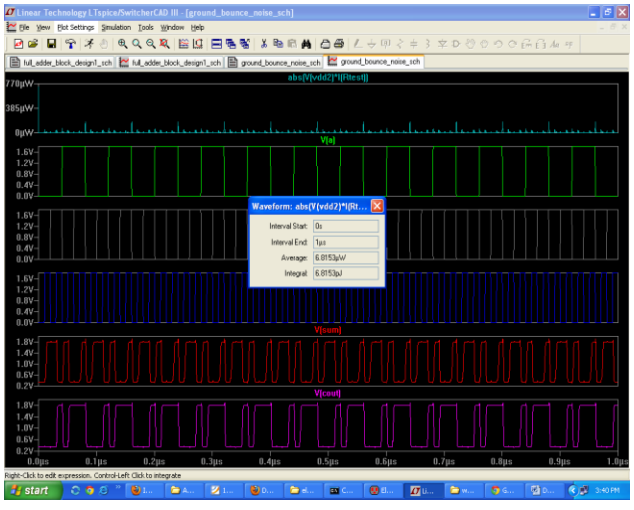
Layout for Design2

As per the ground bounce noise after doing this operation we can reduce some noise levels as well as the power it is nearly 1.2uwatts of power.

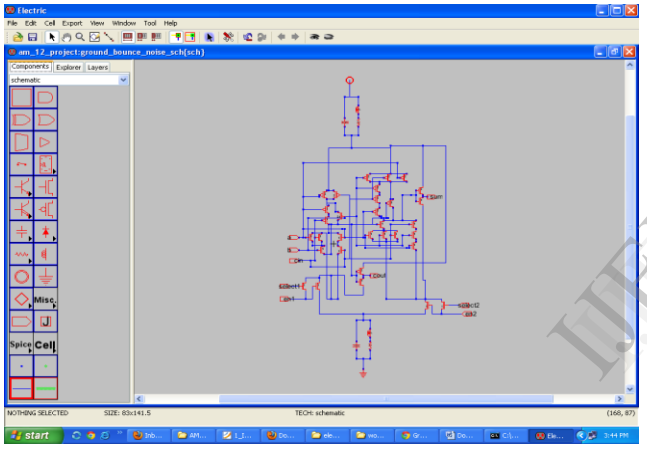
Ground bounce noise for design 1 when select1 signal is 0v,then the output becomes as below.



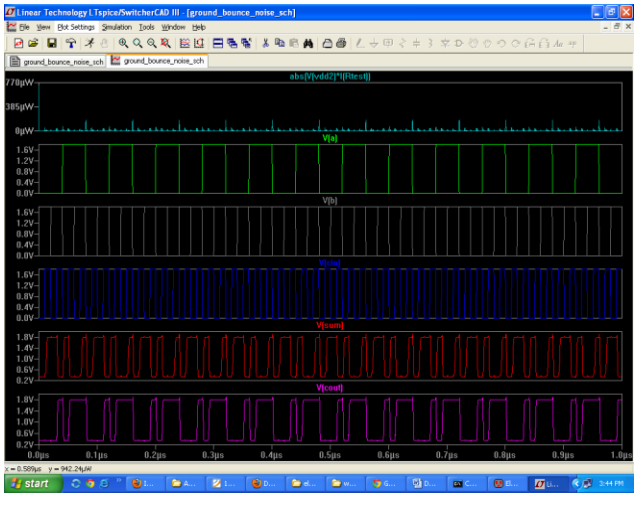
And the power has reduced to 6.815uwatts, as compared to the design 1 with ground bounce technique is 7.89uwatts



Schematic of the design 1 for the ground bounce technique



And the waveforms of the above circuit



V. CONCLUSION

In this paper, ground bounce noise and leakage power are analyzed for conventional and modified 1 bit adder circuits, in 130nm technology. 4-bit full adder is designed based on the I-bit adder and the adders are analyzed for active and standby power in 130nm technology. Standby power or leakage power of Designl and Design2 is reduced by almost 70% and 80% than the conventional design, respectively. Active power dissipation is reduced by almost 45% and 60% by using Designl and Design2 respectively. Ground bounce noise is reduced by about 25% and 45% with designl and Design2 respectively, compared to conventional design. Ground bounce has been analyzed for 5v and 3.3v supply voltage. By the use of power gating technique, specifically the sleep transistor, and by transistor resizing, power dissipation and ground bounce noise is minimized considerably.

VI.REFERENCES

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