Low Power Cache Design Using 7T SRAM Cell

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ABSTRACT

Sram represents a large portion of the chip,and It is expected to increase in the future in both portable devices and high-performance processors. Charging/discharging large bit lines capacitance represents a large portion of power consumption during a write operation. Therefore,the proposed 7TSRAM Cell reduces the power consumption performed in write operation. Experimental results using HSPICE simulation shows that read delay and static noise margin are maintained after carefully sizing the cell transistors.

Keywords — SRAM cell, Low power, SNM.

1. INTRODUCTION

Cache,An area of high-speed computer for the temporary storage of frequently used data.SRAM is used in the cache memory of processors because of its high speed and the low power consumption.SRAM does not need to be refreshed as the transistors inside would continue to hold the data as long as the power is not cut off.This behavior leads to a few advantages,not least of which is the much faster speed that data can be written and read.The word "static"indicates that the memory retains its contents as long as power remains applied. On-chip cache consumes a large percentage of bthe whole chip area and expected to increase in advanced technologies.Bit lines,word lines,data lines are the largest capacitive parts in the memory.Low-power SRAM design techniques [2]—[3] are mainly based on reducing the capacitance and voltage swing level.

2 .CONVENTIONAL 6T SRAM CELL

A conventional 6T SRAM cell,shown in Fig 1,consists of two inverters,inv1 and inv2,connected back-to-back and two nMOS pass transistors that are used to access the cell for read or write.For stable write operation,setting one of the bit lines to "0" and the other to "1" is necessary.Careful transistor sizing is also required to ensure a stable read and write operations [4].

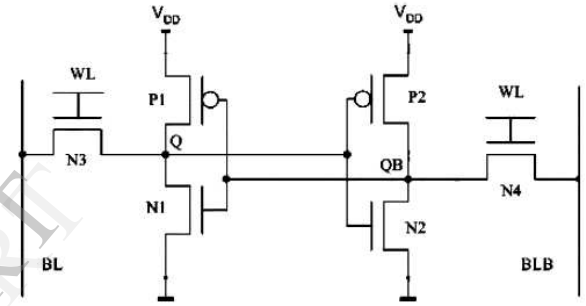

Fig 1. Conventional 6T SRAM cell.

3. PROPOSED 7T SRAM CELL

1) The proposed 7T SRAM cell is proposed to reduce the power consumption write operation.

2) The optimal cell transistor sizes for stable read/write operation and to maintain read/write delay and static noise margin are determined.

3) Evaluate the following characteristics for SRAM using the proposed cell: performance of read/write delay,power consumption, area, and static noise margin.

All the results were obtained in a 180nm CMOS technology at room temperature using HSPICE for 1.8-V supply voltage.The salient feature of the scheme is an additional nMOS connected to the source of driver nMOS transistors of the memory cell,which enables small swing of bit lines in a write operation.The precharge level must not be Vdd because access transistors of the cell cannot turn on in the write operation.There is no additional power consumption even if the write and read cycles come alternately,because there is no mismatch between the voltage level of bit lines in read cycles and that in write cycles.

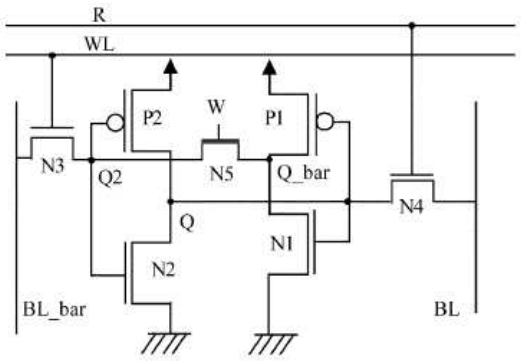

Fig 2.Proposed 7T SRAM cell

The proposed 7T SRAM cell depends on cutting off the feedback connection between the two inverters,inv1 and inv2,before a write operation.The feedback connection and disconnection is performed through an extra nMOS transistor N5 and the cell only depend on BL_bar to perform a write operation.

3.1 WRITE OPERATION

The write operation starts by turning N5 off to cut off the feedback connection.BL_bar carries complement of the input data,N3 is turned on,while N4 is kept off as shown in Fig .3. The 7T SRAM cell having two cascaded inverters,inv2 followed by inv1.N3 transistor transfers the data from BL_bar to Q2 which drives inv2,P2 and N2 to develop Q ,the cell data. Similarly, Q drives inv1,P1,N1,to develop Q_bar which equals Q2 if data is ‘”0” and slightly higher than Q2 if data is”1”.Then WL is turned off and N5is turned on to reconnect the feedback link between the two inverters to stably store the new data.

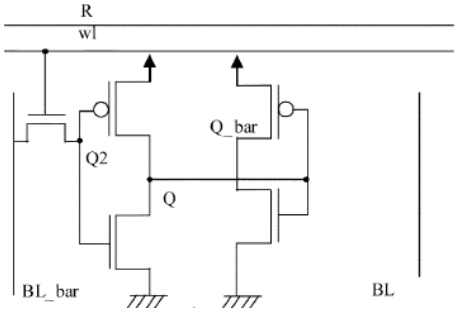

Fig. 3. Proposed 7T SRAM cell during a write operation.

Both BL and BL_bar are precharged “high”.Using the proposed write scheme,BL_bar is kept “high” to write “0” with negligible power consumption and careful transistor sizing is essential to guarantee a stable write “0”operation .

To store “1” in the cell,BL_bar is discharged to”0” with comparable power consumption to the conventional 6T cell.To store a”0” in the cell,there is no need to discharge BL_bar .

3.2 READ OPERATION

Both WL and R signals are turned on, while N5 is kept on. When Q=”0”,the read path consists of N2 and N4 as show in Fig.4(a),and the behaves like a conventional 6T cell. When Q=”1”,the read path consists of N1,N5 and N3,which represents a critical read path as shown in Fig.4(b).In this critical side, the three transistors are connected in series which reduces the driving capability of the cell unless these transistors are carefully sized.

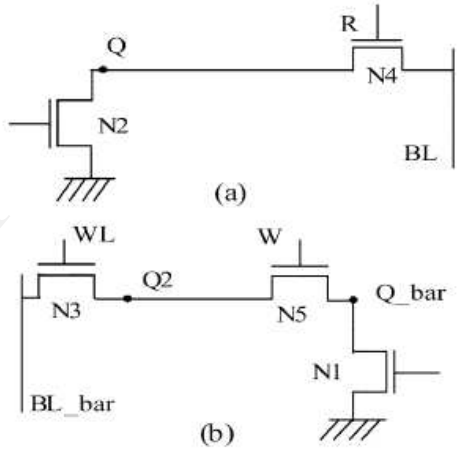

Fig.4 a) Read path when(a) Q=”0” and (b) Q=”1”.

3.3 TRANSISTOR SIZING

When WL is activated,N3 easily transfers a perfect “0” to Q2 which drives Q”1”.Storing “1” starts with discharging BL_bar to 0V and turning N5 off.Both Q2 and Q_bar are “0” with no voltage difference between them.Writing “1” is a stable operation because nMOS transistor is aperfect switch when passing a “0”.On the other hand,writing “0” starts with keeping BL_bar “high” at Vdd and turning N5off.Ater turning WL off and W on ,the cell ends up with Q=”0”,Q_bar =”1”,and Q2 <”1”.For P2=1 and N2≥2,thw switching voltage $V_{M2} \leq 0.7$ V and it is small enough to ensure that Q has a strong “0” and inv2 has $NM_H \geq$ 0.7V.Waveforms for two consecutive write operation shown in Fig.5.

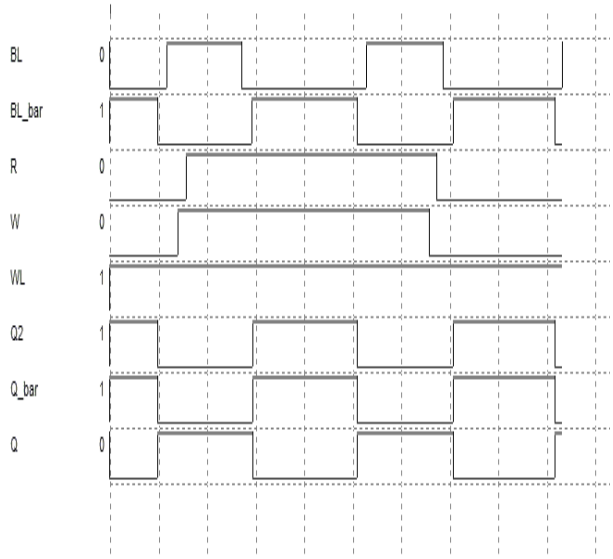

Fig.5 Output waveforms for two consecutive write operation.

4. EXPERIMENTAL RESULTS

4.1 READ AND WRITE DELAY

Read delay defined as the time delay between 50% WL activation to when the sense amplifier has reached 90% of its full swing. Because of the asymmetry of the proposed 7T cell,the read path when Q="1" shown in Fig.4(b).The read delay of the critical read delay path at different transistor sizes as shown in Fig.6..The write delay is approximately equals the propagation delay of inv2 and inv1.

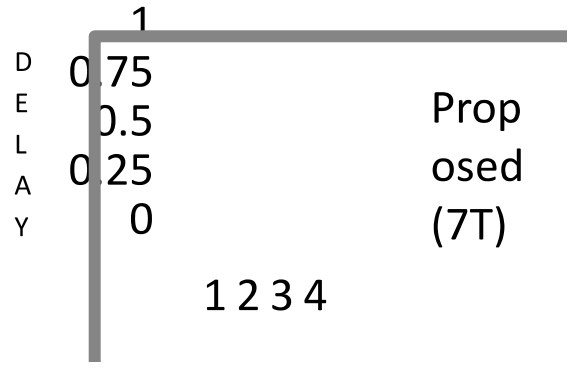

Fig.6. Read delay as a function of N5 width

4.2 STATIC NOISE MARGIN (SNM)

There are two measurements metrics for cell stability:read stability and static noise margin (SNM).The SNM is defined as the maximum dc noise voltage required to flip cell data[ ].Because the proposed 7T SRAM cell has two asymmetrical read path as shown in Fig.4,its butterfly curve has asymmetric lobes which depend on the cell transistor sizes.The SNM consists of two switching curves, vertical and horizontal. The vertical curve depends on the sizes of N2, P2,and N4.The horizontal curve depends on N1,P1,N3,and N5. Table I summarizes the SNM during read operation. Simulation of SNM for read and write operation is shown in Fig.7(a) and Fig 7(b).

TABLE I

SNM READ OPERATION	CONVENTIONAL 6TSRAM CELL mV	PROPOSED 7TSRAM CELL mV	TECHNOLOGY USED
1	148	149	180nm
2	154	155	180nm
3	159	158	180nm

The cell SNM increases with N1,N5 and decreases with N2,N3. Table II determines the SNM during write operation.

TABLE II

SNM WRITE OPERATION	CONVENTIONAL 6T SRAM CELL mV	PROPOSED 7T SRAM CELL mV	TECHNOLOGY USED
1	143	144	180nm
2	145	145	180nm
3	140	142	180nm

HSPICE Simulation of SNM for proposed 7T SRAM cell is shown in the Fig.7.

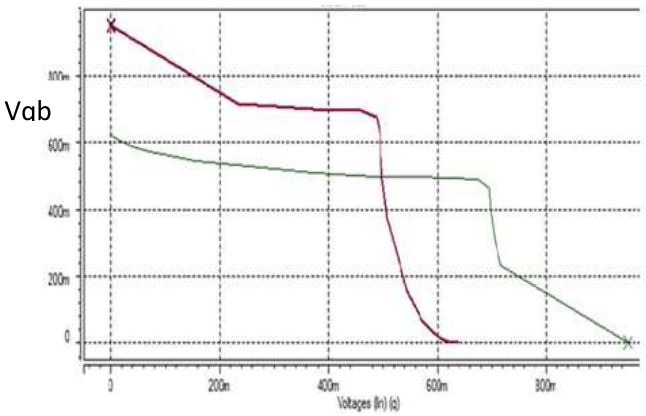

Fig.7. SNM for proposed 7T SRAM cell.

4.3 POWER CONSUMPTION

TABLE .III FOR DIFFERENT INPUT PATTERNS

WRITE PATTERN	CONVENTIONAL 6TSRAM CELL W	PROPOSED 7TSRAM CELL W
0 to 0	4.6072E-06	4.6516E-06
0 to 1	4.6516E-06	4.9985E-06
1 to 0	4.6536E-06	4.6089E-06
1 to 1	4.6062E-06	4.6513E-06

Using the optimal transistors sizes mentioned aboveinput data patterns are adjusted to measure the write power consumption for different input data and HSPICE results are summarized in Table II.

5. CONCLUSION

The design metrics for the Seven-transistor cell are discussed in detail and performance and stability are evaluated. Finally, a comparison is done between existing six-transistor technology and the proposed (seven-transistor) technology.The comparison includes SNM powe and delay. The proposed 7T SRAM cell which exploits the fact by keeping the bit lines "high" to write "0".With careful transistor sizing, the 7T SRAM cell maintains the read/write delay and the SNM.The reduced power, delay, SNM analysis done in HSPICE simulation shows that it can be used in low power cache design.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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