Low Power Area Efficient CMOS Differential Logic Adder With Delay Reduction

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***Abstract*—In this paper, a set of CMOS differential logic circuits are introduced for use in low-power application. Power dissipation is one of the most important design objectives in integrated circuits, after speed. As adders are the most widely used components in such circuits, a new BEC based CSLA adder has been proposed which performs fast addition, while maintaining low power consumption, delay and less area. The comparison results indicate that the BEC based CSLA adder with the proposed logic family offers nearly 77% power reduction, nearly 90% less delay and nearly 62% less area, compared with that of the conventional logic. This work mainly focuses on implementing the 64 bit BCDL adder. The proposed design has been developed using VHDL and results synthesized in Xilinx ISE.**

Keywords— CSLA, Low power, Area efficient, Voltage Boosting, BCDL, BEC,DCVS.

I. INTRODUCTION

The requirement of low power consumption in modern portable devices like Mobile phones and portable PCs are increased today. The major problem in these devices is their power consumption. So the trends in the reduction of power consumption are developed. One way to reduce the power consumption is lower the supply voltage. The previous chip designs are developed with 5V is the input and referred as 'logic 1'. Nowadays this 5V is reduced to minimum 1.2-2V range. In the extreme case, circuits can be made to be operated in the subthreshold region for maximum energy efficiency.

The approach only used in low end-design because it is limited where speed is a secondary concern, because of severe speed degradation due to temperature and threshold voltage variations. For medium- and high end designs, where speed performance and energy efficiency are both important. As the supply voltage scales down toward the threshold voltage, the speed performance is still degraded of conventional CMOS circuits, such as static CMOS logic, differential cascode voltage switch (DCVS) logic [5] [see Fig. 1(a)], and domino CMOS logic [see Fig. 1(b)] due to the reduced overdrive voltage (Vgs − Vth) of transistors.

CMOS bootstrapped dynamic logic (BDL) [8] [see Fig. 1(c)] was proposed, for fast logic operation at low supply voltage. To overcome the aforementioned problem, a bootstrapped CMOS large capacitive-load driver [7] was proposed. The switching speed is to improve low supply voltage by allowing the voltage of some internal nodes. A novel boosting CMOS differential logic style is proposed in this brief. Section II describes the Binary to Excess 1 converter operation of the proposed logic style. In Section III, Circuit structure and operation Section IV describes the simulation comparison of the proposed logic style.

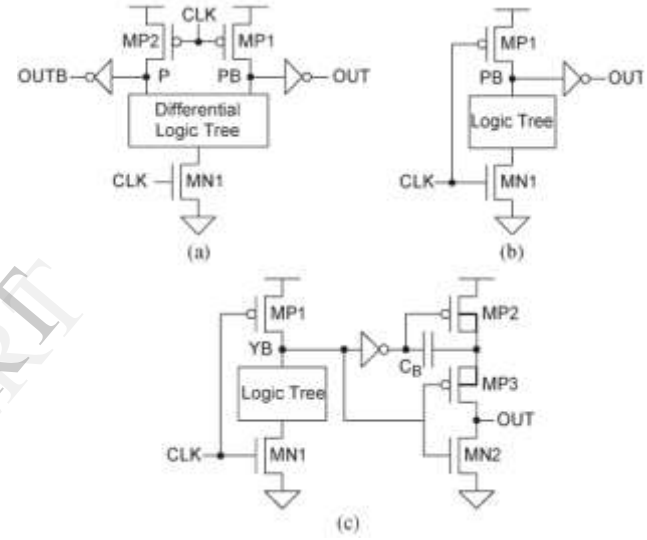


Fig. 1. Conventional digital CMOS circuits. (a) DCVS. (b) Domino CMOS logic. (c) BDL.

Section V describes the experimental result for 64-bit adders as a design example to prove the practicality of the proposed logic style. Finally, we present the conclusion in Section VI.

Now a day our computers speed is fast high in terms of GHz. So conceptually we need to improve the speed for the given design by decreasing several numbers of stage or gates. The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with in the regular CSLA to achieve lower area and power consumptions [1],[2],[6],[7]. the CSLA needs more area because of using multiples of Ripple Carry Adder for generating sum and carry on the dependency of carry input Cin=0 and Cin=1[5]. Then the final results of sum and carry are selected by the multiplexers from bit to bit going to increase. Finally reliable results at the output will depend upon the number of stages.

II. BEC

As stated above the main idea of this work is to use BEC instead of the RCA with C = 1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit

RCA, an n+1 bit BEC is required. A structure of a 4-bit Binary to Excess-1 converter is shown in Fig. 2.

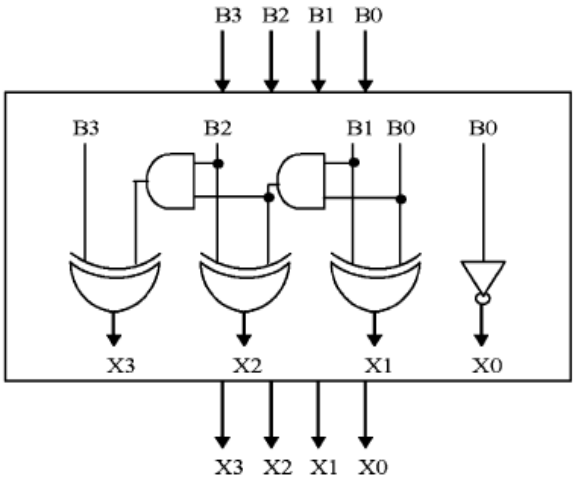


Fig. 2. 4-bit BEC

The basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux [see Fig. 3] gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output [1]. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols NOT, & AND, XOR)

X0 = ~B0

X1 = B0 ^ B1

X2 = B2 ^ (B0 & B1)

X3 = B3 ^ (B0 & B1 & B2)

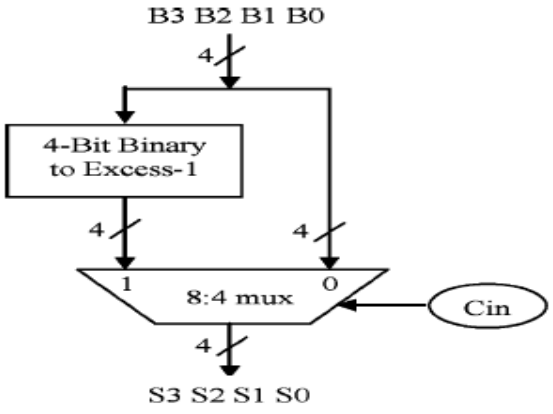


Fig. 3. 4-bit BEC with 8:4 Mux

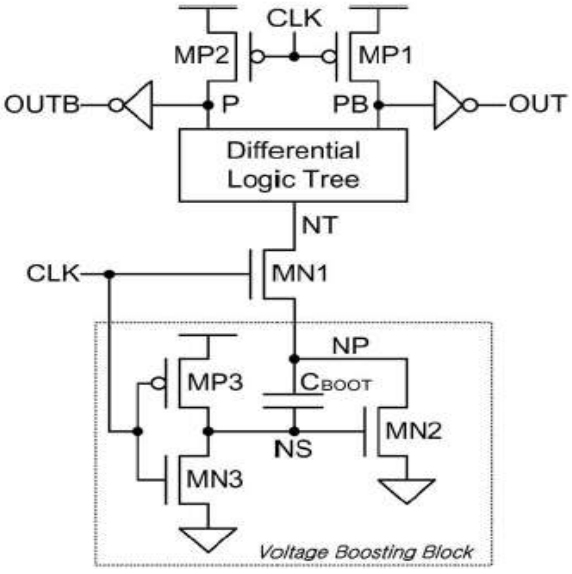
Table .1.Function Table of the 4-bit BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

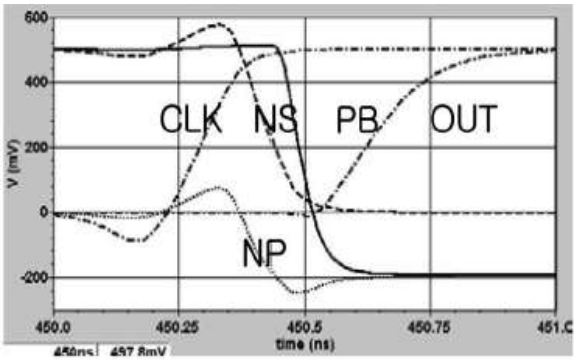
III. CIRCUIT STRUCTURE AND OPERATION

Fig. 4(a) shows a generic structure of the proposed boosted CMOS differential logic (BCDL). It consists of a voltage-boosting block and a precharged differential logic block. The precharged differential logic block, which is composed of a differential logic tree with bottom transistor MN1, precharge transistors MP1 and MP2, and output inverters, receives the boosted voltage at NP and swiftly evaluates the output logic values. The voltage-boosting block, which is shown in the dotted box at the lower part of the circuit, is composed of transistors MN2, MN3, and MP3 and boosting capacitor CBOOT and is used to boost the voltage of NP below the ground.

Let us explain the operation of BCDL. It has two phases of operation, namely, a boosted evaluation phase and a precharge phase. The circuit is in the boosted evaluation when CLK is High, MN1 turns on and connects the differential logic tree to the voltage-boosting block.at the same time, NS is pulled down toward the ground, allowing NP and NT to be boosted below the ground by capacitive coupling through CBOOT. As shown in Fig. 4(b).When CLK changes to Low, the circuit goes into the Pre charged phase. During this phase MN1 is fully off. Precharge nodes P and PB in the differential logic block are then precharged to the supply voltage by MP1 and MP2, letting outputs OUT and OUTB identically low.



(a)



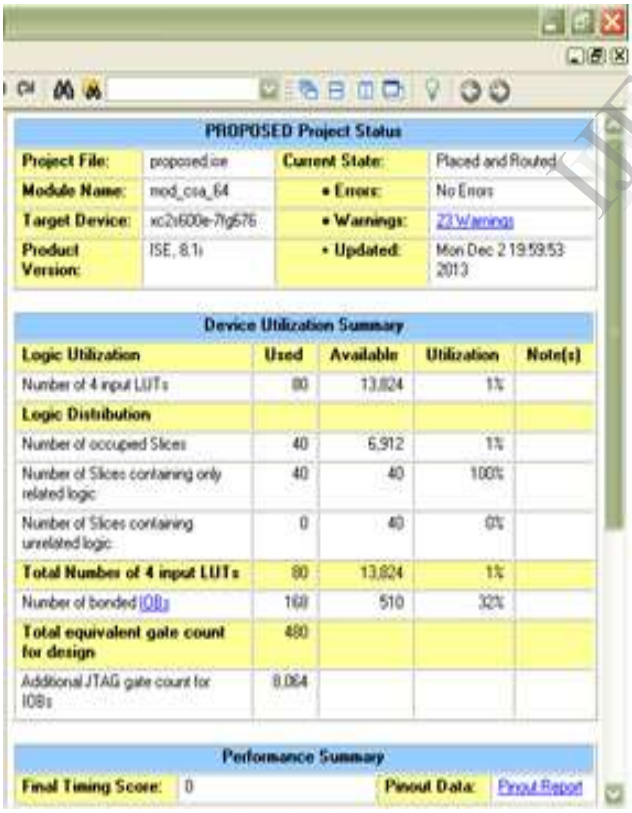
(b)

Fig. 4. Proposed BCDL. (a) structure. (b) operation.

At the same time, transistors MP3 and MN2 in the voltage-boosting block turn on, allowing NS and NP to be high and low. When the supply voltage is applied across CBOOT a voltage is identical.

IV. SIMULATION COMPARISON

The Proposed BEC with CSLA system results are analyzed by Area, Delay and Power. In Fig .5 shows the Area analysis of proposed BEC with CSLA. The Area should be analyzed by total number of Gate count used in the System.



PROPOSED Project Status

Project File:	proposed.ise	Current State:	Placed and Routed
Module Name:	mod_csa_64	• Errors:	No Errors
Target Device:	xc2v600e-7fg676	• Warnings:	23 Warnings
Product Version:	ISE, 8.1i	• Updated:	Mon Dec 2 19:59:53 2013

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	80	13,824	1%	
Logic Distribution				
Number of occupied Slices	40	6,912	1%	
Number of Slices containing only related logic	40	40	100%	
Number of Slices containing unrelated logic	0	40	0%	
Total Number of 4 input LUTs	80	13,824	1%	
Number of bonded IOBs	169	510	32%	
Total equivalent gate count for design	480			
Additional JTAG gate count for IOBs	8,064			

Performance Summary

Final Timing Score:	0	Pinout Data:	Pinout Report

Fig. 5. Area Analysis

Then the Delay is analyzed by the synthesis report. As shown in Fig .6.

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Timing Summary:
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Speed Grade: -7

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 10.765ns

Timing Detail:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 304 / 56
-------------------------------------------------------------------------
Delay:               10.765ns (Levels of Logic = 5)
  Source:            a<59> (PAD)
  Destination:       s1<63> (PAD)

  Data Path: a<59> to s1<63>
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   0.769    1.188  a_59_IBUF (a_59_IBUF)
     LUT4:I1->O            2   0.418    1.035  u1/u1/f41/f1/carry1 (u1/u1/f41/c1)
     LUT3:I1->O            2   0.418    1.035  u1/u1/f41/f2/carry1 (u1/u1/f41/c2)
     MUXF5:S->O            1   0.648    0.828  u1/u1/f41/f4/Mxor sum xo<1>1 f5 (s1 63 OBUF)
```

Fig. 6. Delay Analysis

The ISE software to generate a detailed Power Report that contains the following information Estimated total power consumption, Estimated power consumption on each supply rail, Device junction temperature, Power analysis are shown in Fig .7.

Fig. 7. Power Analysis

The output result comparison of existing system BCDL and proposed system BEC with CSLA as shown in Table .2.

Table .2. Results Comparison

System	Area	Delay(ns)	Power(mw)
Conventional (BCDL)	774	100.032	72
Proposed (BEC-BCDL)	480	10.535	56

Comparison results indicated in the Table that the area of the Proposed BEC with CSLA system was improved by up to 62%, then delay is reduced up to 90% and power is reduced up to 77% compared with conventional BCDL System.

V. EXPERIMENTAL RESULT

The structure of the 8-bit ripple carries chain used in the 64-bit BCDL adder. In our proposed method, we are using Boosted CMOS Differential Logic (BCDL) style adder with Binary To Excess-1 Converter are used in our system. It is shown in the following Fig.8. The outgoing carry from each 8-bit subsection goes into Binary to Excess 1 Converter (BEC).

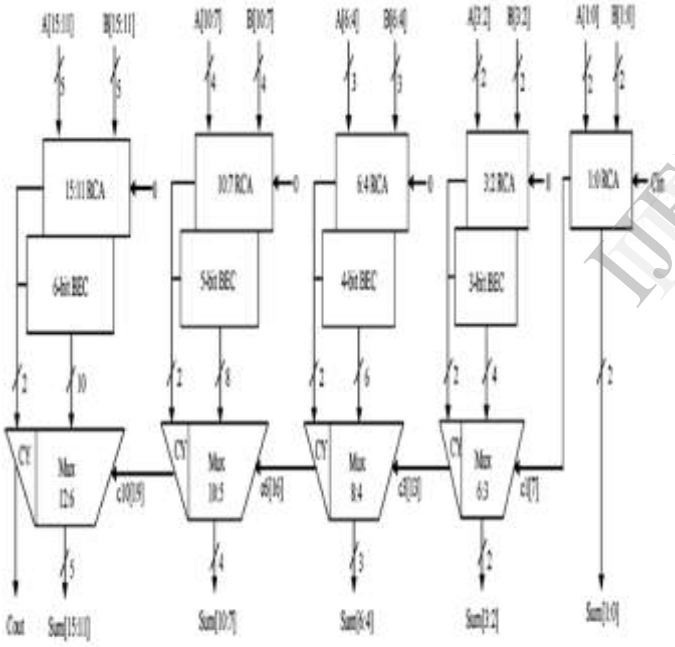

Fig. 8. 16-b Modified CSLA with BEC

There is a pair of BECs in each 8-bit subsection in the upper half of the adder, and carries are selected using the carry bit propagated from the lower half. As shown in Fig .9.

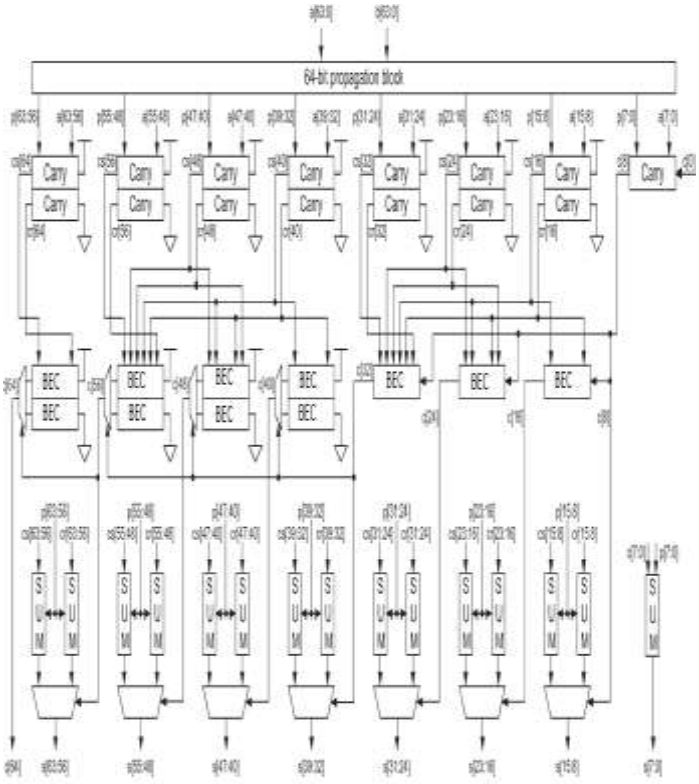

Fig. 9. Block diagram of 64-b (BCDL-BEC) adder

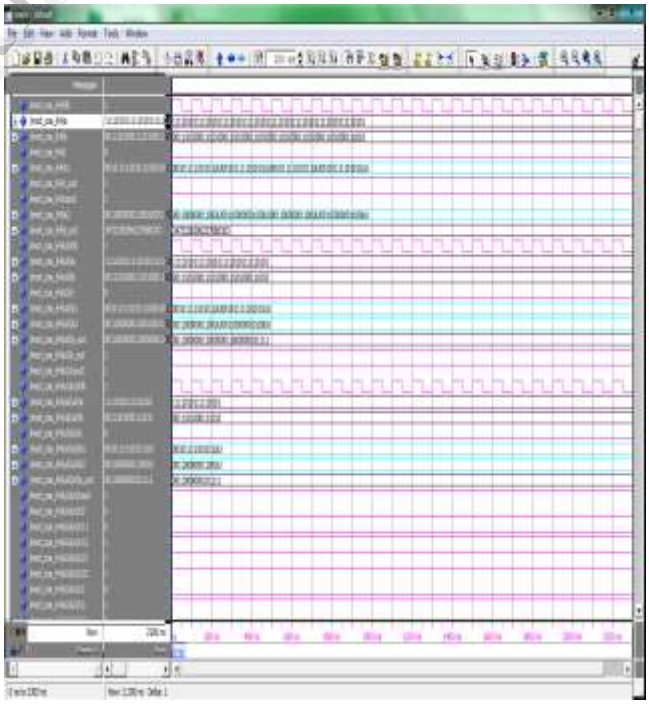

Fig. 10. .Simulated output of a Proposed 64 bit BCDL-BEC adder

The proposed BEC with CSLA based BCDL adder system synthesized in xilinx8.1 and verified the output wave form using modelSim6.3 which is shown in Fig .10 in which according to the input signal .

VI. CONCLUSION

Conventional logic CMOS circuits all are having the drawback of energy consumption due to higher supply voltages. This proposed logic concentrates on the reduction of area, delay and power. A CMOS differential logic style with voltage boosting has been described. The BCDL provides higher switching speed than the conventional logic style at low supply voltage. The BCDL also minimizes area overhead by allowing a single boosting circuit to be shared by complementary outputs. the proposed system consumes low power 56mW then conventional system. The Gate count, Delay and Area is also reduced. Comparison results indicated that the area, power and delay of the proposed logic style was improved compared with conventional logic. The experimental result for a 64-bit BCDL adder designed with the proposed logic style in the BEC so that the computational power required for the CSLA with BEC operations can be reduced. It can be implemented in the operation of CSLA.

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