Low Power & Area Efficient 16 Bit Carry Select Adder Based On Adiabatic Logic

Ms. Archana Kakde [1], Ms. Manisha Waje [2]
[1]*M.E., Electronics and Telecommunication Engineering Department GHRCEM, Wagholi, Pune.*
[2]*Department Of Electronics & Telecommunication, GHRCEM, Wagholi, Pune, India*
University Of Pune

Abstract

Adders are of fundamental importance in a wide variety of digital systems. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. A new CMOS logic family called ADIABATIC LOGIC, based on the adiabatic switching principle is presented. In this paper current parameter of carry select adder will be reduced using adiabatic logic which in turn will reduce heat dissipation of the circuit. Proposed work shows better performance in terms of delay, area & power. Simulation & implementation is based on TannerV13 tool with 0.18µm CMOS process technology.

Keywords— **Application specific integrated circuits (ASIC), Area efficient CSLA, Low power.**

1. Introduction

The importance of a fast, low-cost binary adder in a digital system is difficult to overestimate. Not only are adders used in every arithmetic operation, they are also needed for computing the physical address in every memory fetch operation in CPUs. Due to the growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades, that increases power requirement and it requires more expensive packaging and cooling technologies, increase cost, and decrease system reliability. Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like low power, reliable performance in the processing technology. Power dissipation in CMOS circuits is caused by three sources:

1 The leakage current which is primarily determined by the fabrication technology, consists of reverse bias current in the parasitic diodes formed between source and drain.
2 The short-circuit current which is due to the DC path between the supply rails during output transitions
3 The charging and discharging of capacitive loads during logic changes.
4 The dynamic power dissipation is given by:

$$P = 0.5\ CV_{dd}^2\ E(sw)\ f_{clk}$$

Where C is the physical capacitance of the circuit, V_{dd} is the supply voltage, E(sw) is the switching activity which is the average number of transitions in the circuit per 1/ f_{clk} time, and f_{clk} is the clock frequency.

Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy. Unlike traditional CMOS circuits, which dissipate energy during switching, adiabatic circuits attempt to conserve charge.

This paper presents two new families of adders, both based on a new bit carry Select & adiabatic structure that computes propagate signals called "carry-strength" in a ripple fashion. The first family of adders is a family of new carry-select adders that are significantly faster than traditional carry-select adders while not much larger. The second family of adders

is a family of hybrid lookahead adders similar to those presented in [5] but significantly smaller and still comparable in speed. In our new type of carry-select adder, the new block structure eliminates the delay due to the rippling at the end of the life of a long-range carry signal.

2. Principle of Adiabatic Switching

The word ADIABATIC used to describe thermo dynamic processes that exchange no energy with the environment and no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as Energy Recovery CMOS[3].

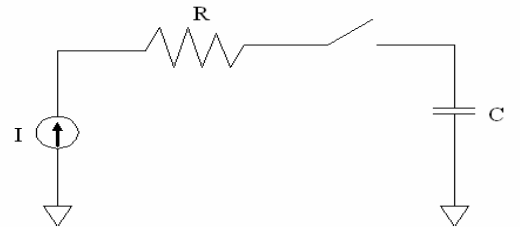

Figure 1. Adiabatic Switching

The load capacitance is charged by a constant-current source. R is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume, the capacitor voltage V_C is zero initially [8].

$E = E_{diss} = [RC/T]CV^2 = [2RC/T][1/2CV^2]$

Therefore from this equation it is observed that
1 The dissipated energy is smaller than for the conventional case, if the charging time T is larger than 2RC.

2 Also, the dissipated energy is proportional to R, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation.

There are two types of adiabatic logic one is Efficient charge recovery Logic (ECRL) & the second is Positive Feedback Adiabatic Logic (PFAL)

2.1 Efficient Charge Recovery Logic (ECRL)

Efficient Charge recovery logic(ECRL) proposed by Moon and Jeong[9], shown in Figure2, uses cross-coupled PMOS transistors.

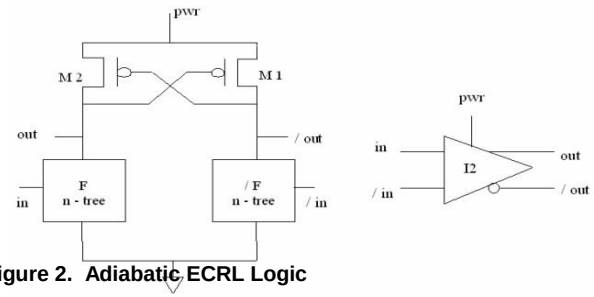

Figure 2. Adiabatic ECRL Logic

It consists of two cross-coupled transistors M1 and M2 and two NMOS transistors in the N-functional blocks for the ECRL adiabatic logic block. An AC power supply pwr is used for ECRL gates, so as to recover and reuse the supplied energy. Both out and /out are generated so that the power clock generator can also drive a constant load capacitance independent of the input signal. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases.

2.2 Positive Feedback Adiabatic Logic (PFAL)

Positive Feedback Adiabatic Logic(PFAL) uses the lowest energy consumption if compared to other families. It uses two PMOS M1-M2 and two NMOS M3-M4.

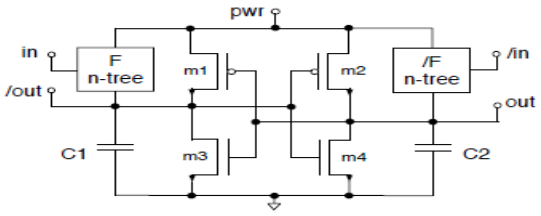

Figure 3. Adiabatic Positive feedback Logic

The two n-trees realize the logic functions. This logic family generates both positive and negative outputs. The structure of PFAL logic is shown in figure 3. The functional blocks are in parallel with the transmission PMOSFET's.

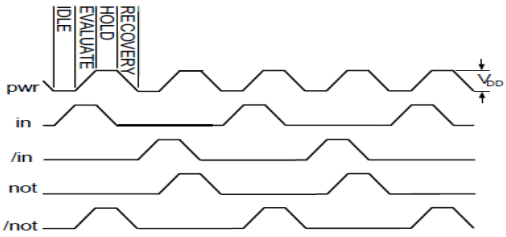

Figure 4. Four Phase Power clock

Thus the equivalent resistance is smaller when the capacitance needs to be charged. From figure 4, During the recovery phase, the loaded capacitance gives back energy to the power supply and the supplied energy decreases. The energy dissipation in a PFAL adiabatic logic gate is described by

$$E=[RC/T]\ CV_{DD}^2$$

where R is the path resistance, C is the capacitance at the output, T is the rise/fall time of the power-clock signal. It increases the leakage currents which limit the energy dissipation in the mid- and low-frequency range.

3. Adiabatic 16 bit carry select adder using PFAL family

A partially adiabatic logic family PFAL 16 bit Carry select Adder block can be implemented as shown in the Figure 5 & 6 for sum & carry block and figure 7 is the combination of sum and carry block. Which gives the final output.

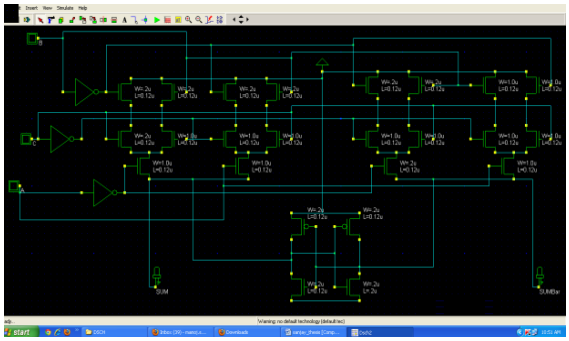

Figure 5. PFAL Sum Circuit

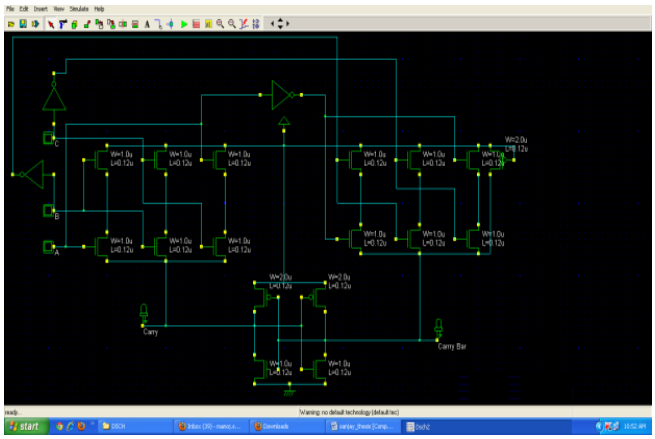

Figure 6. PFAL Carry Circuit

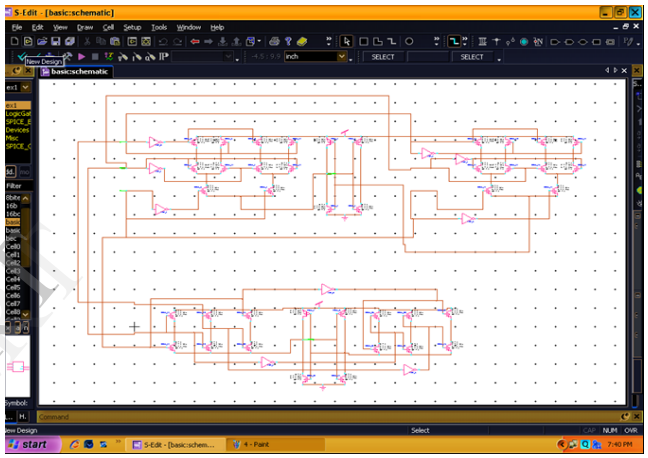

Figure 7. Sum & Carry block 16 bit CSLA using adiabatic logic

4. Comparison between 8 bit and 16 bit positive feedback adiabatic logic CSLA

Word Size	Adder	Area µm²	Delay(ns)
8-bit	8bitadiabatic	928	2.08
	8bitadiabatic BEC	656	2.16
16-bit	16bitadiabatic	1856	2.42
	16bitadiabatic BEC	1312	2.54

Table 1. Comparison between 8 bit and 16 bit positive feedback adiabatic logic CSLA

Comparative study of 8 bit and 16 bit Carry select adder based on positive feedback adiabatic logic as shown in table 1. In that regular Adiabatic 16- bit Carry Select Adder using Ripple carry Adder (RCA) and modified Adiabatic 16- bit Carry Select Adder using Binary to excess-1 (BEC) is compared.

5. Conclusion

In this paper Carry Select Adder will gives reduced power as adiabatic logic is used. Simulation of this design shows area and delay is reduced as compared to conventional CMOS.

6. References

[1] IEEE Transactions on very large scale integration(VLSI) systems, Vol. 20, No. 2, February-2012

[2] C. Cheng & KK Parhi, "Hardware efficient Fast Parallel FIR Filter structures based on iterated short convolution," IEEE Trans. Circuits syst. I, Reg. Papers, Vol.51, No.8, pp. 1492-1500 Aug. 2004

[3] J. M. RABAEY, AND M. PEDRAM, "Low Power Design Methodologies," Kluwer Academic Publishers, 2002.

[4] NAGENDRA, C., IRWIN, M.J., OWENS, R.M.: "Area-time-power tradeoffs in parallel adders", *IEEE Trans. CAS-II*, 43, (10), pp. 689-702.

[5] T. LYNCH, E.E. SWARTZLANDER, "A spanning-tree carry-look-ahead adder", *IEEE Trans. on Comp.*, Vol. 41, n°8, Aug. 1992.

[6] V. KANTABUTRA, "A recursive carry-look-ahead/carry-select hybrid adder", *IEEE Trans. on Comp.*, Vol. 42, n°12, Dec. 1993.

[7] R. Zimmermann and H. Kaeslin, "Cell-Based multilevel Carry-Increment Adders with Minimal AT- and PT-Products, unpublished manuscript. http://www.iis.ee.ethz.ch/~zimmi/

[8] T. INDERMAUER AND M. HOROWITZ, "Evaluation of Charge Recovery Circuits and Adiabatic Switching for Low Power Design," Technical Digest IEEE Symposium Low Power Electronics, San Diego, pp. 102-103, October 2002.

[9] Y. MOON AND D. K. JEONG, "An Efficient Charge Recovery Logic Circuit,"IEEE JSSC, Vol. 31, No. 04, pp. 514- 522, April 1996.

[10] P. Ashok Kumar, B. VIJAYA BHASKHAR "Design Of Adiabatic Logic Based Low Power Carry Select Adder" Vol. 2, Issue4, July-August 2012, pp.1867-1870.

AUTHORS

First Author – Ms. Archana K Kakde, ME (VLSI and Embedded System), GHRCEM, Wagholi Pune .
email : archana.kalpana2005@gmail.com

Second Author – Ms. Manisha Waje, ME(ETC),GHRCEM,Wagholi pune.

Correspondence author – Archana K Kakde
Archana.kakde@raisoni.net