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Low Power and Area Efficient Reconfigurable FIR Filter

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Abstract: **Multiplication of input sample and impulse response. Direct form and interchangeable form implementations are two forms of FIR filter implementations. Instead of direct form, transposed form is most effective. The Multiplication process takes place in multiplier block. Thus transposed form multiplier blocks in FIR filter will replace by MCM architecture also known as shift and add architecture.**

Keywords:-Verilog,Multiple-Constant Multiplication(MCM), Finite Impulse Response, Low Complexity, Distributive Arithmetic(DA)

I INTRODUCTION

In digital signal processing (DSP) systems finite impulse response (FIR) filters have very much importance since their characteristics in linear-phase and feed-forward implementations make them very useful for building stable high performance filter architectures. The direct and transposed form FIR filter logic diagrams are illustrated in Fig.1(a) and 1(b). As shown in figure both architectures have similar complexity in hardware, and the performance and power efficiency.

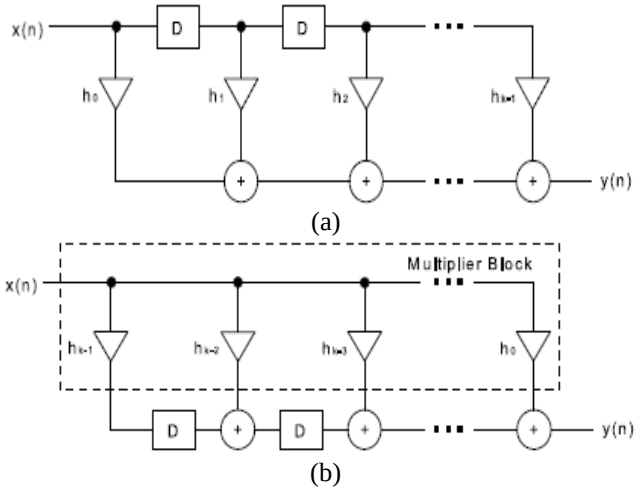

Fig.1. Design of FIR filter. (a) Direct form (b) Transposed form with generic multipliers.

The architecture of a multiplier of the digital FIR filter in its rearrangeable form is shown in [Fig. 1(b)], where the multiplication of filter inputs with the filter coefficients is accomplished, due to the significant impact on the complexity and performance of the design because a huge number of constant multiplications are essential. This is generally known as the multiple constant multiplications (MCM) operation and is also a central operation and performance bottleneck in many other DSP systems such as fast Fourier transforms, discrete cosine transforms (DCT's) and ECC codes.

II. DISTRIBUTED ARITHMETIC (DA)

Filters are usually frequency selective networks, which is capable of modifying an input signal in order to facilitate further processing. Thus digital filters are more preferred than analog due to its high signal integrity [2]. An FIR filters are mainly applied for different DSP areas because providing virtues of linear phase and system stability. The basic convolution equations of filter representation are shown as follows:

$$Y(n) = b_0x(n) + b_1x(n-1) + \ldots + b_Nx(n-N) \quad (1)$$

$$= \sum_{i=0}^{N} bi\, x(n-i) \quad (2)$$

Distributed Arithmetic is termed so because the multiplications that appear in signal processing are reordered and combined such that the arithmetic becomes distributed completely through the structure rather than being lumped. Multipliers are replaced by combinational Look Up Tables (LUT) [3]. Since LUTs are considerably larger in size, the property of materialize the FIR filter primarily relies upon the performance of logic synthesis algorithm mapping to FPGA.

DA provides bit serial operations that implement a series of fixed point MAC operations in a known number of steps, regardless of number of terms to be calculated. The main operations required for DA based computation of inner product are sequence of lookup table access followed by shift accumulation operations of LUT output [9].

According to DA, we can make look up tables (LUT) to store MAC values and call out values accordingly to the input data if necessary. Therefore, LUT's are utilized

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to facilitate the operations of MAC units so as to save hardware resources. This technique also promotes DA computation suitable for FPGA recognition, because the LUT along with shift and add activities can be directly summerized to LUT base FPGA logic structure.

The convenience of DA is its efficiency of mechanization. Itbring out well when the number of ingredients in a vector is nearly same as word size then DA is really fast.

III. PROPOSED WORK

Distributed arithmetic is a famous method of implementing FIR filters without the use of multipliers. In DA the task of summing product terms is replaced by table lookup procedures that are easily implemented on FPGA.

In FIR filtering, one to one diagrams of the scrolling sequences are from two sources, one obtained from input samples while the other sequences are accomplished from fixed impulse response coefficients of filter [6]. This behavior of FIR filter makes it suitable for DA based technique for memory realization. It yields faster output, it stores pre-computed partial results in memory components that can be read out and accumulated to obtain desired result [8].

(LUT), Shifters and accumulator with adder tree. In this technique all the partial product outputs are pre- of FIR filter consists of Look-Up Table computed and placed in a Look Up The Distributed Arithmetic technique Table (LUT). These table entries are addressed by the addresses generated by input multiplier bit data. All inputs are fed simultaneously. From the input data, address will originated and allowed to connect the LUT; its outcome is merged to the accumulated partial products.

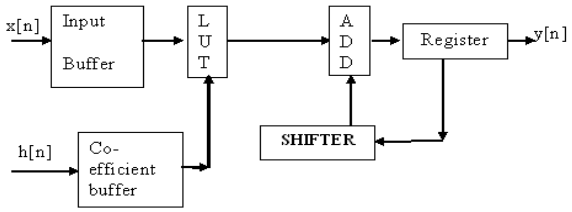
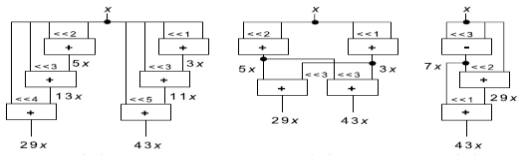


Fig 2:Block diagram of FIR filter using DA

The Basic block diagram for FIR filter implementation using DA [8] is shown in Figure 2. The complete dot product calculations takes L clocks where L is the size of input data, and it is not depended on input data size. During the initial cycle of operation, the Least-Significant Bits of input i.e., $X_0(n)$, $X_0(n-1)$…, of the K input samples are arranged to form K-bit addresses. These addresses are allowed to access Look-Up Table and that table outcome becomes the initial value of the accumulator. During the very next cycle of operation, the next-to-least significant bits $X_1(n)$, $X_1(n-1)$, ..., $X_1(n-K+1)$ of the K input samples are arranged to form K-bit address which will be allowed access lookup, and the adder sums the Look up Table output is shifted by one bit and summed to the contents of the accumulator.



(a) (b) (c)

Fig.3:Shift-add's implementation of 29x and 43x (a) Without partial product sharing and with partial product sharing

1V. SIMULATION AND SYNTHESIS RESULTS

The design have been implemented using Verilog Hardware description language and simulated and synthesized using Xilinx ISE simulator. The synthesis results obtained are targeted for SPARTAN 3E XC3S250E FPGA.

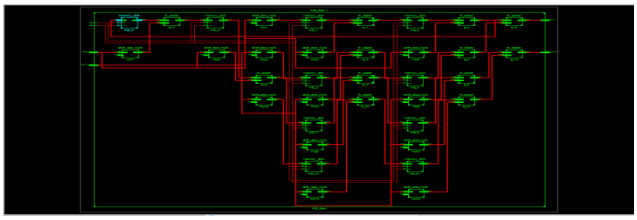


Fig. 4: RTL Schematic for Reconfigurable FIR Filter

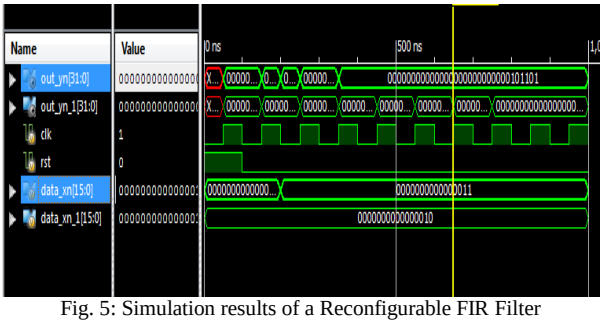


Fig. 5: Simulation results of a Reconfigurable FIR Filter

Table 1: Comparison of Area of existing and proposed

DESIGN	LUT	SLICE's
PROPOSED ADAPTIVE LMS	329	179
PROPOSED RECONFIGURABLE FIR FILTER	271	149

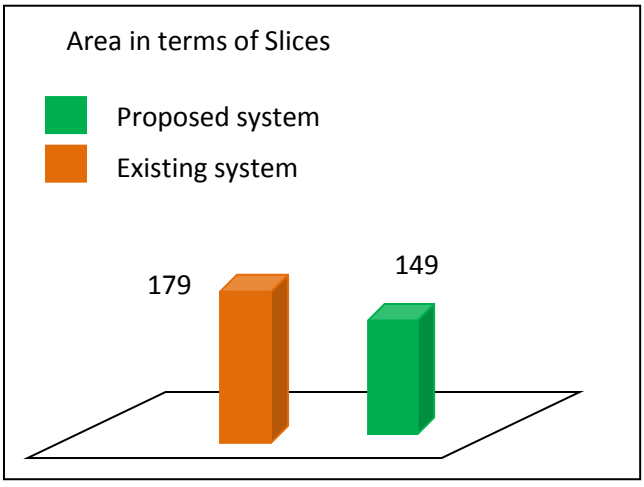


Fig 6: Area in terms of SLICEs for a proposed and existing system

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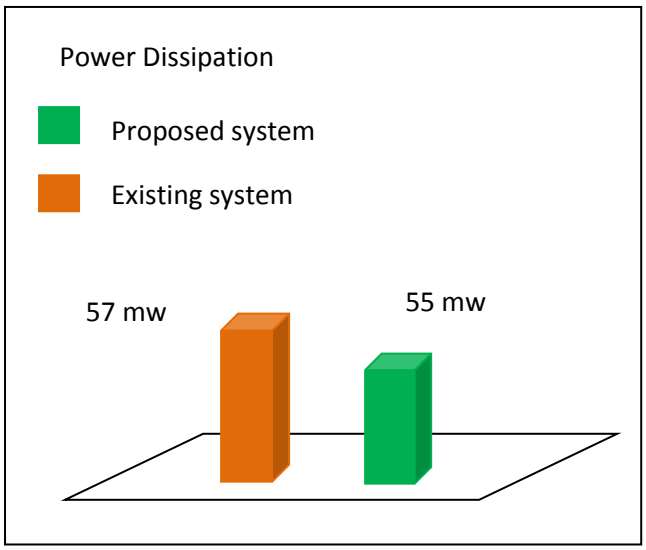

Fig 7: Power dissipation of proposed and existing system

V. CONCLUSION

The proposed architecture shows the area conducive implementation of Digital filter using DA based on FPGA. This architecture replaces the complicated multiplication-accumulation operation with simple shifting and adding operations based DA algorithm which is directly applied to realize FIR filter. The simulation results have been observed by Modelsim simulator. Also synthesized by XILINX XST tool and targeted for SPARTAN 3E FPGA device XC3S250E. Device utilization values of both algorithms are compared. We have examined up to 50% diminishing in the number of pieces and up to 75%shrinkagen the number of LUTs for fully parallel applications.

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