

Low Power and Area Efficient Multiplier Design using ANT Architecture

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Abstract— In this paper, we propose a reliable low-power multiplier design by adopting algorithmic noise tolerant (ANT) architecture with the fixed-width multiplier to build the reduced precision replica redundancy block (RPR). The proposed ANT architecture can meet the demand of high precision, low power consumption, and area efficiency. We design the fixed-width RPR with error compensation circuit via analyzing of probability and statistics. Using the partial product terms of input correction vector and minor input correction vector to lower the truncation errors, the hardware complexity of error compensation circuit can be simplified. In a 12×12 bit ANT multiplier, circuit area in our fixed-width RPR can be lowered by 44.55% and power consumption in our ANT design can be saved by 23% as compared with the state-of-art ANT design.

Index Terms— Algorithmic noise tolerant (ANT), Fixed-width multiplier, Reduced-precision replica (RPR), Voltage overscaling(VOS), Column bypassing multiplier.

I. INTRODUCTION

The portable and wireless computing systems drives the need for ultralow power systems in recent years due to its rapid growth. To minimize the power dissipation, supply voltage scaling is widely used as an effective low-power technique [1]. However, in deep-submicrometer process technologies, noise interference problems have raised difficulty to design the reliable and efficient microelectronics systems; hence, to enhance noise tolerance design techniques are developed [2]–[12].

An effective low power technique known as voltage over scaling(VOS), was proposed to lower the power supply without sacrificing the throughput[4]. However, VOS leads to severe degradation in signal-to-noise ratio (SNR). To overcome this a novel algorithmic noise tolerant (ANT) technique [2] combined VOS main block with reduced-precision replica (RPR), which combats soft errors effectively while achieving significant energy saving. Some ANT deformation designs are presented in [5]–[9] and the ANT design concept is further extended to system level in [10]. However, the RPR designs in the ANT designs of [5]–[7] are designed in a customized manner, which are not easily adopted and repeated. The RPR designs in the ANT designs of [8] and [9] can operate in a very fast manner, but their hardware complexity is too complex. As a result, the RPR design in the ANT design of [2] is still the most popular design because of its simplicity. However, adopting with RPR in [2] should still pay extra area overhead and power

consumption. In this paper, we further proposed an easy way using the fixed-width RPR to replace the full-width RPR block

in [2]. Using the fixed-width RPR, the computation error can be corrected with lower power consumption and lower area overhead. We take use of probability, statistics, and partial product weight analysis to find the approximate compensation

vector for a more precise RPR design. In order not to increase the critical path delay, we restrict the compensation circuit in RPR must not be located in the critical path. As a result, we can realize the ANT design with smaller circuit area, lower power consumption, and lower critical supply voltage.

II. ANT ARCHITECTURE DESIGNS

The ANT technique [2] includes both main digital signal processor (MDSP) and error correction (EC) block as shown in Fig. 1. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay T_{cp} of the system becomes greater than the sampling period T_{samp} , the soft errors will occur. It leads to severe degradation in signal precision. In the ANT technique [2], a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block. Under VOS, there are a number of input-dependent soft errors in its output $y_a[n]$; however, RPR output $y_r[n]$ is still correct since the critical path delay of the replica is smaller than T_{samp} [4]. Therefore, $y_r[n]$ is applied to detect errors in the MDSP output $y_a[n]$. Error detection is accomplished by comparing the difference $|y_a[n] - y_r[n]|$ against a threshold T_h . Once the difference between $y_a[n]$ and $y_r[n]$ is larger than T_h , the output $y[n]$ is $y_r[n]$ instead of $y_a[n]$. As a result, $y[n]$ can be expressed as

$$\begin{aligned} y[n] &= y_a[n], \text{ if } |y_a[n] - y_r[n]| \leq T_h \\ y[n] &= y_r[n], \text{ if } |y_a[n] - y_r[n]| \geq T_h \end{aligned}$$

T_h is determined by,

$$T_h = \max |y_o[n] - y_r[n]|$$

Where, $y_o[n]$ is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation [2].

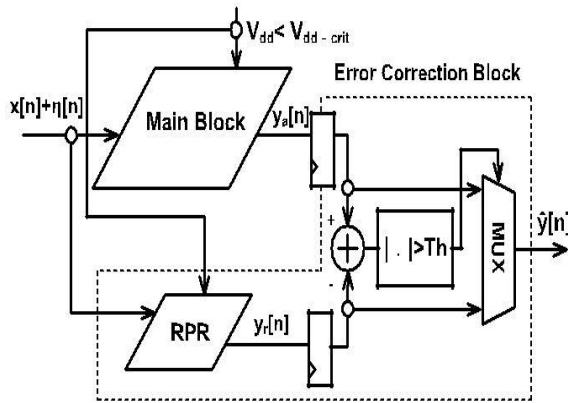


Fig.1. ANT Architecture [2].

III. PROPOSED ANT MULTIPLIER DESIGN USING FIXED-WIDTH RPR

In this paper, we further proposed the fixed-width RPR to replace the full-width RPR block in the ANT design [2], as shown in Fig. 2, which can not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating supply voltage, and lower power consumption in realizing the ANT architecture. We demonstrate our fixed-width RPR-based ANT design in an ANT multiplier.

The fixed-width designs are usually applied in DSP applications to avoid infinite growth of bit width. Cutting off n-bit least significant bit (LSB) output is a popular solution to construct a fixed-width DSP with n-bit input and n-bit output. The hardware complexity and power consumption of a fixed-width DSP is usually about half of the full-length one. However, truncation of LSB part results in rounding error, which needs to be compensated precisely. Many literatures [13]–[22] have been presented to reduce the truncation error with constant correction value [13]–[15] or with variable correction value [16]–[22]. The circuit complexity to compensate with constant corrected value can be simpler than that of variable correction value; however, the variable correction approaches are usually more precise.

In [16]–[22], their compensation method is to compensate the truncation error between the full-length multiplier and the fixed-width multiplier. However, in the fixed-width RPR of an ANT multiplier, the compensation error we need to correct is the overall truncation error of MDSP block. Unlike [16]–[22], our compensation method is to compensate the truncation error between the full-length MDSP multiplier and the fixed-width RPR multiplier. In nowadays, there are many fixed-width multiplier designs applied to the full-width multipliers. However, there is still no fixed-width RPR design applied to the ANT multiplier designs.

To achieve more precise error compensation, we compensate the truncation error with variable correction value. We construct the error compensation circuit mainly using the partial product terms with the largest weight in the least significant segment. The error compensation algorithm

makes use of probability, statistics, and linear regression analysis to find the approximate compensation value [16]. To save hardware complexity, the compensation vector in the partial product terms with the largest weight in the least significant segment is directly inject into the fixed-width RPR, which does not need extra compensation logic gates [17]. To further lower the compensation error, we also consider the impact of truncated products with the second most significant bits on the error compensation. We propose an error compensation circuit using a simple minor input correction vector to compensation the error remained. In order not to increase the critical path delay, we locate the compensation circuit in the noncritical path of the fixed-width RPR. As compared with the full-width RPR design in [15], the proposed fixed-width RPR multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption.

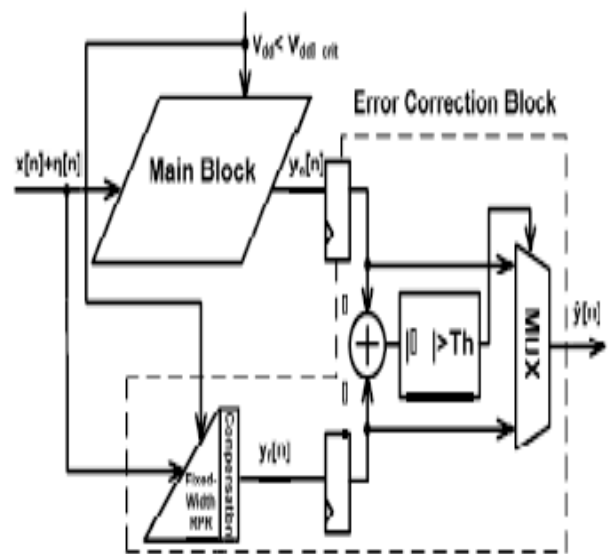


Fig.2. Proposed ANT Architecture with fixed-width RPR.

A. PROPOSED PRECISE ERROR COMPENSATION VECTOR FOR FIXED-WIDTH RPR DESIGN

In the ANT design, the function of RPR is to correct the errors occurring in the output of MDSP and maintain the SNR of whole system while lowering supply voltage. In the case of using fixed-width RPR to realize ANT architecture, we not only lower circuit area and power consumption, but also accelerate the computation speed as compared with the conventional full-length RPR. However, we need to compensate huge truncation error due to cutting off many hardware elements in the LSB part of MDSP. In the MDSP is designed using column bypassing multiplier.

The column bypassing structure has a full adder and the multiplexer. Column Bypassing with reference to multiplier means turning **off** some columns in the multiplier array whenever certain multiplicand bits are zero. In this technique, during working, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0, to save the

power. This technique is totally depended on the number of zeroes in the multiplicand bits. To implement this technique, we have to modify our full adder required in general multiplication as shown in fig.3.

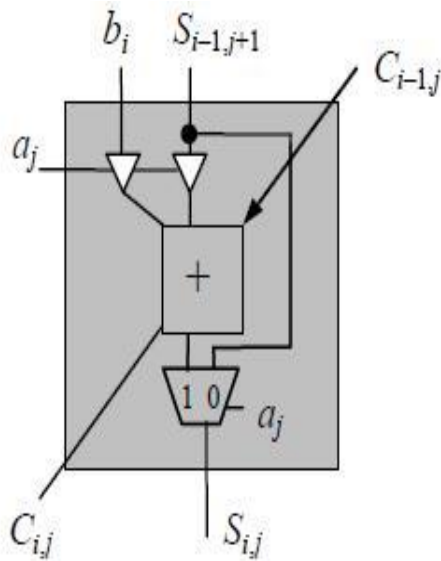


Fig.3.The Modified FA Cell For Column Bypass Multiplier.

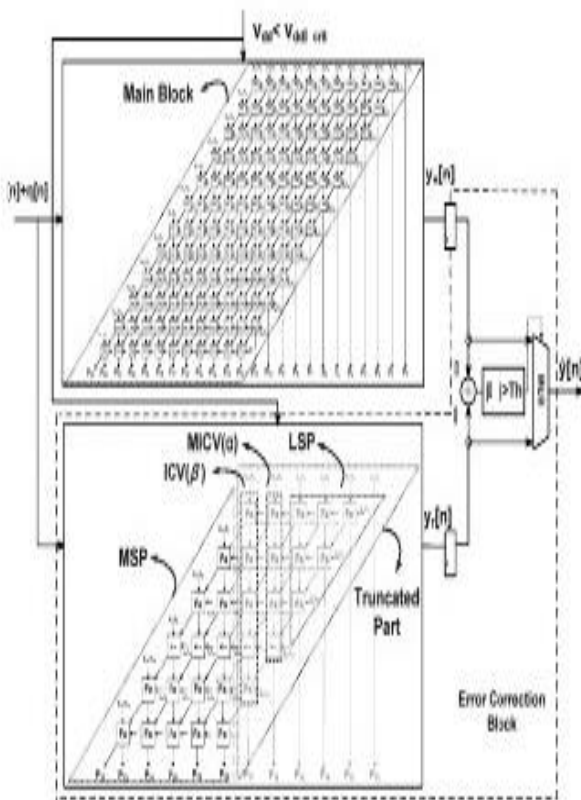


Fig. 4. 12 × 12 bit ANT multiplier is implemented with the six-bit fixed-width replica redundancy block.

Here where $f(EC)$ is the error compensation function, $f(ICV)$ is the error compensation function contributed by the input correction vector $ICV(\beta)$, and $f(MICV)$ is the error compensation function contributed by minor input correction vector $MICV(\alpha)$. The source of errors generated in the fixed-width RPR is dominated by the bit products of ICV since they have the largest weight. In [8], it is reported that a low-cost EC circuit can be designed easily if a simple relationship between $f(EC)$ and β is found. It is noted that β is the summation of all partial products of ICV. By statistically analyzing the truncated difference between MDSP and fixed-width RPR with uniform input distribution, we can find the relationship between $f(EC)$ and β . As shown in Fig. 4, the statistical results show that the average truncation error in the fixed-width RPR multiplier is approximately distributed between β and $\beta+1$. More precisely, as $\beta = 0$, the average truncation error is close to $\beta + 1$. As $\beta > 0$, the average truncation error is very close to β . If we can select β as the compensation vector, the compensation vector can directly inject into the fixed-width RPR as compensation, which does not need extra compensation logic gates [17]. We go further to analyze the compensation precision by selecting β as the compensation vector. We can find that the absolute average error in $\beta = 0$ is much larger than that in other β cases.

Moreover, the absolute average error in $\beta = 0$ is larger than $0.5 * 2(3n/2)$, while the absolute average error in other β situations is smaller than $0.5 * 2(3n/2)$. Therefore, we can apply multiple input error compensation vectors to further enhance the error compensation precision. For the $\beta > 0$ case, we can still select β as the compensation vector. For the $\beta = 0$ case, we select $\beta + 1$ combining with MICV as the compensation vector. Before directly injecting the compensation vector β into the fixed-width RPR, we go further to double check the weight for the partial product terms in ICV with the same partial product summation value β but with different locations.

For the $\beta = 0$ case, we go further to analyze the error profile the ICV and MICV. In ICV, we can find that all the truncation errors are positive when $\beta = 0$. It implies us that if we adopt the multiple compensation vectors for the average compensation error terms are larger than $0.5 * 2(3n/2)$, we can lower the compensation error effectively and no additional compensation error will be generated. The multiple compensation vectors are constructed by $ICV(\beta)$ combined with $MICV(\alpha)$. The weight of $MICV(\alpha)$ is only half of $ICV(\beta)$. The summation of all partial products of $MICV(\alpha)$, which is denoted as βl , have four possible values of 0, 1, 2, and 3 as $n = 12$ and $\beta = 0$. The statistical results show that the average truncation error contributed by the MICV in the case of $\beta = 0$ is approximately proportional to α . Moreover, the absolute average truncation error in the situation of $\alpha = 0$ is smaller than $0.5 * 2(3n/2)$, while the absolute average truncation error in the situation of $\beta l > 0$ is larger than $0.5 * 2(3n/2)$.

For the case of the absolute average truncation error is smaller than $0.5 * 2(3n/2)$, $\beta l = 0$, selecting β as the

compensation vector is suitable. However, for the case of the absolute average truncation error is larger than $0.5 * 2(3n/2)$, selecting β as the compensation vector is not suitable since insufficient error compensation will occur. Therefore, we adopt ICV together with MICV to amend this insufficient error compensation case when $\beta = 0$ and $\beta l > 0$ as well.

If $\beta = 0$ is contributed by $\beta l > 0$, we will inject one more carry-in compensated vector in the weight of $2(3n/2)$. In this way, we can remove the cases of $|\epsilon| > 0.5 * 2(3n/2)$ effectively. The compensation error is effectively lowered by adopting ICV together with MICV while comparing with the case of fixed-width RPR only applying the compensation vector of β and with the case of full-width RPR.

B. Proposed Precise Error Compensation Vector for Fixed-Width RPR Design

To realize the fixed-width RPR, we construct one directly injecting ICV(β) to basically meet the statistic distribution and one minor compensation vector MICV(α) to amend the insufficient error compensation cases. The compensation vector ICV(β) is realized by directly injecting the partial terms of $X_{n-1} Y_{n/2}$, $X_{n-2} Y_{(n/2)+1}$, $X_{n-3} Y_{(n/2)+2}$, ..., $X_{(n/2)+2} Y_{n-2}$. These directly injecting compensation terms are labeled as C_1 , C_2 , C_3 , ..., $C_{(n/2)-1}$. The other compensation vector used to mend the insufficient error compensation case is constructed by one conditional controlled OR gate. One input of OR gate is injected by $X_{(n/2)} Y_{n-1}$, which is designed to realize the function of compensation vector β . The other input is conditional controlled by the judgment formula used to judge whether $\beta = 0$ and $\beta l = 0$ as well. The term C_{m1} is used to judge whether $\beta = 0$ or not. The judgment function is realized by one NOR gate, while its inputs are $X_{n-1} Y_{n/2}$, $X_{n-2} Y_{(n/2)+1}$, $X_{n-3} Y_{(n/2)+2}$, ..., $X_{(n/2)+2} Y_{n-2}$. The term C_{m2} is used to judge whether $\beta l = 0$. The judgment function is realized by one OR gate, while its inputs are $X_{n-2} Y_{n/2}$, $X_{n-3} Y_{(n/2)+1}$, $X_{n-4} Y_{(n/2)+2}$, ..., $X_{(n/2)+1} Y_{n-2}$. If both of these two judgments are true, a compensation term C_m is generated via a two-input AND gate. Then, C_m is injected together with $X_{(n/2)} Y_{n-1}$ into a two-input OR gate to correct the insufficient error compensation. Accordingly, in the case of $\beta = 0$ and $\beta l = 0$ as well, one additional carry-in signal $C_{(n/2)}$ is injected into the compensation vector to modify the compensation value as $\beta + 1$ instead of β . Moreover, the carry-in signal $C_{(n/2)}$ is injected in the bottom of error compensation vector, which is the farthest location away from the critical path.

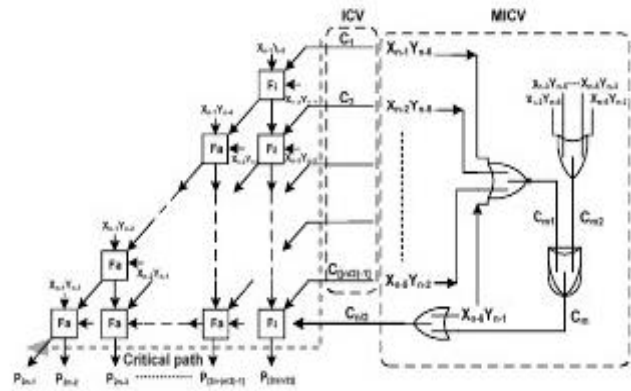


Fig. 5. Proposed high-accuracy fixed-width RPR multiplier with compensation constructed by the multiple truncation EC vectors combined ICV together with MICV.

IV. PERFORMANCE COMPARISONS

To evaluate and compare the performance of the proposed fixed-width RPR based ANT design and the previous full width RPR-based ANT design, we implemented these two ANT designs in a 12-bit by 12-bit multiplier. The main performance indexes are the precision of RPR blocks, the silicon area of RPR blocks, the critical computation delay of RPR blocks, the error probability of RPR blocks under VOS, and the lowest reliable operating supply voltage under VOS. Through quantitative analysis of experimental data, we can demonstrate that our proposed design can more effectively restrain the soft noise interference resulting from postponed computation delay under VOS when the circuit operates with a very low-voltage supply. Moreover, hardware overhead and power consumption can also be lowered in the proposed fixed-width RPR-based ANT design.

V. CONCLUSION

Due to ANT architecture the power consumption is reduced. The column bypassing design implemented in the main block reduces the area to the great extend than the normal array multiplier design. Thus due to the usage of the ANT architecture and the column bypassing method for multiplier design power as well as area is reduced. The performance of the system is also increased.

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