Low Power 6T SRAM Design using 45nm Technology

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***Abstract*—Memories are nothing but series of SRAM or DRAM. SRAM has been playing major role in the world VLSI industry becauseof their large occupancy and shortinterval. In the field of research, SRAM has been prioritized due to considerable growth of low power and low voltage memory designs in the course of emerging times. This is due to large requirement of high-end gadgets, IC memory card and other communication devices and also, becauseof enhancement of portable battery-operated devices. In this paper, low power 6T-SRAM cell design isevaluated for power and area. The high agility orderand reduction in technology cause to more convolution with elevated power dissipation. This paper presentsthe schematic, simulation of transient and DC analysis of 6T SRAM cell, 6T SRAM has beenscrutinizedfor dynamic power, static power, area measurementsat gpdk045 technology. The Cadence Virtuoso tool is availed for drawing schematic,editing layout, design rule checking (DRC), layout versus schematic (LVS) to check whether layout matches the schematic. (Mukesh Kumar, 2017).Additionally, also taken care of lowest voltage supply of 1V provided for the design under 45 nm technology.**

Keyword: Memory; SRAM; Cadence tool; DRC; LVS;Power consumption.

I. INTRODUCTION

For nearly 5 to 6 years back electronics device like mobile phone had a single process, but nowadays mobile appliances have octa-core processor, then the transistor density will be more and also the Capacity but the size will be less, so we are designing the area efficient memory. SRAM cell don't need sustained restoring to keep information as long as power is there. This crucial lead of SRAM is the basis why it is taken over (DRAM). SRAM's unification with standard CMOS technology gives it the likelihood to become the exceedinglyfinestarea consumer on System on Chips (SoCs).(Bhaskar, 2017), Low voltage nano-scale SRAMS are becoming remarkably important. Technology scaling effects in a significant increase in leakage current of CMOS system which expands Power consumption of the device. As the integration density of transistors enlarges, leakage current which increases Power dissipation has becomeextensive cover in today's tech world(Saurabh, 2012). The SRAM cell occupies the 50% of the processor for any digital chip so it can perform the criteria like speed, power dissipation, and also area, for this faster processor we should design the fastest RAM, so for this design we are using the CMOS inverter in SRAM cell. An attempt to reduce power, area and analyze the performance of 6T SRAM cell foundin CMOS technology is performed. Outcome shows 6T SRAM cell with 45nm technology has improved SNM curve and lower power and area compared 8T SRAM cell. (S.Kumar, 2015)It is observed that scaling down in terms of transistor, size and voltage reduces dynamic power, area. Power consumption of 8T SRAM cell is 25nw in 65nm technology and expected result for 6T SRAM cell in 15nw or lesser than that of the 8T SRAM. Area of the 6T SRAM layout is around 3.5µm².

II. LITERATURE SURVEY

K Takeda,Y.Hagihara, M. Nomura, proposed an IEEE paper in Jan 2006 [1],where it tells that the main problem is the limits of the speed of conventional SRAM. Here seven transistors are taken to attain low-VDD and high-speed implementation and area of proposed SRAM is 23%less than that of regular SRAM.

Farshad Moradi,Mohammad Tohidi,Behzad Zeinali,proposed an IEEE paper in 25th Nov 2015 [9].The main problem is SRAM arrays put upmorequantity of power consumption for the processors in sub-100nm technology. Here 8t are used to design SRAM cell using 65nm.This new 8t SRAM cell exhibits upgrade in read and write margins by 2.2X and 22% contrast to usual 6t SRAM cell.

Soumitra Pal,and Aminul Islam proposed an IEEE paper on Mar 2016[12],which tells that it is problem to achieve SRAM cell with stable operation at low voltage for low power process,voltage and temperature.In this paper, a

double ended read decoupled 9T SRAM cell is proposed,and proposed cell supports the column bit inter leaving architecture.Dueto its read-decoupled technique,its noise tolerance is improved.

T Santhosh Kumar, Suman Lata TripathiInternational Journal of Engineering in Jan 2019 [20], in this paper, the major problem with the design of memories are speed and power performance.Different configurations the SNM is calculated by butterfly curve using 45nm technology.Power consumed by 7,8,10,12 transistors SRAM cells is 20nw,25nw,30nm,33nw respectively.

III. METHODOLOGY

The schematic diagram of designed 6T SRAM cell using 45nm technology is as shown in Fig.1. A typical SRAM cell is composed of six MOSFETs. Each bit in an SRAM is stored on four transistors (P1, P2, N1 and N2) that form two cross-coupled inverters. This secondary cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to regulate the ingress to the cell during read and write operations. Access to the cell is enabled by the word line WL which controls the two access transistors N4 and N3 which in turn, control whether the cell should be connected to the bit lines: BL and BLB. The bit lines BL and BLB used to transfer the data for both read and write operations. During read accesses, the bit lines are actively driven high and low by the inverters within the SRAM cell.(Saurabh, 2012)

The SRAM cell has three variant states:

1. Write state (when updating the data)
2. Read state (when the data has been updated)
3. Standby state (when the circuit is idle)

The three different states work as follows:

1. Write state(when updating the data):

The values to be written into the memory cell are provided with the help of bit lines and there by write state begins. Bit lines are pre-charged with high voltage. The information will be stored in the SRAM memory cell until the power is supplied. WL is then asserted and therefore the value that's to be stored is latched in. This works because bit line input-drivers are designed to be stronger than the relatively weak transistors within the cell itself. Access NMOS transistors N4 and N3 have to be stronger than either bottom NMOS (N1, N2) or top PMOS (P1, P2) transistors. This can be easily obtained because PMOS transistors are much weaker than NMOS when both are in same size. If logic 0 has to written,BLB charged to VDD and BL is discharge through ground, then the WL gets active and data is written into the cell.

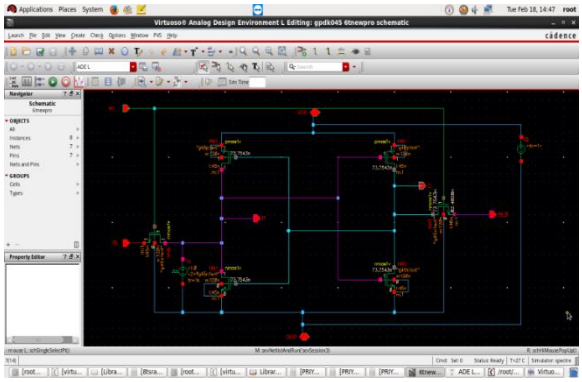

Fig.1. 6T SRAM cell schematic in cadence virtuoso

2. Read state (when the data has been requested):

During read state, both bit lines are pre-charged to logical 1. Bit lines are act as output during read operation and contains large parasitic capacitance. After pre-loading of both the bit lines BL and BLB, word line WL is asserted which enables both the access transistors N4 and N3 that are connected to the bit lines, which causes one-bit line BL voltage to slightly drop. Then the BL and BLB lines will have a small voltage difference between them. Bit lines are traditionally pre-charged to high voltage. Second step occurs when the values stored at SRAM cell are transferred to the bit lines by leaving bit at its pre-charged value and discharging BLB through N4 and N3 to a logical 0.

3 *Standby state (when the circuit is idle):*

During this standby state, the word line is not asserted which in turn turns off the access transistors. The access transistors N4 and N3 disconnect the cross coupled inverters from the bit lines. The two cross-coupled inverters formed by P2-N1 and P1-N2 will continue to reinforce each other as long as they are connected to the supply and the value stored in the SRAM cell retains its value in this condition. Hence the state called as idle state. (Shikha & Hemant, 2019)

IV. IMPLEMENTATION

Implementation of the proposed design is given in terms of power and area and performance of the SRAM cell is analyzed in terms of transient and dc analysis.

A. Transient Analysis

Transient analysis which issues the time domain waveforms which are plots of current or voltage versus time. Transient response is a measure of how well a DC is supplied.Transient analysis is performed to simulate the inverter to check its functionality, visualize the input and output waveforms and to calculate its delay, rise time and also fall time.This analysis also calculates the circuit response over a period of time which is defined by the user. The accuracy of the transient analysis depends on dimension of internal time steps, which together structure the entire simulation time referred to as Run to time or Stop to time.

B. DC a.nalysis

DC analysis which gives DC current or voltage, usually versus a stepped voltage or current.DC simulation is used to plot the inverters characteristics curve. The characteristics are often helpful in determining the inverters threshold voltage, noise margins and its gain. DC analysis is useful for characterizing the static behavior of a circuit.The dynamic behavior characterization requires running a transient analysis. Before setting up a new simulation we need first to modify the schematic of a circuit.

Fig.2 shows the Transient and DC analysis of 6T SRAM cell respectively. The inverted output waveform in transient analysis of SRAM cells with respect to input waveform which is similar to inverter circuit output and hence,we can conclude we have got good results for our transient analysis. According to ohms law ,in DC analysis if input waveform of vertical straight line applied then output waveforms should be exponential and hence, from this we can also conclude that we have correct results for DC analysis .from these two analysis, it is proved that proposed 6T SRAM schematics are working properly and we can further proceed to calculate power and area from layout.

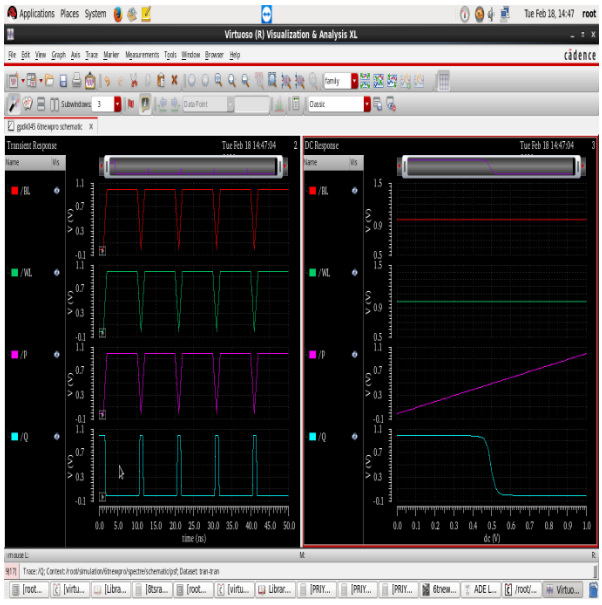

Fig.2. Transient and DC analysis of 6T SRAM Cell

C. Area of layout

The layout of the inspected cell types areimplemented using a standard metal CMOS n-well process at the 45nm technology node. To make sure both read stability and write stability, transistors must satisfy certain dimensional limitation. Additionally, so as to achieve good layout density, transistors must be designed to be as small as possible. In general we can also say that the driver transistors must be well built than that of the access transistor i.e, to read ability and access transistors should persuade against pull-up transistor that was set for all cells are the following: 6/2 for pull driver transistors, 4/2 for access transistors and 3/2 for pull-up transistors. For signal routing, three metal layers ae used. The connection with is made the core ie, latch of the cells are implemented with metal-1 wires and poly silicon gates, while input and output routing paths also contains the metal-2 and metal-3 wires. Data and Data node represent cell outputs. Layout of the proposed 6T SRAM cell is in Fig 3.

The layout design and area efficiency are continuous reduce in size, scale or extent for CMOS technology that intensifies the efforts for far more compact structure and shrinking of circuit element. (Manna, 2017)So, it also can extend the delay time, due to shorter signal routes. Both DRC and LVS

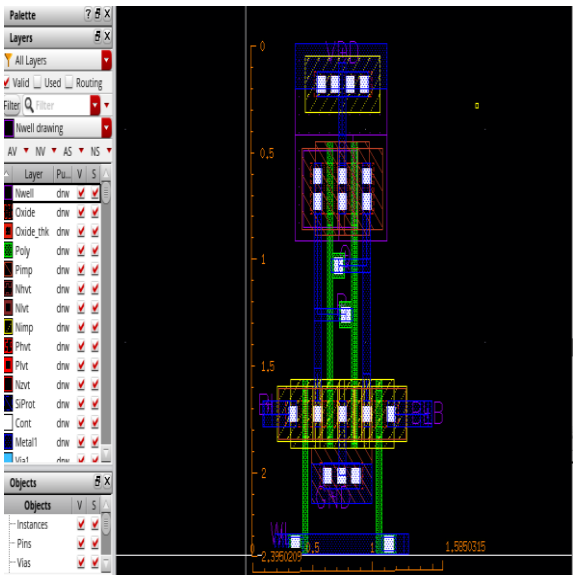

Fig.3. Layout of 6T SRAM Cell

has been verified. The calculated area of 6T SRAM Layout shown in Fig 4

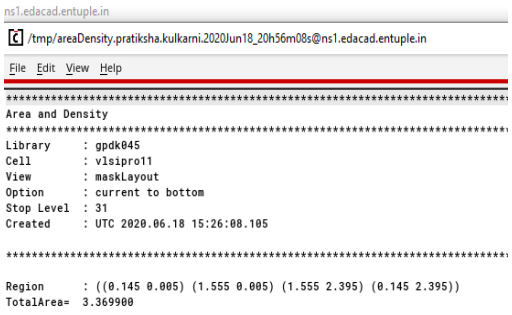

Fig.4. Area of the 6T SRAM cell layout

V.RESULT

Cadence simulation is for analyzing of DC and Transient waveform which has given a good result in 45nm technology. Here, the analyzing was done by the support of DC simulation results by giving inputs as a DC signal to understand the stability of the SRAM cell. Power has been calculated with the assistance of Cadence tool.

The calculated power with the comparison between the 6T and 8T SRAM cell which is shown in the TABEL I.Static power, average power and dynamic power has been calculated. Tables shows:Power waste reduces with the scaling of technology. The power dissipation depends on the supply voltage and parameter.

Parameters	6T SRAM Cell	8T SRAM Cell
Supply Voltage	1 V	1 V
Static Power	8.62pW	8.1pW
Dynamic Power	61.98pW	23.5nW
Average Power	70.60pW	23.52nW

TABLE I. Power of 6T SRAM Cell

Area has been downscaled by constructing layout as minimum as possible and obtained area is 3.36 m^2.

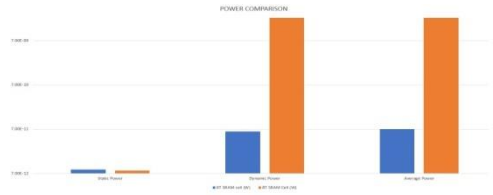

Fig.5. Power of comparison of 6T and 8T SRAM cell

V. CONCLUSION

This papershowcases the pattern of SRAM cell in 45nm technology that have very low power consumption and also area. The low power 6T SRAM cell design is investigated. The transient and DC analysis is carried in simulation process and the power consumption is estimated. Also,the simulation of this project is done by Cadence Virtuoso tool. The simulation is done for 6T SRAM cell using 45nm technology. The design shows the improvement of speed and also scaling of technology also area is decreased. Power dissipation also decreases with scaling of technology. (Mohammad, 2019)Simulation and result analysishas been done in terms of power dissipation and area. Both DRC and LVS checks has been satisfied with no errors and low area consumption.

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