# Low Power 1 Bit SRAM Architecture Design using GALEOR Technique

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***Abstract*—In this paper a 10T 1-bit static random access memory (SRAM) cell has been proposed by incorporating gated leakage transistor (GALEOR) with conventional 6T SRAM. In the proposed GALEOR technique one gated NMOS transistor is included between pull up and output and one gated PMOS transistor is added between pull down and output. Simulation of the proposed design is done in Cadence environment on 180 nm Standard CMOS process. The proposed design achieves substantial reduction in leakage power in read and write operation.**

***Keywords—6T SRAM; static noise margin; GALEOR;leakage power***

## I. INTRODUCTION

Semiconductor memory arrays are very crucial part in any digital system as it can hold a large number of digital information in terms of '1's and '0's. Memory arrays[1] can be divided into three categories, Random Access Memory (RAM), Serial Access Memory and Content Addressable Memory(CAM).RAMs are further divided into two categories Read/Write Memory or RAM which is volatile in nature and read only memory (ROM) which is non-volatile in nature. Volatile memory can hold its data as long as power is applied, while non-volatile memory can hold its data indefinitely. Read/Write memory or RAM can be further divided into two categories static RAM or SRAM and dynamic RAM or DRAM. DRAM are widely used for the main memory in personal and mainframe computers as it has low cost and high density whereas SRAMs are only used in cache memory and handheld devices where high speed and low power consumption is required. The SRAM cell has bi-stable latch structure and can hold one of the two possible state '0' or '1' until the power is on, no refresh operation is requiredby SRAM.

*Design Overview*

This work focuses on the design of the Low Power 1 Bit SRAM Architecture. Static power dissipation is an important issue for the design of any memory cell. In this design GALEOR technique has been used to reduce the static power dissipation of the SRAM cell. The total architecture is divided into four parts as shown in Fig.1

1.Precharge Circuitry
2.10TGALEOR SRAM Cell
3.Write Driver
4.Sense Amplifier

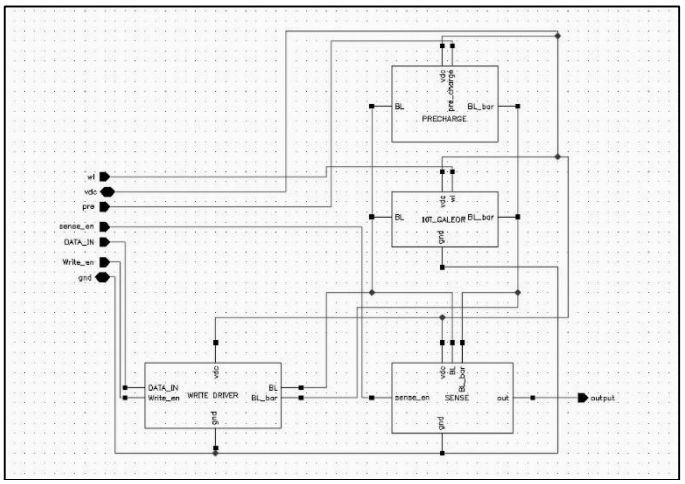


Fig.1 1 Bit Architecture Using 6T GALEOR

## II. CONVENTIONAL 6T SRAM

As shown in Fig.2a conventional 6T SRAM cell consists of two cross coupled CMOS inverters, two access transistors M3 and M4, two bit lines BL and BL_bar and one wordline WL.WL turns on the access transistors and connects the cell with two bitlines BL and BL_bar. There are mainly three operations can be done using SRAM cell, READ operation WRITE operation and HOLD operation.

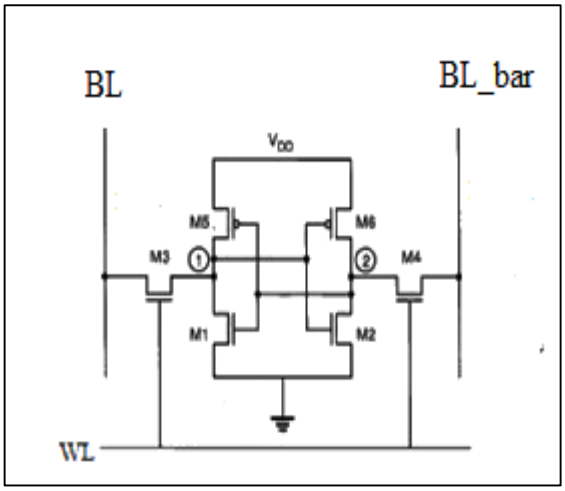


Fig.2 Conventional 6T SRAM Cell

*Working of SRAM Cell*

To perform a WRITE operation of a conventional 6T SRAM cell [2-4] shown in Fig.2, WL is raised to high, the bitlines are set at opposite voltage such that to write '1' in the cell BL will be high and BL_barwill be low. Data will be stored in two nodes node 1 and node 2. During write operation the pull up and pull down ratio will be according to the equation (1).

$$\frac{k_{n,3}}{k_{n,1}} = \frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}} < \frac{\mu_n}{\mu_p} \frac{2(V_{dd}-1.5V_{T,n})V_{T,n}}{(V_{dd}+2V_{T,p})^2} \qquad (1)$$

Now during the read operationthe WL will be raised to high, both bit lines will be precharged to high value, as one of the nodes are in low value, one of the precharged bit lines will be start to discharge.

In read operation we have to take care of certain things, so that the stored data will not destroy or flip. The two conditions for the READ operations are

$$V_1 < V_{T,2} \qquad (2)$$

$$\frac{k_{n,3}}{k_{n,1}} = \frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}} < \frac{2(V_{dd}-1.5V_{T,n})V_{T,n}}{(V_{dd}-2V_{T,n})^2} \qquad (3)$$

In HOLD operation WL will be OFF, the cell will retain its stored value.

## III. STATICNOISEMARGIN (SNM)

Static Noise Margin (SNM) [5] is used to measure the stability of SRAM cell. A basic SNM or butterfly curve is formed by mirroring the inverter characteristics. Then maximum possible square will be fitted between them, now from the diagonal of the square we will find the SNM. The diagonal of the square can be found from $\sqrt{2}a$ where 'a' is the side of the square. Fig.3 is the basic setup for SNM. Butterfly curve is formed by mirroring the inv1 and inv2. Fig.14 shows the butterfly curve of 6T READ operation.

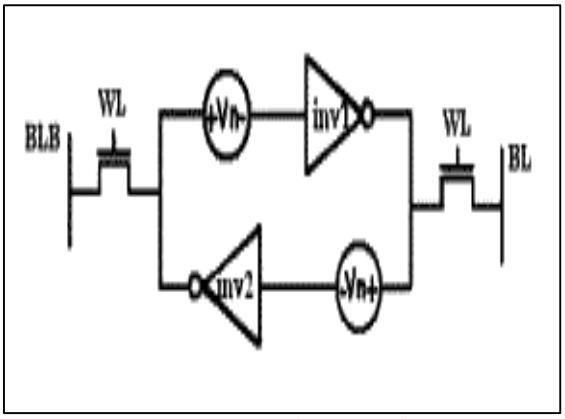


Fig.3The Standard Setup for SNM Definition[5]

## IV. GALEOR SRAM

GALEOR [6-7]technique can be implemented on any circuit by placing the gated leakage transistor in between pull up and output and in between pull down and output as shown in Fig 4. Leakage current is highly reduced due to the stack effect[8] of high threshold voltage gated transistors. During standby mode due to the voltages at x and r both of the leakage transistors will form transistor stacking with pull up and pull down network thus reduces the leakage current. In Fig.4 GLT1 and GLT2 are two high threshold gated transistors. Fig.5 shows the architecture of 10T GALEOR SRAM cell.

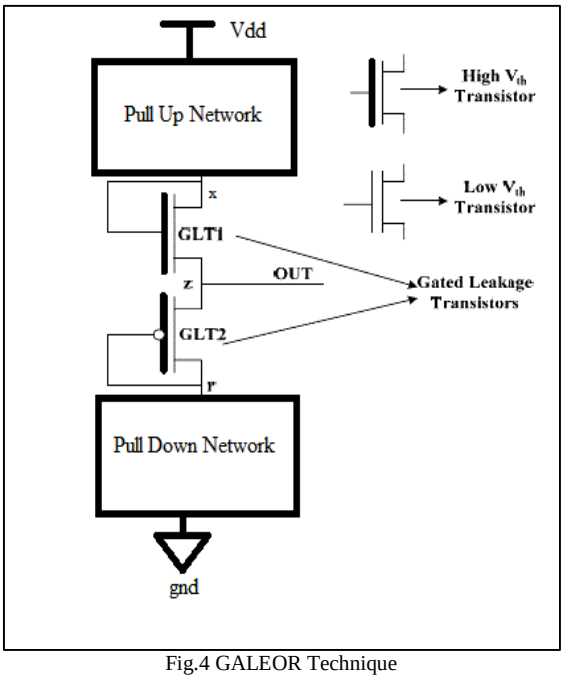


Fig.4 GALEOR Technique

Fig.6 shows the precharge circuit. The other SRAM peripherals write driver circuit and sense amplifier are shown in Fig.7 and Fig.8 respectively.

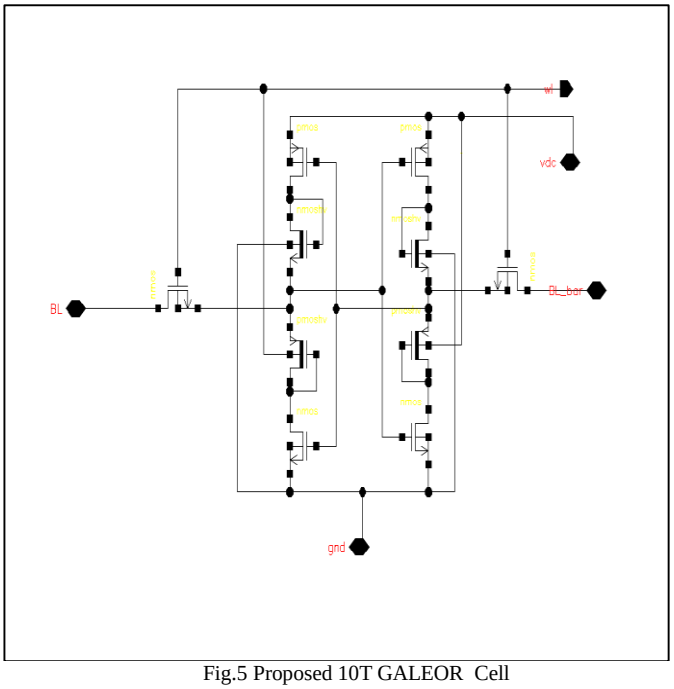


Fig.5 Proposed 10T GALEOR Cell

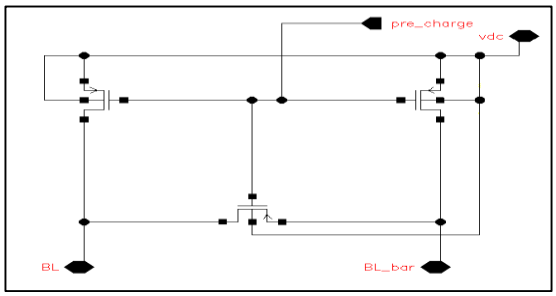


Fig.6 Precharge Circuitry

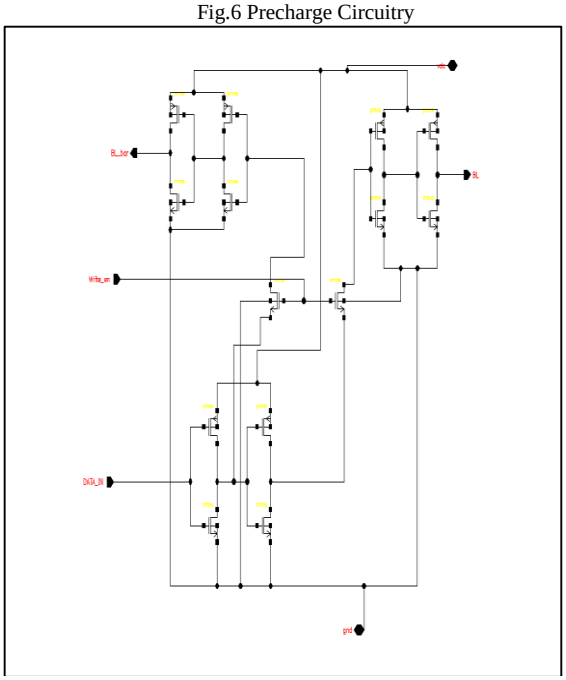

Fig.7 Write Driver Circuitry

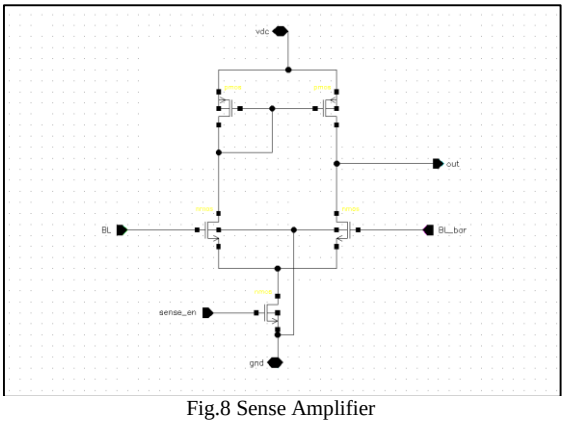


Fig.8 Sense Amplifier

## V. SIMULATION RESULTS

The proposed SRAM cell with peripheral circuitry is simulated in Cadence Virtuoso on 180 nm Standard CMOS process technology. The power supply voltage is 1.8 V. Fig.9 and Fig.10 show the transient analysis of conventional 6T SRAM cell and 10T GALEOR SRAM cell respectively..

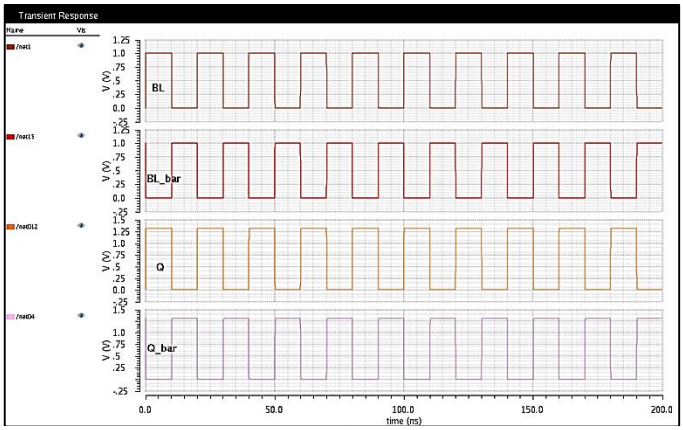


Fig.9 Transient Analysis of Conventional 6T

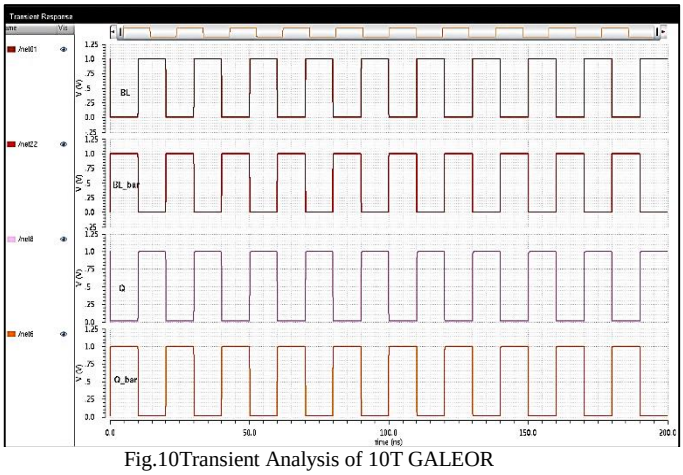


Fig.10Transient Analysis of 10T GALEOR

Fig.11 and Fig.12 show the output of sense amplifier and write driver circuit respectively.1-Bit 10T GALEOR SRAM architecture output is given in Fig.13.

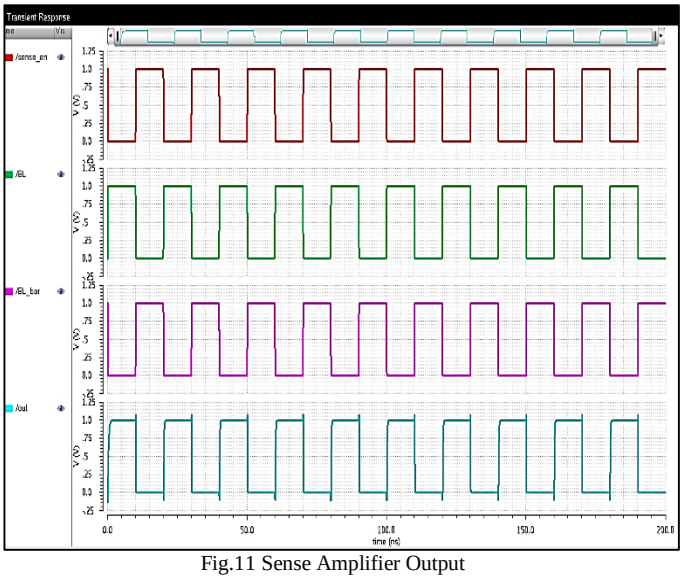


Fig.11 Sense Amplifier Output

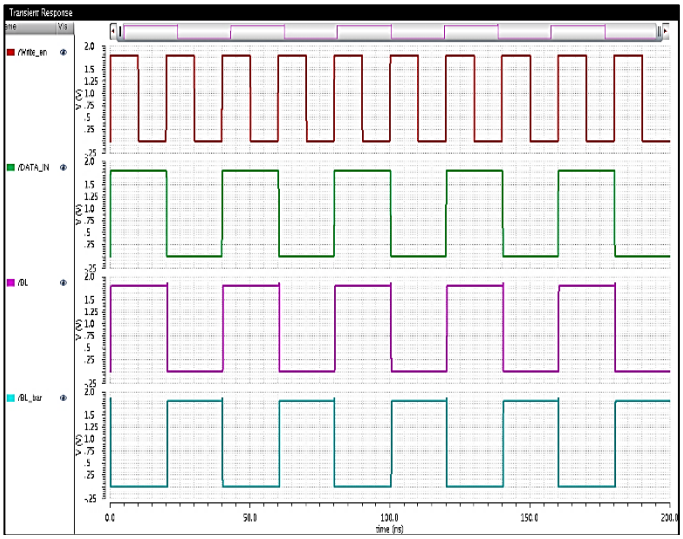


Fig.12 Write Driver Output

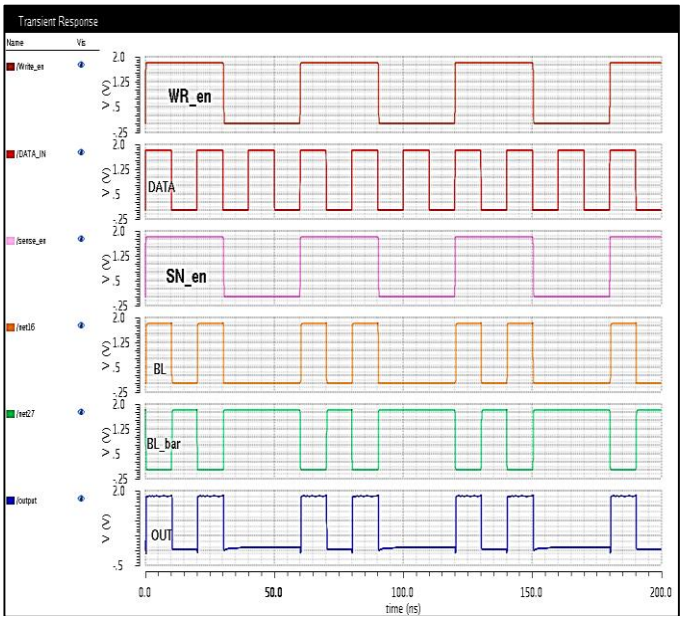


Fig.131 Bit 10T GALEOR SRAM Architecture Output

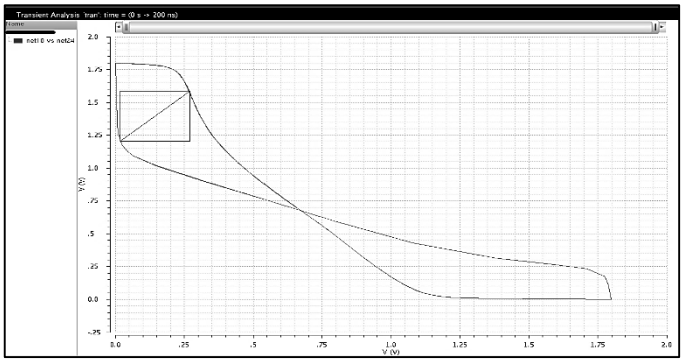

Fig.14 6T READ SNM

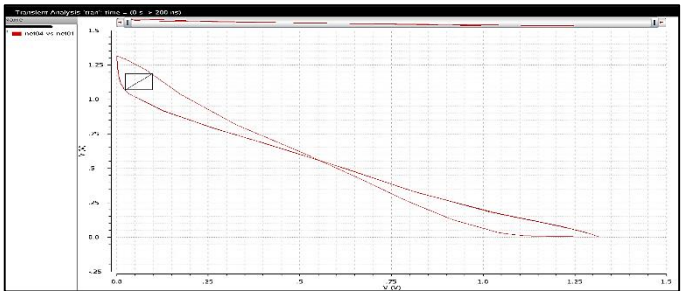

Fig.15 6T WRITE SNM

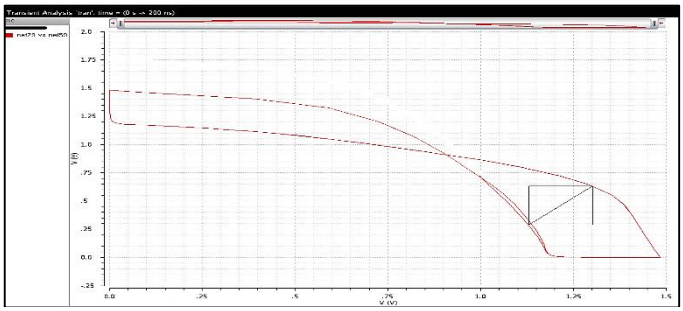

Fig.16 10T GALEOR READ SNM

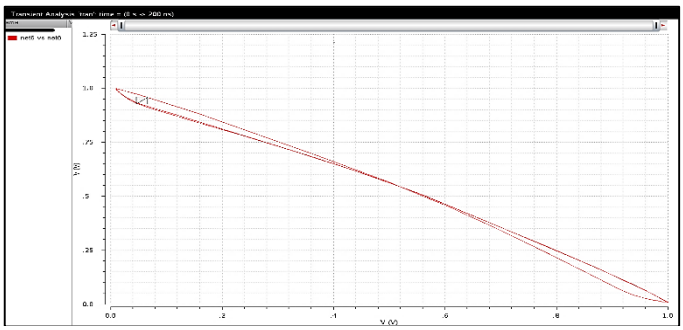

Fig.17 10T GALEOR WRITE SNM

Fig.14 and Fig.15 show the SNM of 6T conventional SRAM for READ and WRITE operation respectively. Fig.16 and Fig.17 show the SNM of 10T GALEOR SRAM for READ and WRITE operation respectively.

TABLE 1.WRITE '0' OPERATION

| SRAM CELL | Leakage power | Delay |
|---|---|---|
| Conventional 6T | 13.02 pW | 11.18 ps |
| 10T GALEOR | 10.5PW | 6.66 ps |

TABLE 2. WRITE '1' OPERATION

| SRAM CELL | Leakage power | Delay |
|---|---|---|
| Conventional 6T | 63.25 pw | 11.16 ps |
| 10T GALEOR | 11.82 pw | 6.67 ps |

TABLE 3. READ '0' OPERATION

| SRAM CELL | Leakage power | Delay |
|---|---|---|
| Conventional 6T | 13.05pW | 35.18ps |
| 10T GALEOR | 10.6PW | 23.32 ps |

TABLE 4. READ '1' OPERATION

| SRAM CELL | Leakage power | Delay |
|---|---|---|
| Conventional 6T | 63.27 pW | 50.16 ps |
| 10T GALEOR | 14.22 pW | 40.6 ps |

TABLE 5.WRITEOPERATION

| Parameter | Conventional 6T | 10T GALEOR |
|---|---|---|
| Power consumption | 205.2 uW | 20.12 uW |
| SNM | 169.7 mV | 70.71 mV |

TABLE 6. READ OPERATION

| Parameter | Conventional 6T | 10T GALEOR |
|---|---|---|
| Power consumption | 205.2 uW | 125.3 uw |
| SNM | 565.6 mV | 424.2 mV |

Table 1 shows that for WRITE 0 operation 10T GALEOR achieves 19.30% and 40.42% reduction in leakage power and delay respectively compared to Conventional 6T SRAM cell. From Table 2 it is seen that using GALEOR technique the proposed design achieves 81.31% leakge power reduction and 33.71% delay reduction for WRITE 1 operation. Table 3 shows that during READ 0 operation GALEOR SRAM exhibits 18.46% reduction in leakage power and 33.88% reduction in delay. Table 4 illustrates that GALEOR SRAM achieves 77.52% reduction in leakage power and 19.05 % reduction in delay during READ 1 operation.

From Table 5 and Table 6 it is seen that 10T GALEOR reduces 90.19% overall WRITE power consumption and also reduces 38.93% READ power consumption respectively. Also Table 5 and Table 6show that using GALEOR WRITE stability and READ stability are decreased by 58.33% and 25% respectively when compared with conventional SRAM.

Fig. 18 ,Fig. 19, Fig.20show the overall power consumption, leakage power and stability comparison between 6T conventional SRAM and 10T GALEOR SRAM for WRITE and READ operatons.Fig.21 shows the layout of 10T GALEOR SRAM.

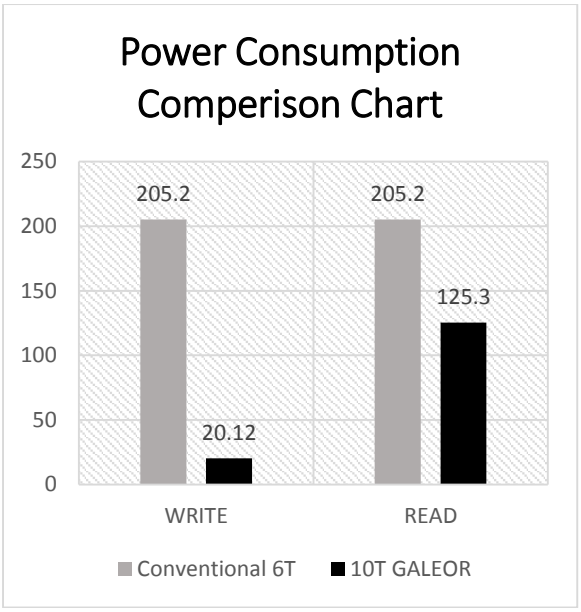


Fig.18 Power Consumption Comparison Between Conventional 6T and 10T GALEOR

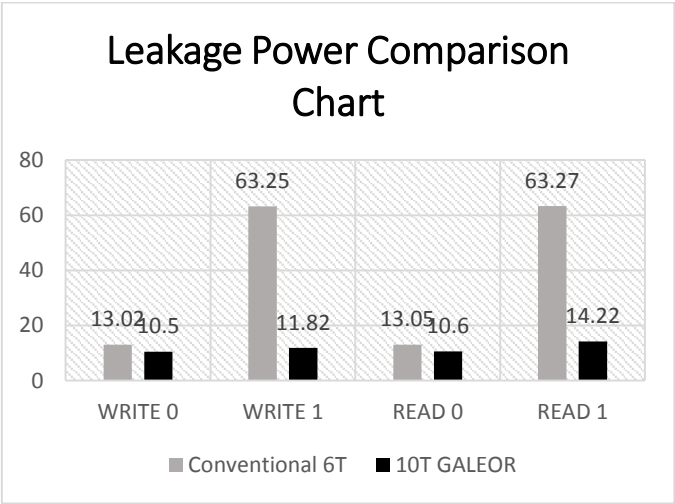


Fig.19 Leakage Power Comparison Between Conventional 6T and 10T GALEOR

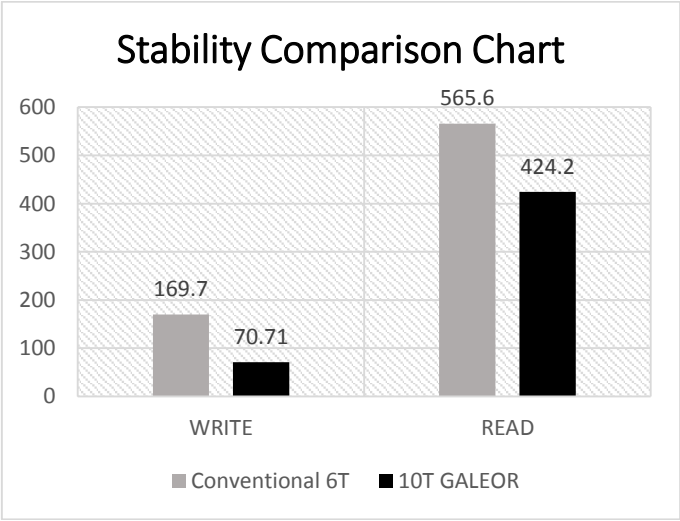


Fig.20Stability Comparison Between Conventional 6T and 10T GALEOR

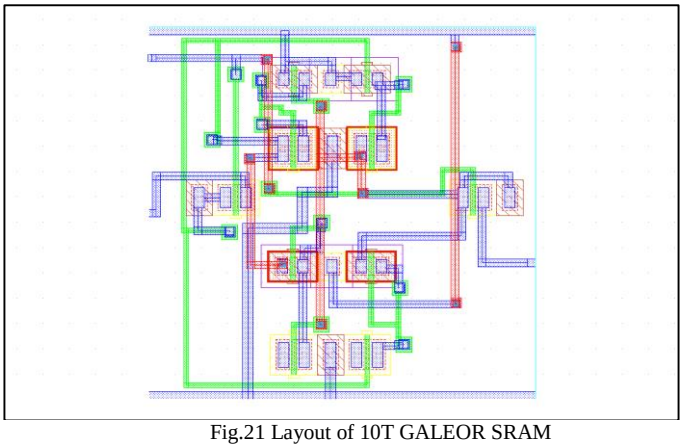

Fig.21 Layout of 10T GALEOR SRAM

## VI. CONCLUSION

Simmulation results show that proposed GALEOR technique efficiently reduces50.30% WRITE leakage power and 47.99% READ leakage power and also reduces 37% WRITE delay and 26.46% READ delay when compared to conventional 6T SRAM. Itis also observed that 10T GALEOR reduces the overall power consumption of the cell but the main drawback is stability. Using 10T GALEOR 58.33% WRITE stability and 25% READ stabilty is decreased in comparison to 6T SRAM.

## VII. ACKNOWLEDGEMENT

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