

# Low Leakage Cell for Ternary Content Addressable Memory: A Tutorial and Review

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**Abstract-** Ternary Content addressable Memory (TCAM) has been an emerging technology for packet forwarding in Network Router. New architecture innovations are reducing power and leakage in TCAM. Beside power, leakages also constitute a major part in TCAM performance. In this paper we review various schemes for low leakage TCAM. The circuits have been implemented in 0.35- $\mu\text{m}$  CMOS technology. The minimum power supply is 1.5 V and the maximum supply current is 11.5  $\mu\text{A}$  for a temperature range of 25°C to 30°C.

**Index Terms-** TCAM Cell, Leakage Current, Power Dissipation

## I. INTRODUCTION

A Content Addressable Memory (CAM) is an outgrowth of random access memory (RAM) technology. Unlike RAMs which access a word based on its address, CAMs access a word based on its contents. A CAM compares an incoming key with all the words in parallel and returns the address of the best match in the array [1]. Therefore CAM is an application specific memory that allows its entire contents to be searched within a single clock cycle. TCAM applications include parametric curve extraction [2], Hough transformation [3], Huffman coding/decoding [4], [5], Lempel-Ziv compression [6]-[9], and image coding [10]. Techniques are described to reduce leakage. Fig.1 gives general view of TCAM architecture. The input to the system is the *search word* that is broadcast onto the search lines to the table of stored data. Each stored word has a matchline that indicates whether the search word and stored word are

identical (the match or are different (a mismatch case, or miss).

## II. TCAM CELL

### 1.1 Leakage Current Component

The leakage current of a deep sub micrometer CMOS transistor consists of three major components: junction tunneling current, subthreshold current and tunneling gate current [11]. In this section, each of these three components is briefly described

**1.1.1 Subthreshold Leakage Current:** Subthreshold leakage is the drain-source current of a transistor when the gate-source voltage is lower than the threshold voltage. The subthreshold leakage is modeled as [11].

$$I_{sub} = A_{sub} \exp\left(\frac{q}{n'kT}(V_{GS} - V_{to} - \lambda'V_{SB} + \eta V_{DS})\right) \times (1 - \exp(-\frac{q}{kT}V_{DS})) \quad (1)$$

Where

$C_{ox}$  = Gate oxide capacitance per unit area

$W$  = Width of the Transistor

$L$  = Effective Length of the transistor

$K$  = Boltzman's Constant

$T$  = Absolute Temperature

$\lambda'$  = Linearized body effect coefficient

$\eta$  = Drain induced barrier Lowering (DIBL)

$\eta'$  = Subthreshold Swing coefficient of the transistor

**1.1.2 Tunneling Gate Leakage Current:** Electron tunneling from the conduction band, which is only significant in the accumulation region, results in direct tunneling gate leakage current in nMOS transistors. In pMOS transistors, hole tunneling from the valence band results in the tunneling gate leakage current. If is used for the gate oxide, pMOS transistors will have about one order of magnitude smaller gate leakage than nMOS transistors. Therefore, one may conclude that the major source of tunneling gate leakage in CMOS circuits is the gate-to channel tunneling current of the ON nMOS transistors which can be modeled as [12]

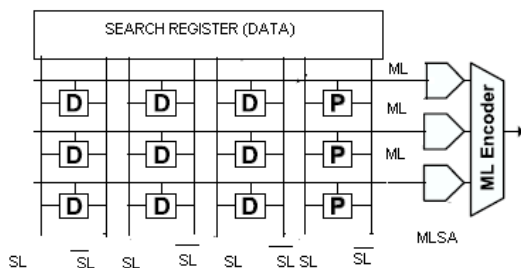


Fig. 1. Schematic of TCAM

$$J_{\text{tunnel}} = \frac{4\pi m^* q}{h^3} (kT)^2 \left(1 + \frac{\gamma kT}{2\sqrt{E_B}}\right) \times \exp\left(\frac{E_F}{KT} - \gamma\sqrt{E_B}\right) \quad (2)$$

Where  $m^*(= 0.19M_0)$  = Electron transfer mass

$M_0$  = Electron Rest Mass

$h$  = plank's Constant

$E_F$  = Fermi Level at the Si/SiO<sub>2</sub> interface

$E_B$  = Height of Barrier

$$\gamma = \frac{4\pi T_{OX} \sqrt{2m_{ox}}}{h} \quad (3)$$

Where  $m_{ox} (= 0.32M_0)$  = Effective Electron Mass in the Oxide

The major contributor to the tunneling gate leakage current in a 6T SRAM cell is the gate-to-channel leakage of the ON pull-down transistor. To weaken this leakage path, one needs to increase the gate-oxide thickness of the pull-down transistors. To reduce other (minor) tunneling gate leakage currents in the SRAM cell, one only needs to increase the gate oxide thickness of the pass transistors, because from the previous discussion, it can be concluded that the gate leakage saving achieved by increasing the oxide thickness of the pMOS transistors would be quite small. Increasing the oxide thickness of a transistor not only increases the threshold voltage, but also reduces the drive current of the transistor. So, the effect of applying this technique to an SRAM cell is an increase in the read/write delay of the cell. This is general equation for leakage in SRAM cell that govern all leakage in TCAM memory.

### 1.2 Conventional Cell 16T TCAM

Fig. 2. shows the leakage paths in a 6T-SRAM-based TCAM cell when the BLs are charged to the 'mask' state ( $BL1 = BL2 = '0'$ ), and minimum-size transistors are used.  $I_{SN}$  and  $I_{SP}$  are NMOS and PMOS subthreshold leakages respectively. NMOS gate leakages are specified by  $I_{GON}$  and  $I_{GOFF}$  for 'ON' and 'OFF' transistors, respectively. Similarly  $I_{GONP}$  and  $I_{GOFFP}$  are PMOS gate leakages.

Leakage Current	Measured Current	Modified Value (fA)
$2I_{SN}$	$2(-4.9087 \text{ nA} + 802.77 \text{ f})$	$-9.815 \text{ e}6 \text{ f}$
$2I_{SP}$	$2(6.0318 \text{ uA} + 3.6117 \text{ u})$	$19.287 \text{ e}9 \text{ f}$
$2I_{GON}$	$2(-1.8082 \text{ fA} + 4.998 \text{ e-}16 \text{ A})$	$-2.6168 \text{ f}$
$6I_{GOFF}$	$6(1.3378 \text{ e-}17 \text{ A} + -2.934 \text{ e-}17 \text{ A})$	$-9.5772 \text{ e-}2 \text{ f}$
$2I_{GONP}$	$2(3.20 \text{ fA} + -1.089 \text{ e-}16 \text{ A})$	$6.1822 \text{ f}$
$2I_{GOFFPK}$	$2(-9.2001 \text{ e-}16 \text{ A} + 3.6729 \text{ e-}16 \text{ A})$	$-5.5272 \text{ e-}1 \text{ f}$

Assuming random data, a TCAM column with shared BLs has the same probability of storing '0', '1' and 'mask'

states. Hence, one-third of the bits will be masked and setting the BLs to the 'mask' state minimizes the subthreshold leakage. For example, if the BLs are set to '0' ( $BL1 = '0'$ ,  $BL2 = '1'$ ), the subthreshold leakage through the access transistors will be  $2I_{SN}$  when the stored value is 'mask'. Typically, the driver transistors (NMOS in the cross-coupled inverters) are sized nearly 2 to 2.5 times larger than the access transistors to perform fast READ operation without disturbing the stored data.

$$I_{6T\_Mask/BLs} = \text{Mask} = 2I_{SN} + 2I_{SP} + 2I_{GON} + 6I_{GOFF} + 2I_{GONP} + 2I_{GOFFPK} \quad (4)$$

Larger transistors result in greater leakages. Since the READ speed is not critical in a TCAM, minimum size transistors can be USED.

This choice also reduces the cell area. Conventional SRAMs also precharge BLs to VDD in order to perform fast READ operation.

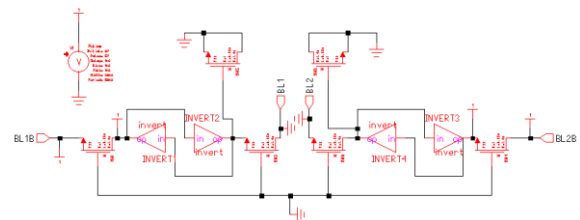


Fig. 2. Conventional TCAM Cell

Leakage Current	Measured Current	Modified Value (fA)
$2I_{SN}$	$2(-4.9087 \text{ nA} + 802.77 \text{ f})$	$-9.815 \text{ e}6 \text{ f}$
$2I_{SP}$	$2(6.0318 \text{ uA} + 3.6117 \text{ u})$	$19.287 \text{ e}9 \text{ f}$
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TABLE I  
LEAKAGE CURRENT OF CONVENTIONAL TCAM

Table I gives leakage current of different transistor of 16 T TCAM Cell. In TCAMs, BLs can be precharged to the state, which results in the minimum leakage. Figure 1 can be used to calculate the leakage current for a 6T-SRAM-based TCAM cell as given by equation (3) for different storage conditions. Below table shows abbreviations

### 1.3 NMOS-Coupled TCAM Cell

Till this point we have studied conventional TCAM cell. In 2006, Nitin and Manoj [13] presented a novel ternary storage cell. In this paper we have review this NMOS and

Next PMOS technique .Each TCAM cell contains two SRAM cells to store the ternary value. These SRAM cells can have four combinations: '00', '01', '10', and '11'. Table II shows leakage current of NMOS coupled TCAM cell

Leakage Current	Measured Current	Modified Value (fA)
$2I_{SN}$	$2(-4.9087 \text{ n+} 802.77\text{f})$	$-9.815 \text{ e}6 \text{ f}$
$2I_{SP}$	$2(6.0318 \text{ u} + 3.6117 \text{ u})$	$19.287 \text{ e}9 \text{ f}$
$2I_{GON}$	$2(-1.8082 \text{ f} + 4.998 \text{ e-}16 \text{ A})$	$-2.6168 \text{ f}$
$6I_{GOFF}$	$6(1.3378 \text{ e-}17 \text{ A} + -2.934 \text{ e-}17 \text{ A})$	$-9.5772 \text{ e-}2 \text{ f}$
$2I_{GONP}$	$2(3.20 \text{ f} + -1.089 \text{ e-}16 \text{ A})$	$6.1822 \text{ f}$
$2I_{GOFFPK}$	$2(-9.2001 \text{ e-}16 \text{ A} + 3.6729 \text{ e-}16 \text{ A})$	$-5.5272 \text{ e-}1 \text{ f}$

TABLE II  
LEAKAGE AT NMOS COUPLED TCAM

. However, only three out of them are used for the ternary value, and the "unused" state (typically '11') is forbidden. This ternary storage cell trades this "unused" state for a smaller leakage by coupling two 5T-SRAM cells and eliminating a subthreshold leakage path [13]. Fig. 3 shows the leakage paths of the NMOS-coupled (NC) ternary storage cell that connects two 5T-SRAM cells . For storing a ternary '0' or '1', one of the storage nodes (connected to the access transistors) is held at logic '0' through the coupling NMOS transistor. Likely when the 'mask' state is stored, both coupling NMOS transistors are 'OFF'. Note that when both coupling NMOS transistors are 'ON', the cell is not stable. Hence, this cell can store only three states. It can be noticed in Figure 3. that the proposed cell can store only three states because the coupling does not allow the "unused" state. The total leakage current for an NC-TCAM cell (with BLs = 'mask') can be given by equation (5)

$$I_{NC\_MASK/BLs=Mask} = 2I_{SN} + 2I_{SP} + 2I_{GON} + 6I_{GOFF} + 2I_{GONP} + 2I_{GOFFPK} \quad (6)$$

Thus, it will exhibit less leakage than the 5TSRAM- based cell only if condition (7) is satisfied:

$$0.67I_{SN} > 3.33I_{GOFF} \rightarrow I_{SN} > 5I_{GOFF} \quad (7)$$

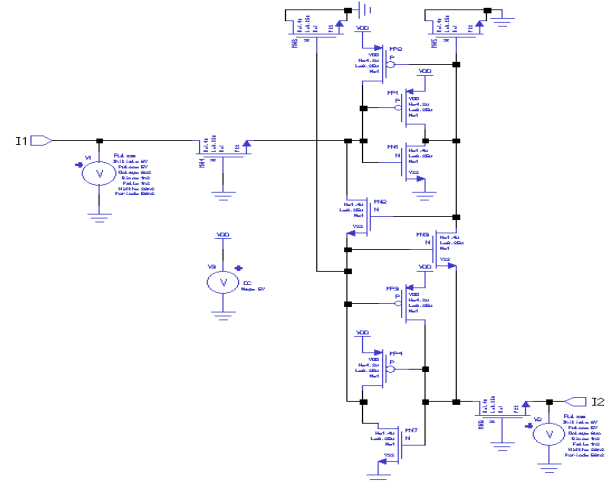


Fig. 3. NMOS Coupled TCAM Cell

#### 1.4 P-MOS Coupled TCAM Cell

The coupling between the two 5T-SRAM cells can also be obtained by PMOS transistors. Fig. 4. shows the leakage paths of the PMOS-coupled (PC) TCAM cell. Similar to the NC-TCAM cell, one of the coupling PMOS transistors does not consume subthreshold leakage under '0' and '1' conditions. Thus, it will also exhibit smaller leakage than the 5T-SRAM-based cell if the subthreshold leakage is more than the gate leakage. The total leakage current for a PC-TCAM cell (with BLs set to the 'mask' condition) can be given by equation (6).

$$I_{PC\_MASK/BLs=Mask} = 2I_{SN} + 2I_{SP} + 2I_{GON} + 2I_{GOFF} + 2I_{GONP} + 2I_{GOFFPK} \quad (8)$$

Similar to the 5T-SRAM-based cell, this BL precharge condition reduces both subthreshold and gate leakages. The PC-TCAM cell will consume less leakage than the 6T-SRAM-based cell only if condition (9) is satisfied.

$$0.67I_{SP} > 0.67I_{GOFFPK} \rightarrow I_{SP} > I_{GOFFPK} \quad (9)$$

Similarly, the PC-TCAM cell will consume less leakage than the NC-TCAM cell (when BLs = 'mask') only if condition (10) is satisfied.

$$0.67I_{SP} + 3.33I_{GOFF} > 0.67I_{SN} + 0.67I_{GOFFPK} \rightarrow I_{SP} + 5I_{GOFF} > I_{SN} + I_{GOFFPK} \quad (10)$$

Table III gives leakage current of PMOS coupled TCAM cell

Leakage Current	Measured Current	Modified Value (fA)
$2I_{SN}$	$2(0 + 91.328 \text{ n})$	$182.64 \text{ e}6 \text{ f}$
$2I_{SP}$	$2(-526.3173 \text{ f} + -9.481 \text{ e-}18 \text{ A})$	$-1.052 \text{ e-}3 \text{ f}$
$2I_{GON}$	$2(0 + 2.20803 \text{ e-}17 \text{ A})$	$4.41606 \text{ e-}2 \text{ f}$
$2I_{GOFF}$	$2(0 + 1.4698 \text{ e-}18 \text{ A})$	$2.9392 \text{ e-}3 \text{ f}$
$2I_{GONP}$	$2(0 + -2.4130 \text{ e-}18 \text{ A})$	$4.82 \text{ e-}3 \text{ f}$
$2I_{GOFFPK}$	$2(-5.9084 \text{ e-}17 \text{ A} + 5.1861 \text{ e-}17 \text{ A})$	$-14.4 \text{ e-}3 \text{ f}$

TABLE III  
LEAKAGE AT PMOS COUPLED TCAM

If the gate leakage is comparable to the subthreshold leakage ( $I_{SN} < 3I_{GOFF}$ ) and BLs of NCTCAM are at GND, the PC-TCAM cell will consume less leakage than the NC-TCAM cell if condition (10) is satisfied.

$$0.67I_{SP} + 1.33I_{GOFF} > 0.67I_{GOFFPK} \rightarrow I_{SP} + 2I_{GOFF} > I_{GOFFPK} \quad (11)$$

Most CMOS processes will satisfy condition (8) because the PMOS subthreshold leakage and the NMOS gate leakage both are typically larger than the PMOS gate leakage.

The leakages of the above cells (when BLs = 'mask') are summarized in Table IV. It can be shown that that the 6T-SRAM-based cell always consumes more leakage than the other three cells

Cell	Stored Value	Subthreshold Leakage	NMOS Gate Leakage	PMOS Gate Leakage
6T	×	$2I_{SN} + 2I_{SP}$	$2I_{GON} + 6I_{GOFF}$	$2I_{GONP} + 2I_{GOFFPK}$
PC	×	$2I_{SN} + 2I_{SP}$	$2I_{GON} + 2I_{GOFF}$	$2I_{GONP} + 2I_{GOFFPK}$
NC	×	$2I_{SN} + 2I_{SP}$	$2I_{GON} + 6I_{GOFF}$	$2I_{GONP} + 2I_{GOFFPK}$

TABLE IV  
LEAKAGE CURRENT OF TCAM WHEN BITLINE=MASK

### III SIMULATION RESULT

We simulated the above TCAM cells using 0.35  $\mu\text{m}$  technology. Figure 5 shows the leakage of different TCAM cells at 0.35 $\mu\text{m}$  CMOS technologies. It can be noticed that the magnitudes of different leakage components are related as follows:

$$I_{SN} > I_{SP} \gg I_{GON} > I_{GOFF} \gg I_{GONP} > I_{GOFFPK}$$

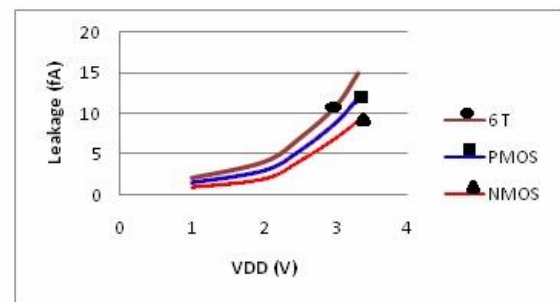


Fig. 5. TCAM Cell Leakage for 35 nm CMOS technology

In this writing 1 was more difficult than writing 0 as it is tough to transfer 1 from NMOS transistor. The conventional 16 transistor TCAM area consume most area and hence most power dissipation. Newer approach like NMOS and PMOS use less area as number of transistor is less as well less power dissipation.

### IV CONCLUSION

In this work we have studied and analyzed TCAM circuits with an emphasis on high capacity RAM. We have simulated conventional 16 transistor TCAM cell, NMOS coupled TCAM cell and PMOS coupled TCAM cell for low leakage and less area. Simulation results shows a reduction of up to 38% leakage reduction in NMOS and PMOS coupled TCAM cell as compared to conventional TCAM cell. The efficiency of PMOS coupled TCAM cell is best in all category

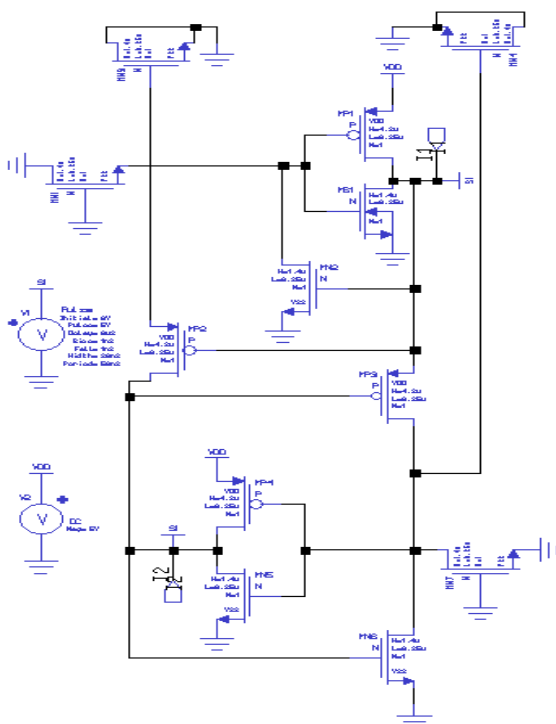


Fig . 4. PMOS Coupled TCAM Cell

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