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Logic Structure Reduction Scheme for FinFET Based TSPC Flip Flop

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Abstract: **This paper discusses about a low power TSPC flip-flop comprising 17 transistors and its implementation. This design follows a master slave type logic structure & some features a hybrid logic design which comprises static CMOS logic & complementary pass transistor logic. Here, logic structure reduction scheme is applied to reduce the count of transistors for aiming at high power & delay performance. In spite of its circuit simplicity, there is no internal nodes left floating while operation which avoids leakage power consumption. The virtual *V*DD design technique is used here which facilitates a faster state transition in the slave part of latch, which is devised to enhance timing performance. The implementation here is done such that transistor sizes are optimized with respect to the power delay product. A TSMC-Taiwan Semiconductor Manufacturing Company 18-nm finFET process is selected as the implementation technology. In this paper five FF designs were considered & their performance levels of were compared. The timing parameters of each Flip-Flop were first characterized to find setup time, hold time, clock to Q delay & data to Q delay. Compared with the conventional TGFF design, the Power Delay Product improvement in the proposed design was found to be 78.67%. Further the bidirectional shift register was implemented using the proposed D flip-flop.**

Index terms – FF - flip-flop, TGFF - transmission gate-based flip-flop

I. INTRODUCTION

Flip-flops are the basic storage element in any of the digital systems. Flip flop is used as registers, & for stack operation, shifting, counting operations. Power consumption of flip-flops in any digital systems with clocking requires 20%-40% of total system power. The design of FF mainly focuses on power consumption, speed & area. Which becomes the critical aspect while designing flip-flop. The conventional flip-flop using transmission gate, SRFF, adaptive coupling flip-flop is reviewed to be fully static designs & topologically compressed flip-flop is been introduced & Which leads to the use of logic structure scheme & implements LRFF [1]. Transmission gate flip-flop is widely used but the drawback is high clock loading & complementary signals is required and even when there less data switching activity the dynamic power is present. TSPC flip-flop is implemented with the aim of lowering clock loading problem. Which can be implemented using simplification of circuit. Cross coupled SR latches are used instead of TGFF to support single phase operations. To reduce the circuit complexity TCFF is used [2]-[4]. In this work the LRFF proposed in [1] is reviewed & the dynamic switching activity is reduced using logic structure reduction scheme.

The section II follows review of the existing flip-flop designs. Section III explains the proposed D flip-flop. The section IV gives the results and section V draws conclusion.

II. EXISTING FLIP-FLOP DESIGNS

Taking few existing flip-flops as base for comparison & the proposed design is implemented. TGFF master slave flip-flop is shown in the figure 1a, which shows that it comprises of two TG-based latch designs. Inverter I1, I2 is used for the generation of complementary clock signals. The TGFF design suffers from high capacitive clock loading problem, where the 12 transistors are driven by clock signal. Which indicates continuous power consumption even when the input remains static. The same complication is also occurred in conventional SRFF designs as shown in figure 1b. The problem of power consumption is reduced by implementing adaptive coupling technique & topologically compressed scheme have been proposed. The ac FF design is shown in figure 1c. The TSPC operation is achieved using differential latch structure which uses pass transistor logic. The n-type or p-type transistors are replaced instead of transmission gates. A pair of level restoring circuits is used which is placed into cross coupled path of master part of the latch to overcome by impact of process variations. Now only two pMOS & nMOS is driven by the clock signal, & the number of transistors is reduced to 22.

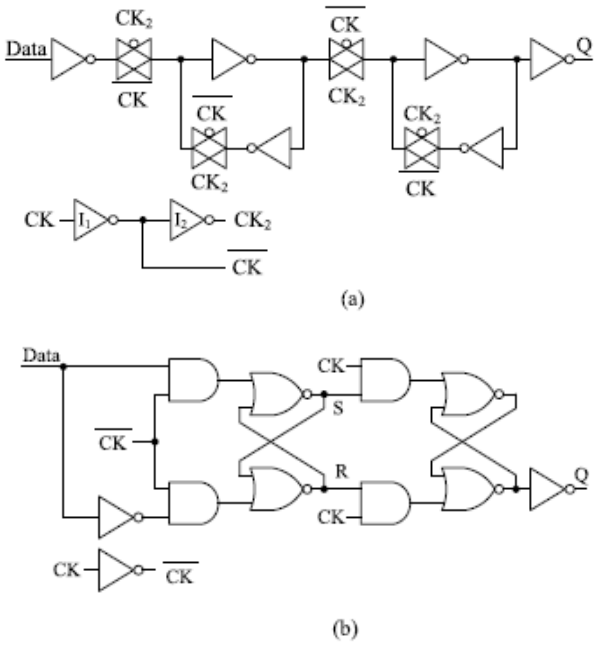

Figure 1: Conventionally fully static FF designs

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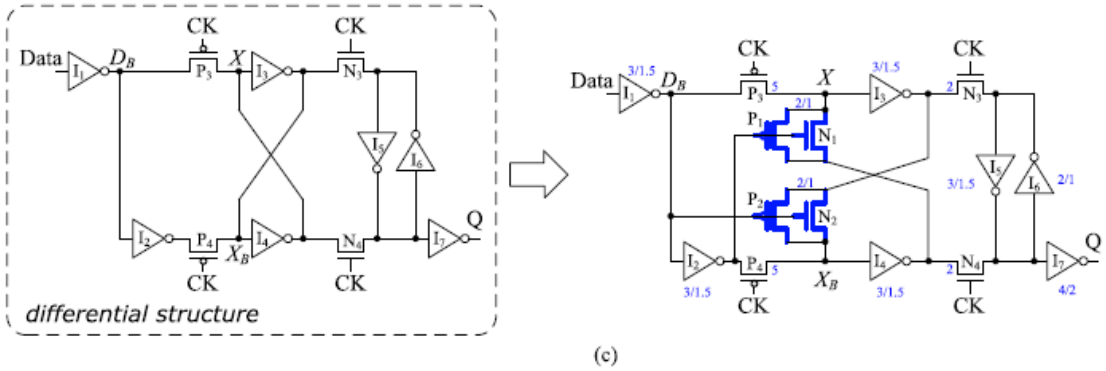

Figure 1: Conventionally fully static FF designs

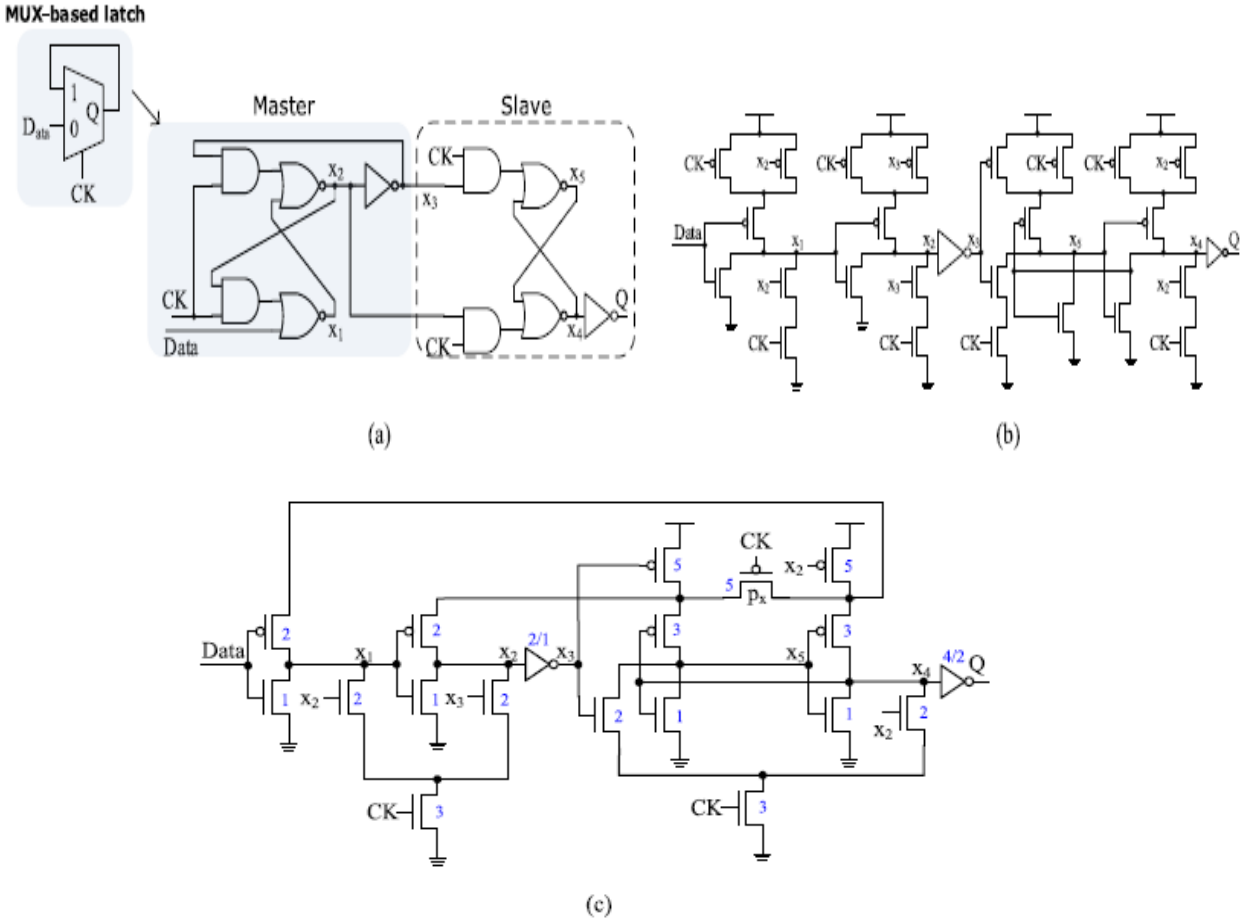

Figure 2: (a) logic schematic (b) MOS circuit schematic (28 transistors) (c) circuit optimization (21 transistors) using topologically compressed circuit scheme.

The power consumption can be lowered significantly by lighter clock loading with the help of circuit simplification of Flip-Flop design. In this design power saving is eliminated due to data contention problem in slave part of the latch which will be deteriorated as data switching activity increases. Setup time will be longer if we use level restoring circuit pair. The design is prone to power leakage problem when certain internal node combinations occur. Set Reset latch based true single phase clocking flip-flop design called as TCFF- Topologically Compressed FF is shown in figure 2, which is obtained from topologically compressed scheme. Topologically compressed flip-flop logic schematic is shown in figure 2a, where the MUX-based latch is used for its implementation and the MOS circuit schematic is shown in figure 2b which comprises of 28 transistors. The circuit in figure 2b can be optimized further sharing the terminals in circuit. For the pull-down logic, one clock-controlled n-type transistor can be shared by two of the discharging paths. For the pull up logic, 4 p-type transistors connected to V_{DD} are used, where two p type transistor pairs can be reduced. Here the virtual V_{DD} is the p type transistor which is turned ON. And the resultant circuit is shown in figure 2c where the 28 transistors is reduced to 21 transistors.

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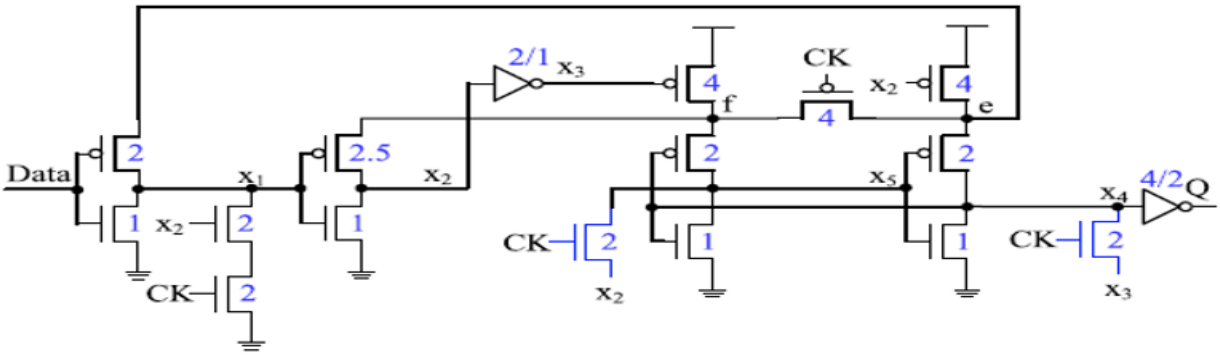

Figure 3: Logic structure Reduction Flip-Flop design

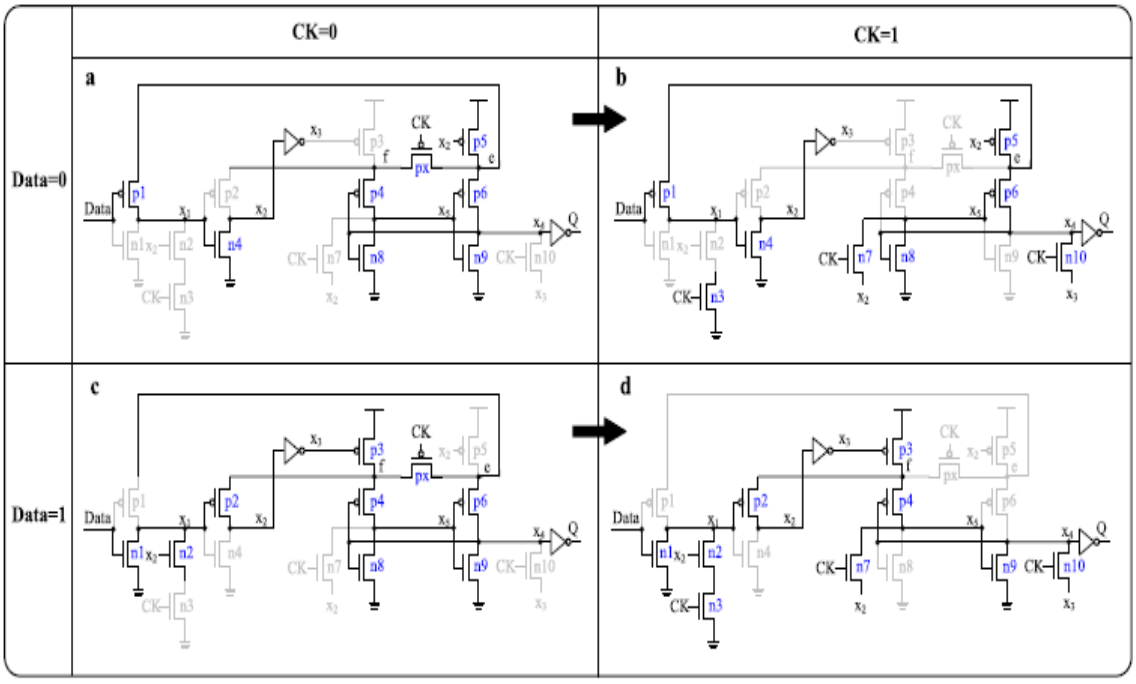

Figure 4: Process of data latching in Logic structure Reduction Flip Flop design

Figure 3 shows the LRFF with 19 transistors. The node e, f is called virtual node which is always high virtually high because node x3, x2 is complementary which ensures that when x3 is low, pMOS transistor is ON & node f is high & similarly when x2 is low the node e is high. When clock is zero the data is passed to node x2 which is master latch and when the clock is high the data is passed to the slave latch and output is obtained. We can observe that data is passed to the slave latch through pass transistors when clock is high. Figure 4 shows the data latching process. Figure 4a, 4b explains data=0 latching process and figure 4c, 4d shows the data=1 latching process. The transistors which are in grey colour indicates that the transistors are turned off. The transistor p_x is called the bridging transistor. Which keeps the node e and f high when clock is low.

III PROPOSED FF DESIGN

The design proposed, is named as logic structure reduction flip -flop. Which can be considered as enhancement of topologically compressed flip-flop. The proposed design is achieved by incorporating various optimization measures. Logic structure reduction for shorter setup time is the first measure, and the second one is for lowering power consumption by circuit simplification, and the third one is floating node case is eliminated to avoid static power leakage problem. Figure 5 shows the circuit of proposed flip flop which uses 17 transistors for its circuit operation. The transistors PM2, PM3, NM2, NM3 forms the bistable latch in slave circuit. When clock is low, master is active and slave is inactive and node x_2=0, x_3=1 which switches on PM5 and PM0 source terminal is connected to V_{DD}.

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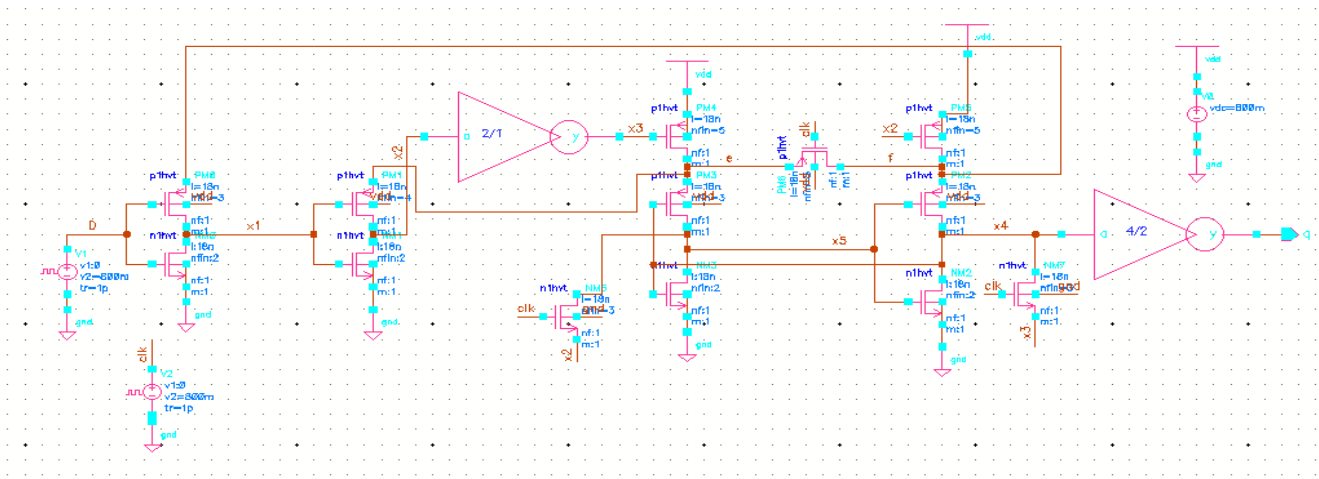

Figure 5: schematic of proposed TSPC flip flop.

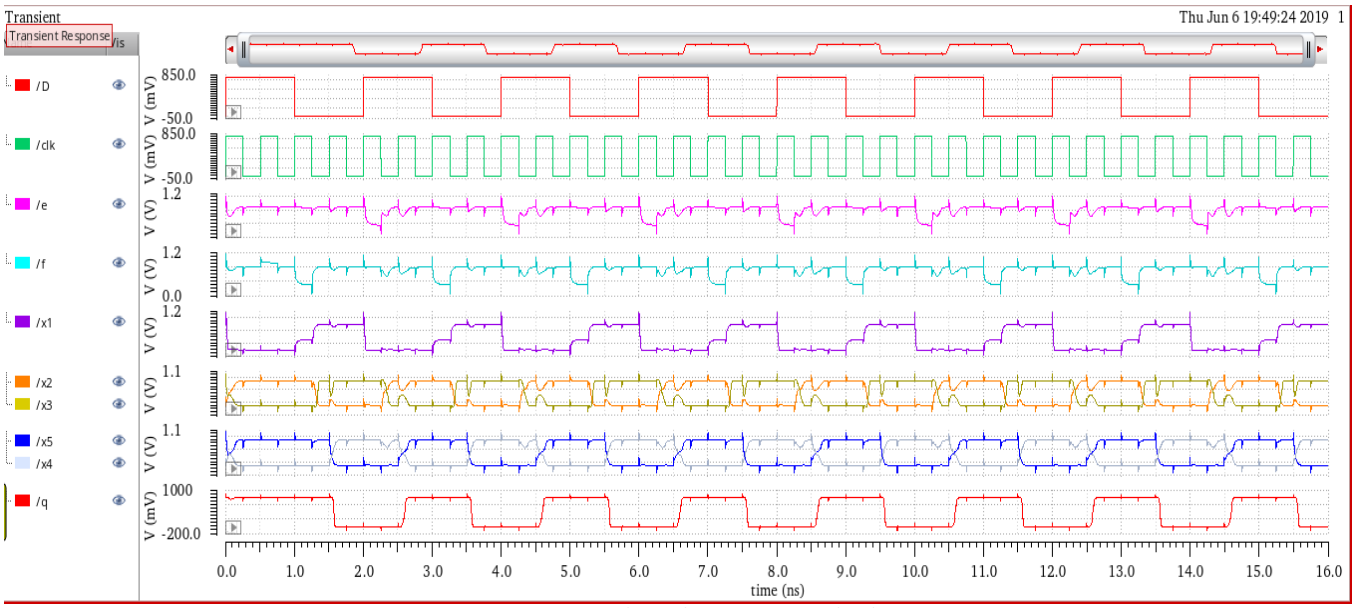

Figure 6: Output waveform of proposed TSPC flip flop.

And when clock is high the data at node x_2, x_3 is passed through slave latch. Any data changes at input is not affected by master when clock is high by ensuring that transistor PM6 is turned OFF and source terminal of PM1 is disconnected from V_{DD}. The operation of the proposed circuit ensures that there is no internal floating node in the circuit. Figure 6 shows the simulation waveform of LRFF using 17 transistors. All internal nodes are depicted in the figure 6. The node e, f is high when x_2 or x_3 is zero. When clk=1 node e and f are disconnected from V_{DD} and output is pulled down because input changes. However, this node does not pose a problem because those nodes are not used to determine the output of slave latch. The waveform shown is with 2GHz clock rate. Thus, adding a protection circuit to prevent the occurrence of soft logical errors is essential [6]. The remedy for transistor stacking has been presented in [10],[11].

IV RESULTS

The study of the existing flip-flops and proposed flip-flops have been done and their static timing analysis and power analysis is shown in table 1. Where we can observe the setup time, hold time, average power, clock to Q delay, data to Q delay, and power delay product of each circuit. The proposed design can balance simultaneously power and speed performance for good results. In terms of complexity of circuit, the proposed LRFF uses a smaller number of transistors and which impacts the area. Here the target frequency was taken as 2GHz to find the average power for the calculation of power delay product.

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TABLE 1 Feature comparison of flip-flop at 2GHz/0.8 V

Architecture	TGFF	SRFF	ACFF	LRFF	PROPOSED
Number of transistors	24	30	22	19	17
Setup (ps)	81.1023	109.43	149.13	129.55	119.126
Hold (ps)	-79.87	-109.43	-149.12	-129.55	-19.12
C_Q (ps)	272.09	342.3	283.99	271.8	272.3
D_Q (ps)	311.8	516.64	450.64	421.59	404.21
Avg power (µW)	5.514	6.661	1.505	1.479	1.175
PDP_{C-Q} (fJ)	1.5	2.28	0.427	0.4019	0.3199
PDP_{D-Q} (fJ)	1.719	3.44	0.678	0.623	0.4749

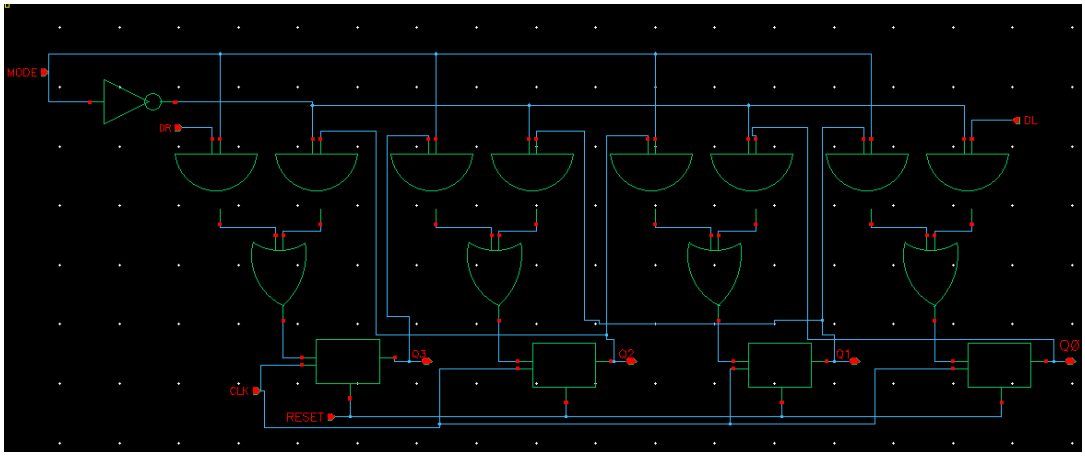

Figure 7: Bi-directional shift register

The designed flip-flop is used as an application to build 4-bit bidirectional shift register. The schematic is shown in figure 7. The Bi-directional register is shown in Figure 7. The bi-directional register has five inputs which are mode, DR, DL, RESET, CLK, and four outputs which are Q_0, Q_1, Q_2, Q_3.

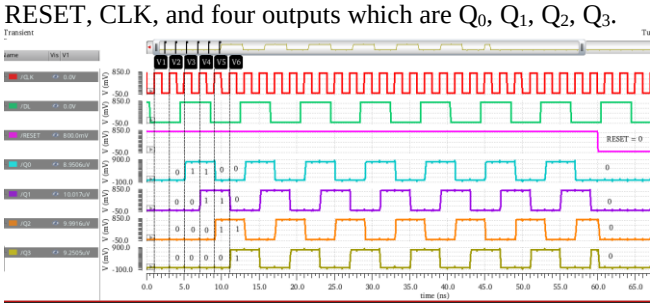

Figure 8: left shift waveform of shift register

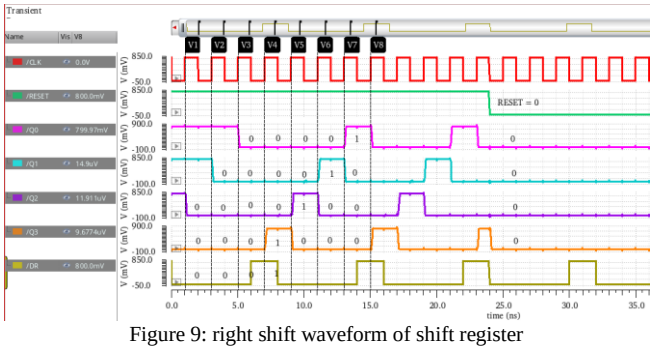

Figure 9: right shift waveform of shift register

When the data has to be shifted left the mode should be made logic '0' and for right shift operation mode should be made logic '1'. To perform left shift the data has to be fed from MSB and for right shift data has to be fed from LSB.

Figure 8 shows the left shift operation of data 0110, we can observe that one-bit left shift causes the data to be multiplied by two and its 1100. Similarly, as shown in figure 9 right shift operation of data 1000 is shown. The right shift by one bit causes the data to be divided by two and given data results into 0100.

V CONCLUSION

In this paper, low power 17 transistor TSPC flip-flop is designed using logic structure reduction scheme for the existing 19 transistor LRFF. Considerable simulations were performed and various performance parameters such as power consumption, power delay product, setup time, and clock to Q delays were evaluated. The proposed flip-flop PDP improvement was found to be 78.67%. Which proves the power efficiency of proposed flip-flop.

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