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Logic State Analyzer for Vibration Analysis

Swati D. Ambade
Department of Electronics Engineering, S.R.C.O.E.M. Nagpur

Prof. M. B. Damle
Department of Electronics Engineering, S.R.C.O.E.M. Nagpur

Abstract

The proposed Logic State Analyzer is a portable device that monitors the fragments and air shock waves emitted by any explosive device. The digital signals are stored in a memory. The stored data can be used for further analysis. This device can be used in remote areas where human interference is not possible. The Logic State Analyzer fills the void between expensive analyzers with many channels, and inexpensive analyzers with few channels and limited sample rates. The design of the LSA presented in this paper can be effectively used in remote areas. It has 32 channels and can login a large amount of data of 80MB in time period of 1 second. It is also having very high sampling rate of 20M samples/sec of width 32 bits. It is also interfaced with PC. After explosion test the data can be transferred to PC and displayed in graphical format and can be further analyzed. It uses FPGA for high speed data acquisition and stores in PSRAM. It also uses a micro controller (AVR) for transferring the test data into SD card and later transferring it to PC via serial interface.

Keywords – Logic State Analyzer, FPGA, AVR, PSRAM,

I. INTRODUCTION

Ongoing succession of states occurring in a collection of digital signals is monitored by a logic state analyzer which stores either all such states or a selected subset thereof meeting certain qualification criteria. The memory into which the states are stored is updated with oldest stored states being overwritten as the newest states are stored, the collectivity of which may be termed a captured trace. The utility of such a trace in a logic state analyzer is enhanced by allowing the user to divide the collection of digital signals into groups of related signals, assign symbolic labels to the groups, and indicate a radix for each group. Such division, assignment and indication may be termed a format specification.

1.1. GOALS

The proposed digital logic state analyzer is used to measure the intensity of mechanical wave in a time period of 1 second with a sampling rate of 50 nanosecond. In this logging period we are logging data of 80 MB. (32 bit*20MHz = 80M samples/sec).

The instrument must be portable and have battery backup. It must have storage capacity of at least 10 tests in non volatile memory. Also it should have the capability to interface with PC via serial communication.

1.2. SYSTEM DISCRIPTION

In this project logic state analyzer (LSA), there are two main parts and we require two main platforms which are FPGA for data logging portion and Micro-controller (AVR) for co-ordination and communication with PC or backup memory. In data login part the two main hard wares interfaced are

FPGA and external PSRAM and in micro-controller portion, the controller used is AVR for storing large data and it is also interfaced with RTC, keyboard, LCD, SD card, PC for viewing the result in graphical format. This LSA starts recording the data when it receives any start input pulse. Switches are used as sensors. When any mechanical wave or fragment is received switches are pressed and FPGA starts login the
data and when the switches are released stops login the data. During this process the logic state of the FPGA changes either from high to low or low to high.

We need FPGA for performing the sampling at a higher rate and storing the high speed data into the non volatile memory as this cannot be done by micro controller.

We need micro controller for interfacing with LCD, keyboard, RTC, memory, PC as it is very complex to interface with FPGA. Also if there are 10 test data and we want to study a particular test data then we need controlling logic for this and so micro controller is used.

II. BLOCK DIAGRAM OF PROPOSED LSA

Fig.1 shows Logic state analyzer is used to measure the intensity of air shock wave in a time period of 1 second with a sampling rate of 50 nsec and login data of 80 MB. The micro controller is interfaced with LCD, keyboard, RTC, PC and memory.

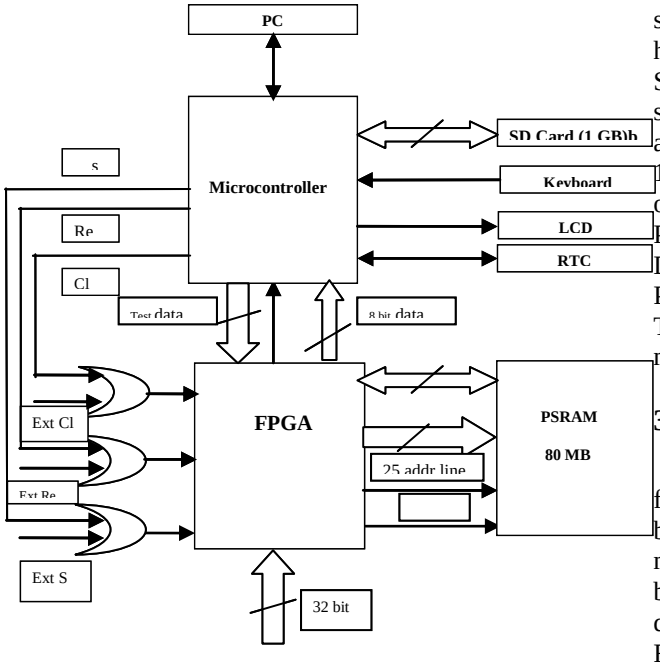


Figure1. Block Diagram of Proposed LSA

Initially after power on FPGA is in reset state. A menu will be displayed on LCD like login mode, test mode, RTC, view data from PC, Retrieve data. When login mode is selected micro controller releases FPGA. After this if FPGA receives any input signal then it starts login the data. When the logic state changes the FPGA stops login the data. FPGA stores this data in PSRAM. FPGA reads the data from memory and sends 1 byte data to the micro controller with each clock pulse. The micro controller stores the data in SD card. If test mode is selected then FPGA will be self tested. If RTC option is chosen then we can set the time and date of received data. We can view the data in graphical format from PC if we choose the view data from PC option. If retrieve data option is chosen then micro controller reads the stored data from memory.

III. THE DATA LOGIN PORTION (FPGA & PSRAM)

In data login portion , two hardware's used that are field programmable gate array (FPGA) of Altera Cyclone II and Pseudo Static Random access memory (PSRAM) which is of 80 Megabytes in sized. Language used for coding of data login portion is verilog hard ware description language.[7] For simulation of data login portion, Modelsim platform is used and for synthesis Quartus II 10.1 web edition platform is used.

3.1. PSRAM (Pseudo Static Random Access Memory):-

PSRAM is a dynamic RAM with built-in refresh mechanism and address-control. It is behave similarly to static RAM (SRAM).It combines the high density of DRAM with the ease of use of SRAM. Pseudo Static RAM typically features high speed, density and inexpensive cost structure. The access time of PSRAM is 70 ns and DPD current is 10µA. It has UB/LB byte control and wide operating temperature range is –30 to +85°C. PSRAM also has low power features which are Deep Power-Down (DPD) refresh mechanism, Partial Array Refresh (PAR) mechanism and Temperature Compensated Refresh (TCR) mechanism [6].

3.2. FPGA CHIP of Altera Cyclone II

Field Programmable means that the FPGA's function is defined by a user's program rather than by the manufacturer of the device. A small device may be present to allow the designers to change a board's glue logic more easily during product development and testing. There are various types FPGA Manufactures such as Xilinx, Altera and Lattice etc. From these manufactures, here we used Altera family which has very low cost, fast interfaces to external RAM. It is Seven member family offers densities ranging from 4000 to 68416 logic elements. It provides clock rates up to 260 MHz[5].

IV. INTERNAL BLOCK DIAGRAM OF PROPOSED LOGIC STATE ANALYZER

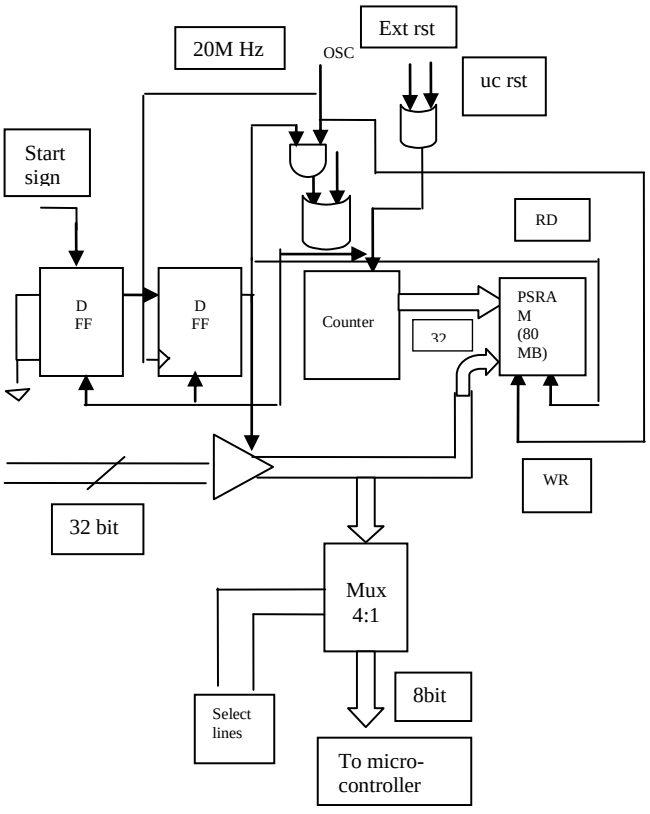
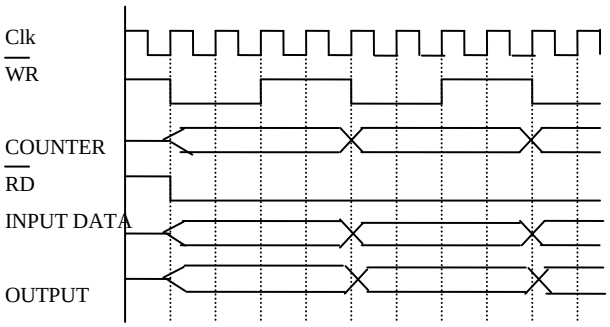


Figure 2. Internal design of Proposed LSA

4.1. TIMING DIAGRAM:-



V. THE MICRO-CONTROLLER SECTION FOR USER INTERFACE

The hard wares used in microcontroller section are 8-bit Micro-controller (AVR 128), Serial flash memory (80 MB), LCD, Keyboard, RTC and PC. Language used for coding purposed are Embedded C and VC++. Platforms used for microcontroller are AVR Studio 4.0, Microsoft visual studio 6.0(for serial communication)

5.1. ADVANTAGES OF ATMEL AVR

The very lowest-price microcontroller available from any manufacturer is the $0.54 Atmel AVR ATtiny11 6 MHz FLASH (same price for 8 pin DIP and 8 pin SOIC). Speed: Not only are most AVR capable of 20MHz (even really cheap ones like the ATtiny25/45/85 and ATmega48), but they actually run at near 20 MIPS; the PIC chips of higher price (for example, PIC16F88) only run at 5 MHz with a 20 MHz oscillator frequency. In addition, with the better addressing modes and registers of the AVR, most operation can be done in only one instruction, where it often takes more than one instruction to do the same thing on a PIC. One big advantage of AVRs is that they are supported by the GNU Compiler Collection (GCC). AVR 128 is a High-performance, Low-power AVR 8-bit Microcontroller. It has Advanced RISC Architecture i.e. 133 Powerful Instructions Most Single Clock Cycle Execution, 32 x 8 General Purpose Working Registers + Peripheral Control Registers, High Endurance Non-volatile Memory segments i.e. 128K Bytes of In-System Self-programmable Flash program memory, 4K Bytes EEPROM, 4K Bytes Internal SRAM also having Optional External Memory Space (OEMS) up to 64K Bytes.[13]
I/O and Packages are 53 Programmable I/O Lines and 64-lead TQFP and 64-pad QFN/MLF. AVR microcontroller Operating Voltages are 2.7 - 5.5V for ATmega128L and 4.5 - 5.5V for ATmega128. It has Speed Grades of 0 - 8 MHz for ATmega128L and 0 - 16 MHz for Atmega12

5.2. SD CARD (1 GB)

Secure Digital (SD) is a flash (non-volatile) memory card format developed for use in portable devices. SD card capacities range from 8 MB to 16 GB.[16]

5.3. RTC

A real-time clock (RTC) is a clock that keeps track of the current time. In this DS1307 serial real-time clock (RTC) is used. It is a low-power, full binary-coded decimal (BCD) clock/calendar, 56 bytes of NV SRAM, address and data are transferred serially through an I²C, bi-directional bus, Operating voltage 5 V, operating frequency is 32.768k Hz and optional Industrial Temperature Range -40°C to +85°C[14].

5.4. USER INTERFACE

Serial communication is used for the purpose of data transferring between micro-controller and PC and the data can be read from PC in graphical format.

VI. SIMULATION RESULTS

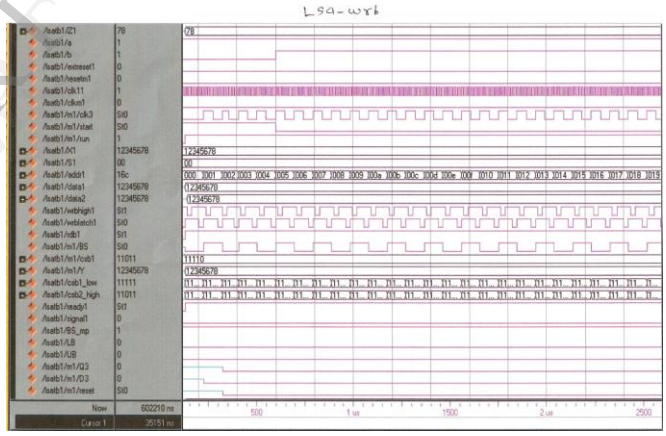


Figure3. Data acquisition through FPGA

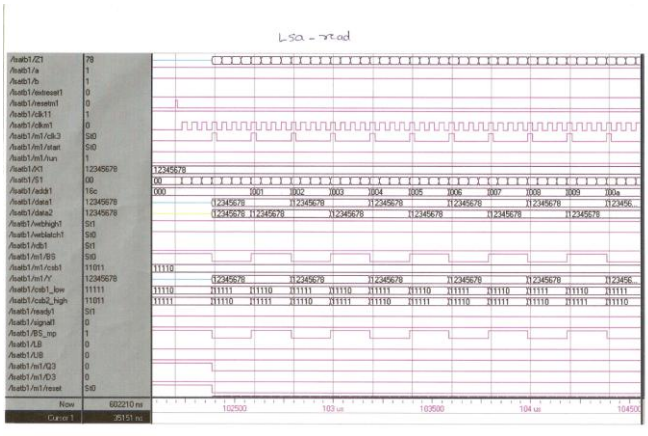


Figure4. Data retrieved from memory

Fig 3 shows the data acquisition process through

FPGA and saved in memory. After FPGA give ready signal to microcontroller for receiving clock pulse from microcontroller which is slower in speed than data acquisition rate and in fig 4 FPGA received clock from microcontroller FPGA give 8 bit data to microcontroller for further analysis

VII. CONCLUSION

The Logic State Analyzer has been designed for specific use like vibration & explosive studies i.e. this LSA is used for measuring the strength or velocity of fragments and there by measuring the explosive power of the explosive device i.e. 80 Mega samples / sec**.** This Logic State Analyzer also meets the portability for acquiring large data and also has battery backup.

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