# Literature Review on Attaining A Wide Frequency Range In Multi - Modulus Prescalar For High Speed Operations

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## Abstract

*This paper presented a literature review to attain a wide frequency range in Multi-modulus Prescalar for high speed operations. In comparing with the state-of-art methods, wide range of frequency is produced by the use of wideband Multi-modulus Prescalar. The input frequency is from the programmable output duty cycle by all-digital fast locking PWCC. The Multi-modulus Prescalar has a maximum operating frequency of 6.2 GHz. The Prescalar can divide the input frequencies and perform the additional division without any extra flip-flop. So, the practical applications like Bluetooth, zigbee, .etc of those fast speed operations done with the help of output frequency widely produced by the Multi-modulus Prescalar.*

***Index terms*** *- Multi-modulus Prescalar, PWCL, Duty cycle, Clock frequency, Asynchronous divider.*

## 1. Introduction

To meet the demand for high speed operations, nowadays many systems adopt a DDR technology. This technology is also one of the solutions for SOC systems capable of fast accessing process. Some variations and distortions have been occurred in the previous system, those limitations are avoided by the various techniques. To generate a clock with output duty cycle of 50% for accurate high speed operation. However, digital control circuit and delay elements limit the maximum operating frequency. Basically, duty cycle distortion in high speed operation due to clock mismatches. Finally, the programmable output duty cycle produce a certain frequency that has been used as the input of Multi-modulus Prescalar. In high speed system, the clock signal often requires multistage clock buffers to drive the circuit. Some variations and distortions been occurred in the previous systems. The Multi-modulus Prescalar will increase the frequency range in higher. The practical applications are in more number to be used and also that will help to increase the data transmitting time fastly.

## 2. Adaptive Pulse width Control Loop (PWCL):

**Concept:**

The duty cycle of a clock is liable to be changed when the clock pass through a multistage buffer in high speed cmos clock buffer design. PICS provide generation of output pulses during all modes of operation. Locking time is faster.

**Circuit Used:**

-Pseudo inverter control stage (PICS),
-Involvement of Adaptive control loop.

**Result:**

The duty cycle can be well controlled in the range from 20% up to 80%, and also an operating frequency of 100 MHz.

**Disadvantages:**

Low operating frequency range.

## 3. PWCL as Duty cycle corrector

**Concept:**

The conventional PWCL architecture only adopts here, but with a new charge pump circuit and a new pulse generator. The charge pump circuit is acting as a constituent of the duty cycle detector. The MPWCL controlling the duty cycle in a wide range and it operates in saturation region, which provides conditional for locking time to be fast.

**Circuit Used:**

-Modified pulse width control circuit (MPWCL).

**Result:**

The duty cycle can be controlled in range from 20% up to 80% and also an operating frequency range is 133 MHz.

**Disadvantages:**

Low operating frequency range.

## 4. PWCL in High-speed CMOS clock buffers

**Concept:**

Temperature and process deviation is influencing the signal quality degradation. Mainly to get a required pulse width and the stability of the loop

is investigated in linearized small signal analysis is used. To sizing the ratio of transistor sizes in the current mirror of charge pump is done only by the easy adjustment of pulse width to a desired value. The temperature sensitivity and process variation can be removed sufficiently.

**Circuit used:**

-Charge pump

**Result:**

The input signal duty cycle is about 50% and the output duty cycle is 50% also. The input clock at clock frequency is 625 MHz with a 50% duty cycle.

**Disadvantages:**

Limited frequency range only, so here it is not suitable for more high speed operations.

## 5. Low voltage PWCL for SOC applications

**Concept:**

The new duty cycle detector and a new pulse generator adopt from the conventional PWCL. Using those circuit, clock frequency can be increased in high range and the fixed rising edge in the output of the PWCL. Pulse width adjustment and phase locking is done by PLL/DLL and a PWCL. The low voltage provides variable duty cycle.

**Circuit Used:**

-New Duty cycle detector based charge pump,
-New pulse generator based AND gate,
-Phase fixed PWCL.

**Result:**

The clock signal with a 0.6ns pulse width for a heavily pipelined multiplier to operate a 400 MHz.

**Disadvantages:**

Using this very low frequency range, practically not applicable in more operations.

## 6. Fast locking PWCL with presettable duty cycle

**Concept:**

The lock time is by a factor of 2.58 is reduced by the voltage-to-differential converter and switched charge pump circuit. To preset the duty cycle of the output clock is described. Locking time depends on built in DLL.

**Circuit Used:**

-Voltage-differential-to-digital converter,
-Switched charge pump.

**Result:**

The output duty cycle of clock can be adjusted from 35% to 70% in steps of 5%. The operating frequency is 500 MHz up to 1.25GHz.

**Disadvantages:**

Limited operating frequency range.

## 7. Low-jitter mutual correlated PWCL circuit

**Concept:**

The scheme implemented in the circuit is mutual-correlation to adjust the duty cycle and also to increase the stability of the loop. This design is less sensitive to the variation. It suppressed the voltage rippling. The power dissipation and voltage ripple are reduced by 35.4% and 93.7%, respectively.

**Circuit Used:**

CMOS integrated circuit

**Result:**

The output is 42ps peak-to-peak jitter in the measurement at 900 MHz.

**Disadvantages:**

Limited operating frequency range

## 8. Synchronous 50% duty cycle clock generator

**Concept:**

DCCG had an clock generator is edge-triggered by an input signal to produce an in which the pulse width is denoted by a delay line. Thus, the delay line is controlled by the phase error integrator. The phase error integrator is to detect the phase difference between the input and an output signal. In the DCCG circuit, the I/O signals are synchronised. The duty cycle converge to 50% of the output signal. The circuit is designed mainly to synchronize the rising edges.

**Circuit Used:**

-Duty cycle clock generator (DCCG),
-Phase error integrator.

**Result:**

The circuit operate from 70 to 500 MHz only and the duty cycle error in output signal is less than 1.5%.

**Disadvantages:**

Low operating frequency range. The duty cycle error is not alleviated completely.

## 9. Single-path PWCL with a built-in delay locked loop:

**Concept:**

The phase alignment between the reference and output clock is been achieved. They eliminated the REF with 50% duty cycle. The duty cycle error been reduced by single-to-complementary circuit and switched charge pump. To output circuit can be adjusted for certain application like switched-capacitor circuit, dc-dc converter, etc.

**Circuit Used:**

-STC circuit and SCP circuit,

-Phase detector with a start up circuit.

**Result:**

The operating frequency is from 1 GHz to 1.27 GHz and the duty cycle of output clock can be adjusted from 35% to 70% in the steps of 5%

**Disadvantages:**

Limited operating frequency range and the duty cycle error can't be eradicated completely.

## 10. High Linearity, Fast-locking PWCL with digitally programmable duty cycle correction

**Concept:**

The use of linear control stage and DCCP can be operated within a wide range of both I/O duty cycle over range of vast frequency. Mainly, the circuit is to reduce the locking time to 4.5. The simple detection circuit is utilized to control the DCCG in complemented architecture.

**Circuit Used:**

-Linear control stage

-Digital-controlled charge pump (DCCP)

**Result:**

The frequency range of the input signal was 1 MHz to 1.3 GHz, the duty cycle range of the output signal is from 30% to 70% in steps of 5%.

**Disadvantages:**

The power dissipation and the peak-to-peak jitter are 4.8mW and 13.2ps respectively, when operating in a 1.3 GHz frequency range. Limited operating frequency range.

## 11. DLL/PWCL with adjustable duty cycle

**Concept:**

The DLL is for using the flash time-to-digital conversion, both the duty cycle of output clock are assured in 10 cycles and phase alignment. The PWCL is for the sequential time-to-digital conversion is taken here to reduce the required D-flip/flop and it locks the pulse width in 28 cycles.

**Circuit Used:**

-Delay locked loop (DLL),

-Pulse width control loop (PWCL).

**Result:**

The DLL generates 25%, 50% and 75% as the output clock with the duty cycle. The operating frequency is from 140 to 260 MHz. The PWCL generates 30% to 70% in steps of 10%. The operating frequency range is from 400 to 600 MHz.

**Disadvantages:**

For the locking time, it takes 28 cycles and the operating frequency is also very low and also not suitable for most of high speed operations. Limited operating frequency range.

## 12. Fast locking PWCC with programmable duty cycle

**Concept:**

Two delay lines and a time-to-digital detector allows the PWCC to operate in high frequency range with fewer amounts of delay cells. A new duty cycle setting circuit calculates the desired output duty without the use of look up table. The input duty cycle ranging from 230% to 70%.

**Circuit Used:**

-All digital PWCC,

**Result:**

The programmable output duty cycle ranging from 31.25% to 68.75% in increments of 6.25%.

**Disadvantages:**

Limited frequency range.

## 13. Recommended Solution:

On comparing with the previous work, the common limitation is very limited frequency range(Refer Table-1). The frequency range is mostly affected by their process variation and certain errors. So, using the Multi-modulus Prescalar produce a wide range of frequency with the use of input clock frequency and also will take the input from the paper of programmable output duty cycle, because this eradicated the limitations. So, the input is taken from the clock frequency range of programmable output duty cycle. The Multi-modulus Prescalar consists of wideband 2/3(N1/(N1+1)) Prescalar, Four asynchronous TSPC divide-by-2 circuit (AD=16), and to achieve a multiple division ratios only the combinational logic circuits are included.

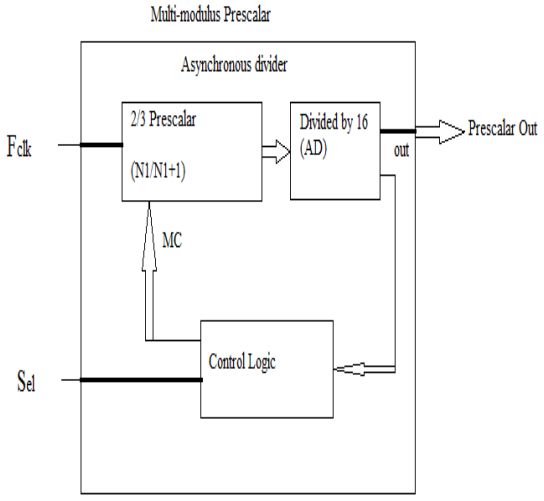


**Fig.1 Multi-modulus Prescalar**

| S. No. | PREVIOUS WORK | CLOCK FREQUENCY |
|---|---|---|
| 1 | **ADAPTIVE PWCL** | **100 MHz** |
| 2 | **PWCL AS DUTY CYCLE CORRECTOR** | **133 MHz** |
| 3 | **PWCL IN HIGH SPEED CMOS** | **625 MHz** |
| 4 | **LOW VOLTAGE PWCL FOR SOC APPLICATIONS** | **400 MHz** |
| 5 | **PWCL WITH PRESETTABLE DUTY CYCLE** | **500 MHz – 1.25 GHz** |
| 6 | **LOW-JITTER MUTUAL CORRELATED PWCL** | **900MHz** |
| 7 | **SYNCHRONOUS 50% DUTY CYCLE CLOCK GENERATOR** | **70 MHz – 500 MHz** |
| 8 | **SINGLE PATH PWCL WITH BUILT IN DLL** | **1 GHz – 1.27 GHz** |
| 9 | **HIGH LINEARITY, PWCL WITH DIGITALLY PROGRAMMED DUTY CYCLE CORRECTOR** | **1 MHz – 1.3 GHz** |
| 10 | **ALL DIGITAL DLL WITH ADJUSTABLE DUTY CYCLE --**<br><br>**ALL DIGITAL PWCL WITH ADJUSTABLE DUTY CYCLE –** | **140 MHz – 260 MHz**<br><br>**400 MHz – 600 MHz** |
| 11 | **ALL DIGITAL FAST LOCKING PWCL WITH PROGRAMMABLE DUTY CYCLE** | **200 MHz – 600 MHz** |

**Table 1. Comparison of frequency range produced in the previous work.**

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