Lighting Control System Using Power Line Communication Networking

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Abstract

In recent years people are more concerned about energy needs and energy prices. This is because shortage of energy sources. That's why industries are focusing on technologies related to energy consumption. In this paper we focus is on minimizing energy consumption of light sources in residential and commercial buildings. The objective of this paper is development of intelligent lighting control system using power line communication networking. For communication purpose power line communication concept (PLC) used. Since PLC gives well-established network infrastructure having data transmission capacity up to 14Mbps. The methodology of project implementation consists of hardware design and software design. For hardware design ds PIC microcontroller based main control module and other slave circuits are developed. And software design consists of embedded c language based microcontroller coding. This paper gives information about development of inexpensive systems for lighting control using existing network infrastructure.

Index Terms— **Power line communication (PLC), embedded systems, Energy Consumption, control and monitor, HV adapter cable, serial communication.**

1. Introduction

A lighting control system using power line communication (PLC), which is more electricity conserving and convenient, is presented here as people put more and more attention to energy conservation. Thus effort has been made to conserve energy. [1], [2]. This system is developed for residential and commercial building where large numbers of light sources are used. But all light sources are not required during day and night times. So to manage these light sources efficiently according to user's requirement this kind of system is useful.

Power Line Communication (PLC) uses existing power lines to provide a cost-effective communication medium. This technology can be used for a wide range of applications including automated meter reading, energy consumption monitoring of individual appliances, and lighting, heating, and solar applications. Data rate and robustness of a power line communication link are the main parameters that decide its application spectrum.

2. System Structure and Design of Hardware

A block diagram illustrating the functional operation of the main control module is shown in Figure -1.

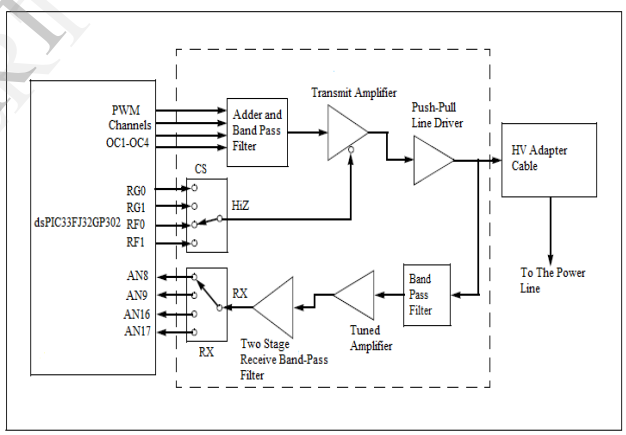

Fig-1: Master System Design diagram

Main control module operates in two stages.

a) Transmit Path
b) Receive Path

a) Transmit Path

The main control module utilizes four PWM channels to generate an approximated sine wave. The PWM channels are shifted in phase such that a sum of their instantaneous amplitude resembles a stepped sine wave. By filtering this stepped sine wave using a band-pass filter, a relatively clean sine wave is obtained, as shown in Figure-2.

After the approximated sine wave is obtained, it is amplified by the MCP6283 Op amp. The chip select pin

of this Op amp is used to implement flow-control. By asserting the HiZ pin, the transmit amplifier is enabled, thus enabling the transmission path. This HiZ pin can be configured on RG0/RG1/RF0/RF1 using jumper, JP2.
The output of this transmit amplifier is fed to the driver circuit implemented using transistors in push-pull configuration. The line driver output is then coupled into the power line through HV adapter cable.

b) Receive Path

The modulated signal on the power line is received by the HV adapter cable and is passed through an LC band-pass filter to filter out noise and interference. This filtered signal is then fed to the tuned amplifier, which is implemented using a transistor amplifier in a common-emitter configuration. This amplified signal is then filtered using a high-gain 2-stage active band-pass filter designed around the MCP6282 Op amp. The output of this filter is then fed to the Analog-to-Digital (ADC) input of the dsPIC33FJ32GP302 DSC device. The ADC input pins, AN8/AN9/AN16/AN17, can be selected by appropriately setting the jumper, JP3.
The amount of filtering required is dependent on the number of PWM channels. Using higher number of PWM channels will require filtering.

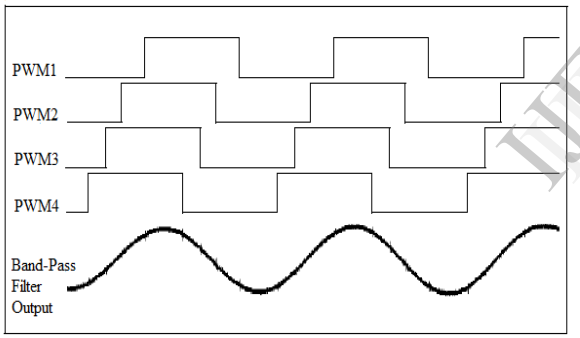

Fig-2: PWM based analog signal generation

2.1 The functional details of hardware components

2.2.1 Transmit-level set Potentiometer: This 100KΩ potentiometer sets the average signal output amplitude transmitted from main control board.

2.2.2 Transmit amplifier: The transmit amplifier is used to implement flow control on the transmit path.

2.2.3 Output Transistors: Output transistors are implemented in the push-pull configuration to amplify the transmit signal before coupling the signal into the HV adapter cable.

2.2.4 RCA connector: The RCA connector is used to connect the daughter board to the HV adapter cable.
2.2.5 HiZ Select Jumper: This jumper is used to select the dsPIC33FK32GP302 DSC device pin used for switching the transmit amplifier. Changing this jumper setting will require appropriate changes in the software.

2.2.6 ADC Input Select Jumper: This jumper is used to select the dsPIC33FJ32GP302 DSC device analog pin required to sample the received signal from the power line. Changing this jumper setting will require appropriate changes in the software.

2.2.7 Tuned Amplifier Transistor: This transistor configured in the common-emitter configuration is used to implement a tuned amplifier on the received path.

2.2.8 Receive Band-Pass Filter
This 2-stage band-pass filter provides high gain to the received signal while filtering out power line noises and interference signals. The circuit is essentially a high-pass filter with a very high gain. The gain bandwidth product limits the higher frequencies (low pass response), thereby resulting in a band-pass filter.

2.2.9 Transient Voltage Suppressor: The transient voltage suppressor is used to protect the main control module from high voltage transients on the power line.

2.2.10 Connector: The main control module connects to power board (Test-Jig) using 20 pin connector.

The software on the dsPIC33FJ32GP302 DSC device generates 4-channel PWM output, which when summed-up and filtered suitably by main control circuitry, forms an approximated sine wave. This approximated sine wave is modulated in the software using the BPSK modulation technique by controlling the PWM channels. On the receive path, the modulated signal on the power line is filtered and amplified by main control module before being fed to the ADC input of the dsPIC33FJ32GP302 DSC device. The ADC module on the dsPIC33FJ32GP302 DSC device converts this received signal into the digital domain where further filtering and demodulation is performed in software to recover the data.

2.2 HV Adapter Cable Circuit

The HV (High Voltage) cable incorporates the circuitry required to provide noise-filtering and isolation from the power line. The main control circuit and HV adapter cable are designed to operate at a carrier frequency of 129.6 kHz (CENELEC-C band).

The AC end of the HV adapter cable is plugged into a mains power outlet. The main control module is compatible with 110V/60 Hz mains supply and the 220V/50Hz mains supply.

It is important to understand that some countries have multi-phase supplies within buildings. In this case, connecting main control module to power outlets on different phases may results in partial or total loss of communication link. A signal coupler device will be required to communicate across different phases of the power supply. A typical signal coupler device consists of a high voltage rated capacitor, optionally in series with an inductor, connected across the two phases of the power supply. The capacitor used in the coupler should be rated to handle the instantaneous voltage between the two phases. Using an X-2 or X-1 rating capacitor is highly recommended.

Here, dsPIC33FJ32GP302 is used. Internal schematic of PLCC main control module is as shown below in Fig-3.

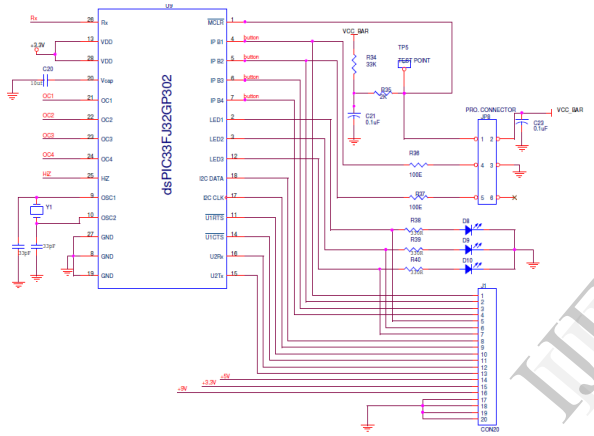

Fig -3: Schematic of PLCC Adapter Block

And bottom view of PLCC adapter is given below in Fig-3.

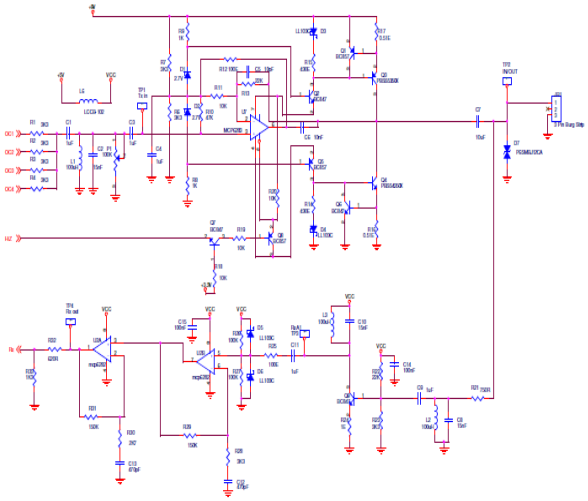

Fig-4: Schematic of PLCC adapter

3. Network-Socket

Network-Socket elements are a parts of passive circuits modules. The general block diagrams for network-socket circuit are given below.

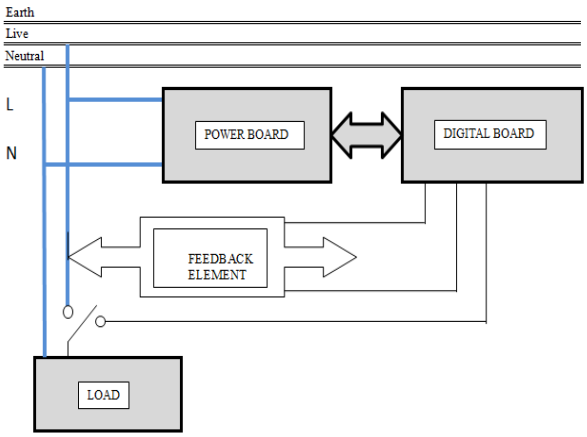

Fig-5: General Block diagram of Network-Socket

The Fig-5 shows connection to power line. Network-Socket connected through live and neutral lines. A feedback element used to indicate any light source is ON/OFF. It sends a status signal to master module, according to request of main control module.

The internal schematic of Network-Socket is as shown below. The network-socket consists of coupler circuit, communication circuit, which step-down 230V AC to required 9V signal. At the first step power line voltage step downed for communication purpose. Second stage consists of feedback circuit. From one end it receives signal from LIVE and gives to isolator. After taking feedback signal, it is given to Load Drive. And at the other end TRIAC used which is connecting to again LIVE. At last step current sensing circuit used.

4. PLCC Test-Jig

For the lighting control system design as a new product separate test-jig is developed. Through that analysis, programming, communication between two circuits is monitored. This can be on PC and test-jig module using Doclight software. Test-Jig module contains power supply, in which required 3.3V DC for dsPIC33FJ32GP302, 5V DC for MAX-485, 9V DC for communication through power lines obtained. Transceiver section used to check communication between two main modules on PC. And 20 pin connector exchange signals from controller.

4.1 Power Supply Section

Power supply sections include voltage regulators, step-down transformers, transceiver section. For power supply it is necessary to convert 230V AC into 12V DC. Input is taken from live and neutral power lines. And across VO+ and VO- output. Through that VO+, 12 VDC is collected. 12Vdc supply from U4 is given input to LM2576S-ADJ/T0263 IC. This converts it to +9Vdc. After converting to +9Vdc it again converted to +5Vdc, +3.3Vdc using LM1117-5, LM1117-3.3 respectively. These are positive adjustable and fixed output current of 1A regulators to provide 1A with high efficiency. The features of voltage regulators include low dropout, 1.3Vmax at 1A output current. 0.04% line regulation, 0.2% load regulation. 100% thermal limit burn in and fast transient response.

5. Transceiver Section

Transceiver MAX485 is used to enable communication between PC and main control module for testing purpose. Max-485 provides error-free data transmission up to 250 Kbps. It operates from a single 5V supply. It is a low power transceiver and having a common mode voltage range -7V to +12V.

6. Software Design

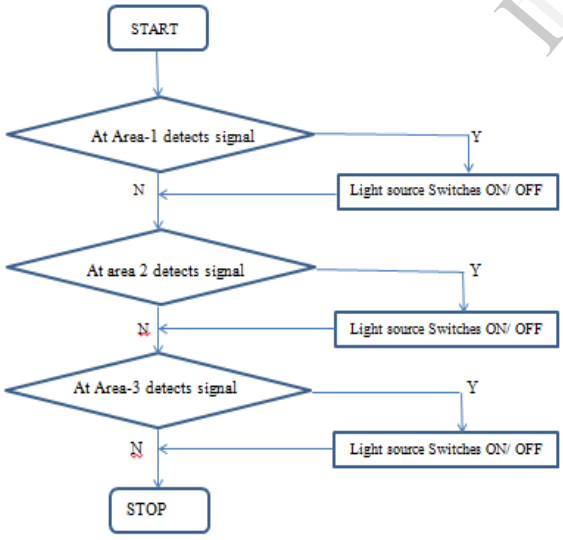

Fig-6: Flow chart of Main program

Main module control flow of program starts with the system initialization as indicated in Fig-5 with checking areas to be controlled and monitored. Monitoring and control can be continuously done. It detects signals from areas (slaves) and sends information to main control module (Master). According to that response actions will be taken.

6.1 Resource Requirement

DsPIC33FJ32GP302 DSC device with at least 2Kbytes RAM, 16 Kbytes of Flash memory, four Output Compare channels (PWM), one DMA channel, and one 12 bit ADC input (at least 500 ksps), can be used with main control board. Using dsPIC33FJ32GP302 DSC devices without the DMA feature will result in a higher processing power requirement for the software, potentially starving the application of execution time. Also, using less than four Output Compare channels will result in reduced operational range and performance.
When API functions called, the following processor resources are starting to use.

- One ADC module (default: ADC1)
- One ADC input (default: AN8)
- One optional DMA channel for the ADC servicing (default: DMA0)
- One timer to trigger the ADC conversion:
  - Timer3 when ADC1 is selected
  - Timer5 when ADC2 is selected
- One DMA interrupt vector/ADC and its triggering timer interrupt vector
- One to four Output Compare channels. Default:
  - OC1 and OC2 when PWM2 modulator is selected
  - OC2 through OC4 when PWM4 modulator is selected
- Timer2 and its interrupt vector as PWM base
- The GPIO pin selected in the configuration for CS control (default:RF0)

6.2 Developing Custom Applications

The software for main control board is designed to operate on a carrier frequency of 129.6 kHz. However, if required, depends on other PLC applications the software can be modified to operate at a different carrier frequency. In this case, the following need to be taken into consideration:

- The Hardware provided in the kit is designed to operate on a carrier frequency of 129.6 kHz. Changing the carrier frequency in software will require modifications to the hardware components, specifically the components that decide the filter cut-off frequencies

- It is necessary for the carrier frequency to be an integral multiple of the baud rate: carrier frequency, $F_C = k * baud, k € Integer$
- Lower carrier frequencies result in lower maximum possible data rates
- Carrier frequency or baud rate changes outside the combinations provided in the in the include file (…\modem\bpsk\bpsk_filter.inc) will require recalculation of digital filter coefficients
- Increase carrier frequency increases the MIPS requirement for the main control module software. For this reason, the carrier frequency must be well within the CPU's useful performance limit. The main control module software requires approximately 0.234 to 0.303MIPS/kHz of carrier frequency

6.3 Serial Communication

The data is transmitted from main control module to passive circuit serially. For that purpose UART transmission and reception code is developed. Data is transferred over the power line and received by receiver. Sender and receiver may change roles at runtime. One-to-many configurations are also valid.

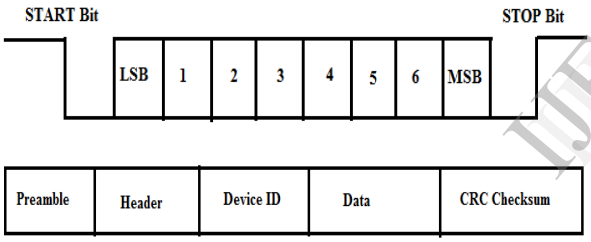

Fig-7: Serial communication and Data Frame

The link is designed to appear raw and unframed to both RS-232 devices. Internally, simple framing is used. Its purpose is to ensure that the receiver maintains byte synchronisation. Without framing it would not be practically feasible to guarantee that the receiver and transmitter are byte-aligned. A frame consists of 10 preamble characters (PRE = 0x45), one Start-of-Frame character (SOF = 0x1B), a length byte, up to 64 payload bytes, and a 16-bit ITUT CRC checksum. In total there is a 14 byte overhead for each frame. In the network these frames are transmitted simultaneously towards each device, to identify valid receiver Device ID is used. These packets accepted only if their Device ID matches to ID provided in the received frame. Otherwise frame is discarded.

The transmitter starts sending when there is at least one byte to send. A frame is terminated when there is no more data in the input buffer or when the 64th payload byte has been transmitted. As long as the application keeps providing data to send, the transmitter will transmit 64byte frames. If a frame checksum is invalid, the receiver will try to resynchronize, but the frame contents will be transferred to the UART interface. The UART configuration contains 19200bps, 8-N-1, and RTS/CTS flow control.

6.4 API Functions

The modem API functions allows for very low level access to the modulator and demodulator code. The application communicates with the modem on a buffer level and the modem itself does not impose any buffer sizes, frames or protocols. All of these features can be freely implemented in the higher layers. All low-level API-functions are declared in the header file (…modem\common\plm.h) and are C-callable. The following functions are available:

plm_mod_start( )

This function starts the modulator and configures the Output Compare channel(s), starts Timer2 and enables the Timer2 interrupt. It is mandatory to call this function before any calls to plm_exit( ) are made.

plm_demod_start( )

This function starts the demodulator and configures the selected ADC channel, starts the timer that triggers ADC conversion and optionally enables a DMA channel to service the selected ADC input. Either DMA or ADC and timer interrupts get enabled. It is mandatory to call this function before any calls to plm_recv( ) are made.

plm_demod_sync( )

This function forces a demodulator resynchronization and may be called in cases when the demodulator keeps indicating bit and byte synchronization, but higher protocol layers decide that patterns received do not form valid frames, thus suggesting that the byte synchronization is misaligned.

plm_xmit( )

This function transmits a buffer and is a zero copy operation, meaning the pointer passed is used to access payload bytes directly when needed. The operation is double buffered; meaning the transmission of previous buffer may already be in progress. In all cases, the buffer

passed is added to a single-entry wait queue and a TX_buffer_full (PLM_TX_BF) flag is set. As soon as transmission become possible, the pointer is copied to a working register and the TX_buffer_full flag cleared. The application must not write to the buffer that was passed until the modem code has finished sending. It is possible to determine whether the buffer is still in use by examining the PLM_TX_BF and PLM_TX_ACTIVE status flags. This function must not be called unless the PLM_TX_BF flag is clear.

plm_recv( )

This function fetches a received buffer. The two parameters passed are the address and the size of new buffer to fill in. The function returns an address within a previously passed buffer, pointing to the first free location in that buffer. If the address returned is equal to the previously passed buffer start address, no data has been received between the calls. If the address returned points outside the buffer (at previous buf+size), the buffer has been fully filled and could possibly overflow, if it was allowed. A NULL pointer is returned on the very first call.

plm_get_status( )

This function returns the following modem status flags:

- PLM_TX_ACTIVE – transmission is in progress.
- PLM_TX_BF – transmit buffer is full.
- PLM_BIT_SYNC – the receiver has found bit synchronization.
- PLM_BYTE_SYNC – the receiver has found byte synchronization.
- PLM_RESYNC – resynchronization has been requested.

7 Test demonstrations

This demonstration implements a UART-to-UART connection over power lines. Test setup contains connection from main control module to Explorer 16 development board. A test setup for PLC communication is as given in Figure-8. Here, explorer 16 development board is used as receiver. On which dsPIC33FJ256GP710 controller used and same code is used. For demonstration purpose the instructions are changed according to controller's instruction set. In this test setup main control module acts as transmitter and explorer 16 development board used as a receiver. Data is immediately transferred over the power line and received by receiver. Sender and receiver may change roles at runtime. One-to-many configurations are also valid. But in this test demonstration only one transmitter and one receiver is used.

7.1 Test setup: Transmitter Side

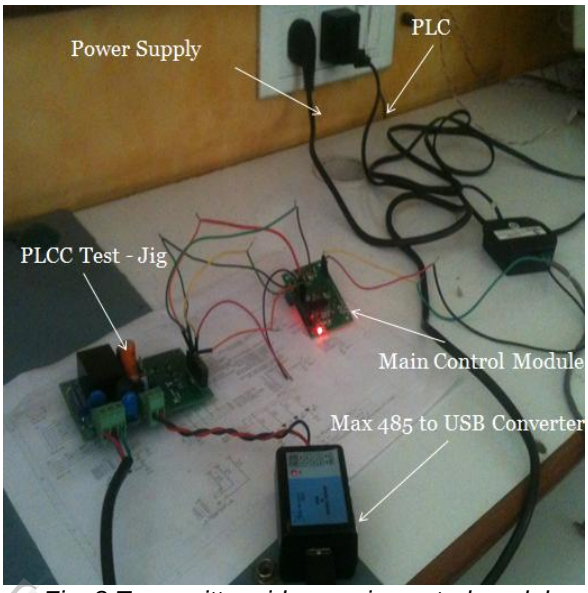

Fig: 8 Transmitter side – main control module

A power supply is given to test-jig, on which it converts to 12V, 3.3V, 5V, and 9V voltage levels.
A main control module is connected to PLCC Test-Jig using con20 connector. From con20 connector required 3.3V, 5V, and 9V signals are taken on main board. on the other end PLC line is connected to main control module.
Here 230V AC signal is used as carrier. And 9V signal is used for data transmission. Max 485 to USB converter is connected from PLCC test-jig to PC. On which signal are monitored and controlled by Dock light software.

7.2 Test Setup: Receiver Side

On a receiver side explorer 16 development board used, in which 9V signal is given to daughter board. And required 9V supply is given to development board. For testing purpose TX and RX pins are connected to each other so that loop back occurs. The reason behind this setting is when signal received by development board coming from main control module. After processing from controller appropriate signal is transmitted towards main control module.
As explained above frame contains different fields of information. When receiver receives frames in RX_buffer, frame will only accepted only when device ID matched.

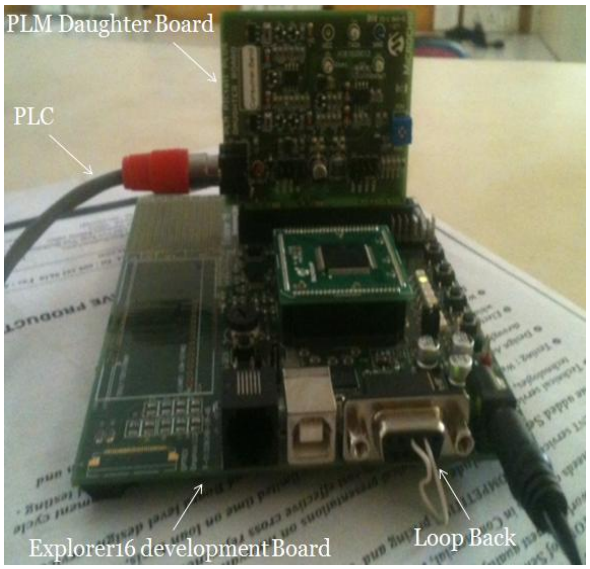

Fig-9 Receiver Side Setup

7.3 Test Results

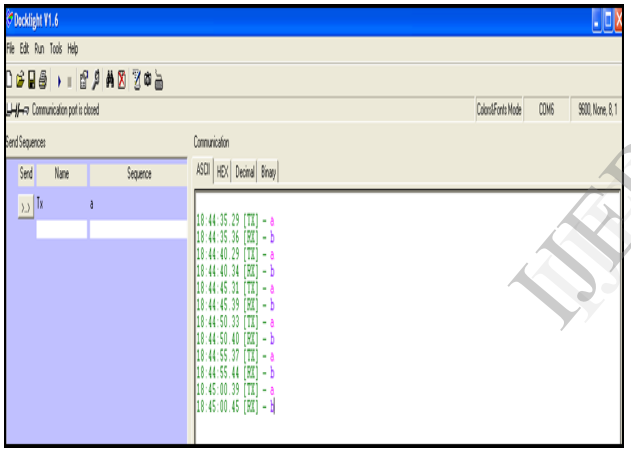

Fig-10 Test results on Dock Light Software

The signals from MAX485 to USB converter is given to Dock light software on PC. In which 19200 baud rate , and RTS/CTS hardware handshaking settings are made.
For testing "a" is transmitted from main control module. When a receiver receives "a" after processing appropriate required frame is transmitted by receiver. Here frame "b" is transmitted from explorer 16 development board. The frames are only accepted only device ID, CRC 16 checksum and other required information matched.

8. Conclusions

In this paper, we have presented a lighting control system using power line communication (PLC). A logic method is introduced to control and monitor light sources at various locations in residential and commercial buildings. Before implementation of communication in such systems transmission characteristics of power line, attenuation characteristics, noise characteristics, impedance characteristics needs to be checked.
As primary results, a communication in proposed scheme is verified by practical implementation of main control module and PC using Dock light software. At time of communication it is noticed that the communication bandwidth is affected by electrical load.
The advantages of system are easy to install and operate, low implementation cost and reliable communication.

9. References

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