Leakage Reduction In Advanced WDR Image Sensors With Halftone Pixels

Aparna. P
ME VLSI Design (PG Scholar)
Anna University

Abstract

Leakage reduction plays an important role in power consumption in many of the systems like image sensors. Adaptive bulk biasing control scheme is used to reduce the leakage during the standby mode of operation in the systems. Advanced WDR image sensors used to take images especially in situations where the light enters a premise from different angles, i.e. where both the dark and bright areas are there in the camera field of view that provides continuous tone images. Every pixel is to be converted in to halftone pixels in any of the conventional press, in order to print the image. Here a halftone pixel is generated using Floyd-Steinberg algorithm. The adaptive bulk biasing control scheme provides 21% power reduction as compared to any other standard systems.

Index Terms- Continuous Tone Image, Halftoning, WDR image sensors, Adaptive Bulk Biasing Control, Leakage Reduction, Halftone Pixels

1. Introduction

In late 1990s, performance of CMOS image sensors improved significant, in terms of the CCD applications such as pinned photodiode, charge transfer gate and micro lens. The X–Y address scanning architecture, which was employed for active pixel sensor and pixel scanning, was investigated during the 1960s prior to the invention of the CCD image sensor. The main advantage of the active pixel sensors is the suppression of the noise injected in the signal readout path or generated. A pixel without signal amplification is termed as the passive pixel. An image sensor can be of analog output, digital output or SOC type. Wide dynamic range image sensors are finding growing applications in surveillance, tactical, automotive, medical and diagnostic instrumentation (fluorescence, detection and spectroscopy) and industrial arenas. In addition to ability to capture scenes in undesirable scene disturbances such as sun reflection or laser jamming, it is able to capture the scenes with large variations in irradiance due to temperature.

CMOS image sensors have benefits such as on chip functionality and power reduction as compared to other image sensors. i.e. they have less power consumption and are intelligent, user friendly image sensors.

Dynamic range is the ratio between the largest and the smallest possible values of a changeable quantity such as signals and lights. The human senses of hearing and sight have high dynamic range, capable of hearing from a quite murmur to the sound of a heavy metal concert. It may exceed a level of 100dB .Whereas the dynamic range of sight is 90dB. A number of techniques were proposed for the leakage reduction in CMOS image sensors. They include stacking cutoff transistors [12], utilization of high threshold voltage (HVT) devices, aggressive supply voltage reduction [10], adaptive voltage scaling [11] and application of negative voltages to the wells or substrate. AB^2C was intended for the integration with image sensors operating in the rolling shutter model. It provides a body bias to the system under consideration. The forward body bias enhance the performance by means of the active current, whereas the reverse body bias reduces the leakage. The technique, originally proposed by Fish et al [5], the reverse body bias is applied dynamically using a network of resistors to the row of pixels, when the rows are not accessed. Since it have a bulk capacitance, dynamic discharging and charging has side effects such as bulk charging delay, noise or interference and additional power consumption. These problems can be reduced by means of gradual voltage application in the AB^2C scheme.

We use a modified Adaptive bulk biasing control scheme that is integrated with a WDR image sensors with halftone pixels. They have improved flexibility, robustness, performance and functionality as compared to the original one. Floyd-Steinberg algorithm is the halftoning algorithm used and based on the error dispersion. It converts the normal pixels in to halftone pixels Thus with the aid of the adaptive bulk biasing control scheme WDR image sensors provide a halftone pixel with less power as compared to any other standard systems. WDR image sensors considered only the normal pixels those

provide pictures with a large number of colors. The proposed system provides halftone pixels that simulates tone imagery by means of dots, varies in spacing and shapes i.e. halftone process reduce reproduction of visuals to an image. This reproduction relies on optical illusion, i.e. the tiny dotes in halftone are blended to tone that are smooth by human eyes. It may become easy to print the image and takes a less ink for the same with a high resolution

2. Effects of Body Biasing

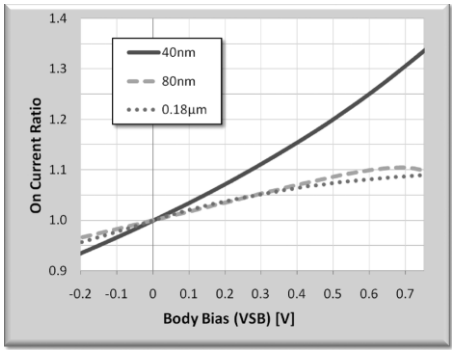
Connecting to a bias rather than to power or ground in the layout circuit is termed as the body bias. It is supplied from an on chip or from an off chip source. The forward body bias reduces the threshold voltage by applying a positive body source voltage to n channel transistor and thereby provides faster and leakier transistor. Reverse body bias on the other hand raises threshold voltage and provides both slower and less leaky transistors. The total power consumed in an image sensor can be denoted as

$$P = P_{dynamic} + P_{static} \quad (1)$$

where $P_{dynamic}$ is the power consumed during transient switching activities and P_{static} is the constant power consumed due to biasing and/or leakage currents. The threshold voltage of a transistor can be represented as

$$V_T = V_{T0} + \gamma \left[\sqrt{2\phi_b - V_{BS}} - \sqrt{2\phi_b}\right] \quad (2)$$

Where V_{T0} is the zero biasing voltage, that is set during fabrication; γ is the body-effect coefficient; ϕ_b is the Fermi potential and V_{BS} is the body-to-source voltage. *Body effect*; is the change in the threshold by creating a potential between the source and body terminals of the transistor .The speed enhancement is done by means of the body biasing in many of the digital circuits only up to 60 nm . The effectiveness of the technique degrades, as technology scales due to several factors, such as the higher influence of *drain induced barrier lowering* (DIBL) and other parameters on sub threshold leakage [6] and the increase of *band-to band Tunneling* current (BTBT) as a result of applying RBB. Body biasing techniques are quiet interested for both improving variation sensitivity as well as performance enhancement in advanced processes.



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$$V_{GS} = V_{DS} = V_{DD}$$

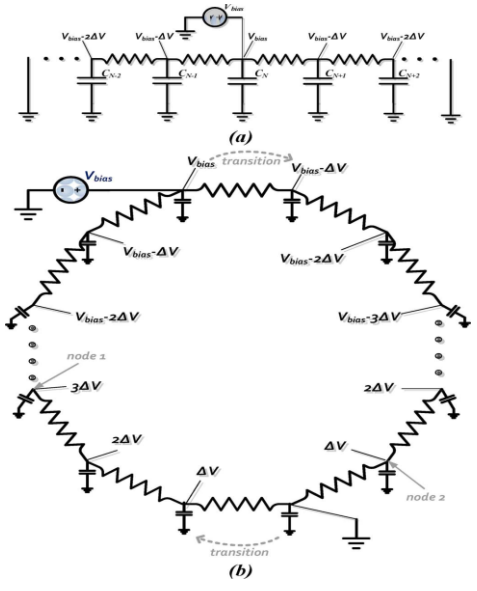
Lowering the threshold voltage that increases a device's *ON* current leads to the performance enhancement. A forward body bias is applied, and has the positive side-effect of reducing the standard deviation of the threshold voltage distribution. Fig. 1 shows the effect of forward body biasing on the saturation current (with $V_{GS} = V_{DS} = V_{DD}$) of a minimum sized nMOS transistor at various (low power) process nodes. The figure shows the drain current increases, as compared to a zero-biased equivalent transistor.

2.1Gradual Bulk Biasing

Consider the circuit shown Fig. 3(a) with 2N capacitors (each representing the bulk. capacitance of a single row) connected in parallel with approximately equal resistances between them. Apply a potential,V_{bias}, to one of the middle capacitors, a constant voltage drop will be symmetrically applied to the remaining capacitors, as they progress towards the opposite voltage supply and can be further extended by connecting the two end nodes and grounding them. A ring of RC circuits symmetrically biased around the virtual line connecting the biased node with the grounded one . The biasing point can easily be moved to a different bulk without upsetting the symmetry, by changing the connection node of both the bias voltage and the ground supply. This is analogous to changing the bias point of the active row.

This scheme results in a gradual voltage drop between the two biasing points. This transition to an adjacent row causes a slight voltage change of ΔV at each node. This small change has a very small disturbance effect as compared to the full step charge, especially since the change is gradual at then on-directly biased nodes. Therefore, a forward biased node can be set at one end of the circuit and a reverse bias can be set at the opposite end, without the need for

large drivers or the danger of applying a large abrupt voltage step.



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Ends of the arrays, where the original circuit lost correct biasing structure. Second, the resistors are replaced with constant biased nMOS transistors [8]. This creates adaptable, high.

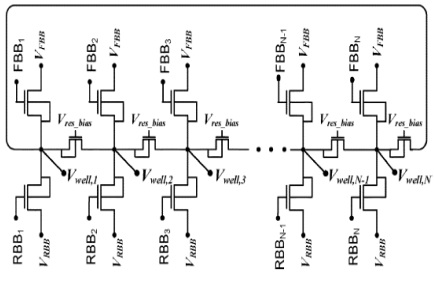
6T SRAM bit cell with minimum sized pMOS and access transistors (M1, M3, M5, and M6) and slightly larger pull-down nMOS (M2 and M4) is used as the standard memory cell.1-bt in pixel resistance, small area resistors, and enables further flexibility, as will be shown herein. Third, theAB^2C improved concept is suitable for utilization in SRAM arrays. In this paper we show an example of its application to a serially accessed SRAM array that is operated in , as part of a wide dynamic range advanced image sensor.

2.2 Body Biasing With AB^2C Scheme

The simplest body bias is to apply a fixed bias identically to all the chips with a value set during design. A more advanced body bias methodology is to apply adaptive body bias where a different bias value is calibrated. Adaptive body biasing corrects the systematic manufacturing variations thus reducing threshold voltage variations and sort yield improvement

AB^2C scheme is efficiently integrated with large components that consist of many leaking devices and can only be applied to components ,that operates in the serial access scheme. Thus a MOS image senor is a perfect candidate for the scheme. In addition to the dynamic control and the system performance enhancement this technique can be used for adapting circuits for performance under process variations. For the body biasing separate well are required for each transistor for different body potential. So it requires the implementation of techniques such as DTCMOS [7] though the size requirement for each transistors are very large.ie A specific circuit with limited number of devices or an entire block of devices with a common well potentials can only make use of the body biasing. Only the later can be considered in the case of a pixel or bitcell arrays with thousands or millions of devices.

A row wise addressing is commonly used for cell access .Accordingly FBB provides an efficient method for performance enhancement. The n-well and p -well in each cell in a certain row should be common .These well are modelled as a lumped RC network. In the improved version the resistor network is connected in a ring structure, provides performance improvement especially at the end of the arrays. nMOS transistors are used instead of the resistors in the circuit and they make use of SRAM bitcells.



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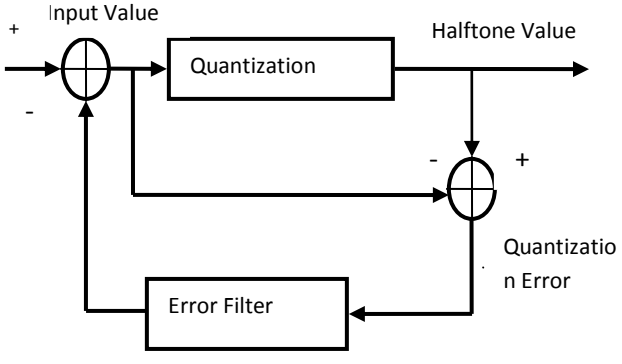
Within the 3 nmos transistor one is connected as pass gate transistor to forward body bias and the other one to the reverse body bias. Shift registers are connected to the gate of the transistors, which control the digital input. The third one, resistive device is connected in between the bulk voltages of the sub circuits.

3. Floyd-Steinberg Algorithm

Floyd-Steinberg algorithm is an image halftoning algorithm, used for the halftone image production in our case. It is a image halftoning algorithm based on the error dispersion. Even though the algorithm is the slowest, provides the best result s compared to any other classical methods. It is commonly used in situations such as,to convert an image in to GIF format ,that is restricted only with 256 colors. halftone image production in our case. It is a image halftoning algorithm based on the error

dispersion. Even though the algorithm is the slowest, provides the best result s compared to any other classical methods. It is commonly used in situations such as, to convert an image in to GIF format ,that is restricted only with 256 colors.

The algorithm scans the image either from top to bottom or from left to right .At each point the color of the image is considered it with the actual color in the system hardware. This difference is termed as the quantization error. The error is diffused over the neighboring pixels where they are added up with the current value. Thus the halftone pixel value is obtained.



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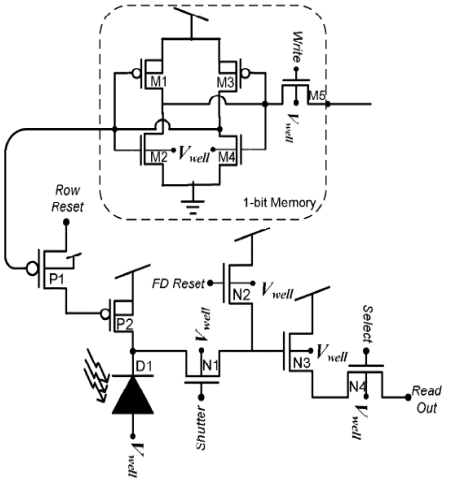
Halftone value is compared with the input value with threshold by means of feedback loop. Quantization error is calculated by subtracting the halftone value from the input value. Error filter transfer this quantization errors to the neighboring pixels without affecting the pixels that re scanned. Hence, if a number of pixels have been rounded downwards, the next pixel is rounded upwards.

4. Halftone Pixels

In this paper a WDR image sensor with halftone pixels is taken as the test case. This image sensor uses both on-chip SRAM and an in-pixel memory bit array to store the number of resets applied to each pixel during a single frame.



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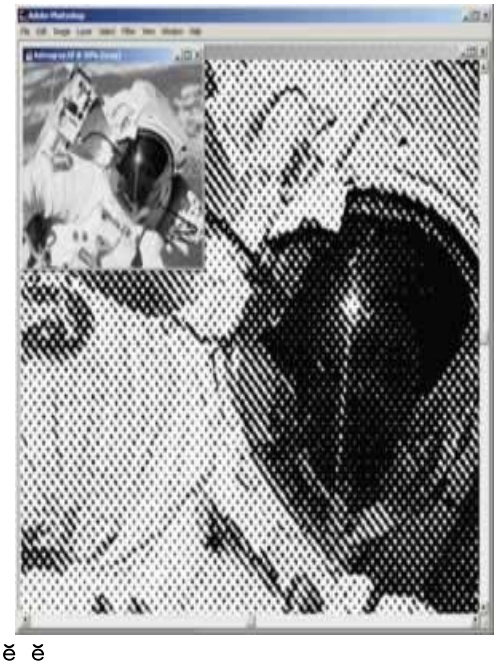
The pixel uses standard 6T SRAM which consist of access transistors and the minimum sized PMOS transistors. The photodiode voltage is reset only when the in-pixel memory has been set. to 1. Adaptive bulk biasing scheme is given as the input through $\boldsymbol{V_{well}}$. Transistors M2, M4, M5, N1, N2, N3, and N4 of the pixel, all receive the RBB voltage, during integration period. Selected rows are forward biased that reduces the threshold voltage of transistors N1-N4 increasing the swing of the signals and shutter efficiency.

4.1 Halftone Images



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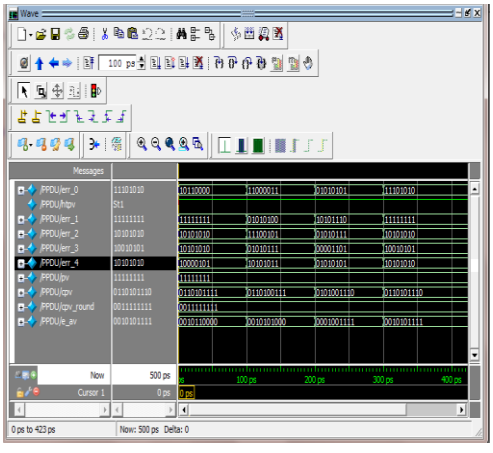
Halftone images mainly consist of dots that vary in size, shapes and spacing. Larger dots are for denser and darker areas while smaller are for lighter areas. The continuous tone images consist of infinite number of colors, whereas halftone process reduces visual reproduction. Optical illusion is the basis of this reproduction i.e. the tiny halftone dots are blended in to smooth tone by human eyes. Thus it is a more efficient way to print the images**.**

5. Observations and Measurements

The normal pixel generation and a halftone pixel generation in a WDR image sensor is compared .Here we have taken the display of 300 ASCII characters to consider the normal pixel generation. The simulation results of the pixel generation is shown below.



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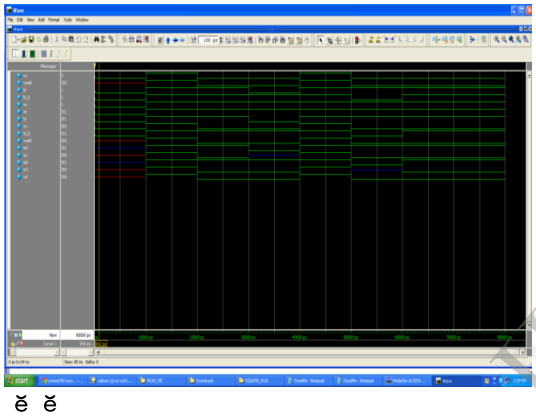

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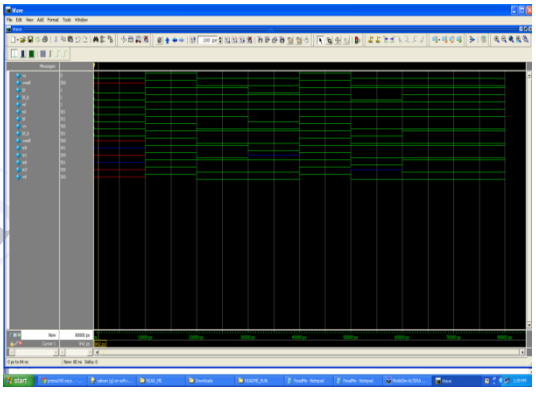

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The halftone pixels are generated by means of the Floyd-Steinberg algorithm. The generation of halftone pixels is represented by means of simulation results using Modelsim shown in fig.7

AB^2C is used to reduce the leakage within the systems such as image sensors. The scheme can be represented in terms of simulation results of the schematic circuit. It is shown below in fig.8

The power consumed in the above three cases can be calculated by means of Xilinx ISE13.2 Design tool and compared in the below table.

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Power summary	
System	**Utilization (in %)**
AB^2C Scheme	1
Normal Pixels	36
Halftone Pixels	27

The power consumed for both the normal pixels and for the halftone pixels are very small compared to standard

systems, with the help of adaptive bulk biasing control scheme.

6. CONCLUSION

Adaptive bulk biasing scheme is used to reduce the leakage within image sensors. As a test case a wide dynamic range image sensor with halftone pixels is used. These halftone pixel images have wide applications in remote sensing, iphone, ipad and ipod touch. The scheme reduces the power consumption of the WDR image sensors with halftone pixels up to 21%. A halftone image is made up of a series of dots rather than a continuous tone. These dots can be of different sizes, different colors, and sometimes even different shapes. Larger dots are used to represent darker, denser areas of the image, while smaller dots are used for lighter areas.

Halftone images are using in newspapers and magazines because it is a much more efficient way to print images. Since a halftone image is made up of discrete dots, it requires significantly less ink to print than a continuous tone image. As long as the resolution of the image (measured in LPI) is high enough, the dots appear as a continuous image to the human eye. However, if you closely examine the images printed in a newspaper, you should be able to see the dots that make up the halftone image.

Even more advanced pixels such as chrome book pixels, other than halftone pixels may be used in WDR image sensors in the future work. The implementation of the scheme integrated with WDR image sensors in Xilinx ISE 13.2 software

REFERENCES

[1] Adam Teman, Orly Yadid-Pecht and Alexander Fish " Leakage Reduction in Advanced Image Sensors Using an Improved AB^{2}C Scheme," IEEE J. Sensors, vol.20,2012

[2]K. von Arnim, E. Borinski, P. Seegebrecht, H. Fiedler, R. Brederlow,R. Thewes, J. Berthold, and C. Pacha, "Efficiency of body biasing in90 nm CMOS for low power digital circuits," in Proc. 30th Eur. Solid-State Circuits Conf. (ESSCIRC 2004), 2004, pp. 175–178.

[3] B. H. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and sizing for minimum energy operation in sub threshold circuits," IEEE J. Solid-Circuits, vol. 40, pp. 1778–1786, 2005.

[4] K. Cho, D. Lee, J. Lee, and G. Han, "Sub-1-V CMOS image sensor using time-based readout circuit," IEEE Trans. Electron Devices, vol.57, pp. 222–227, 2010

[5] M. Elgebaly and M. Sachdev, "Variation-aware adaptive voltage scaling system," IEEE Trans. Very Large Scale (VLSI) Integr. Syst.,vol. 15, pp. 560–571, 2007.

[6] A. Fish and O. Yadid-Pecht, "Low-power "Smart" CMOS image sensors,"in Proc. IEEE Int. Symp. Circuits and Systems (ISCAS 2008), 2008, pp. 1408–1411.

[7] A. Fish, T. Rothschild, A. Hodes, Y. Shoshan, and O. Yadid-Pecht,"Low power CMOS image sensors employing adaptive bulk biasing control (AB2C) approach," in Proc. IEEE Int. Symp. Circuits and Systems ISCAS 2007), 2007, pp. 2834–2837.

[8] V. Gruev, Y. Zheng, and J. Van der Spiegel, "Low power linear current mode imager with 1.5 transistors per pixel," in IEEE Int. Symp. Circuits and Systems (ISCAS 2008), 2008, pp. 2142–2145.

[9] A. Hokazono, S. Balasubramanian, K. Ishimaru, H. Ishiuchi, C. Hu and T.-K. Liu, "Forward body biasing as a bulk-Si CMOS technology scaling strategy, IEEE Trans. Electron Devices, vol. 55, pp.2657–2664, 2008.

[10] K. Ito, B. Tongprasit, and T. Shibata, "A computational digital pixel sensor featuring block-readout architecture for on-chip image processing," IEEE Trans. CircuitsSyst. I, Reg. Papers, vol. 56, pp.114–123, 2009.

[11] A. Khajeh, A. M. Eltawil, and F. J. Kurdahi, "Effect of body biasingon embedded SRAM failure," in Proc. 2010 IEEE Int. Symp. Circuitsand Systems (ISCAS), 2010, pp. 2350–2353

[12] C. H. Kim, J. J. Kim, S. Mukhopadhyay, and K. Roy, "A forward body-biased low-leakage SRAM cache: Device, circuit and architecture considerations," IEEE Trans. Very Large Scale (VLSI) Integr. Syst.,vol. 13, pp. 349–357, 2005

[13] Q. Lin, W. Miao, and N. Wu, "A high-speed target tracking CMOS image sensor," in Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC2006), 2006, pp. 139–142.

[14] S. Mukhopadhyay, Q. Chen, and K. Roy, "Memories in scaled technologies: A review of process induced failures, test methodologies, and fault tolerance," in Proc. IEEE Design and Diagnostics of Electronic Circuits and Systems (DDECS '07), 2007, pp. 1–6.

[15] S. Mukhopadhyay, K. Kang, H. Mahmoodi, and K. Roy, "Reliableand self-repairing SRAM in nano-scale technologies using leakage and delay monitoring," in Proc. IEEE Int. Test Conf. (ITC 2005), 2005, pp.10–1135

[16] S. Narendra, D. Antoniadis, and V. De, "Impact of using adaptive body bias to compensate die-to-die_ variation on within-die variation,"in Proc. Int*Symp. Low Power Electronics and Design*, 1999,pp. 229–232.

[17] C. Neau and K. Roy, "Optimal body bias selection for leakage improvement and process compensation over different technology generations, "in *Proc Proc2003 Int. Symp. Low Power Electronics and Design (ISLPED '03)*, 2003, pp. 116–121. [18] J. M. Rabaey, A. Chandrakasan, and B. Nikolic´, *Digital IntegratedCircuits: A Design Perspective*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 2003, p. 761.

[19] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, pp. 305–327, 2003.

[20] F. Tang and A. Bermak, "A 4T low-power linear-output current-mediated CMOS image sensor," *IEEE Trans. Very Large Scale (VLSI) Integr.Syst.*, to be published.

[21] A. Teman, S. Fisher, L. Sudakov, A. Fish, and O. Yadid-Pecht, Autonomous CMOS image sensor for real time target detection and tracking," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS2008)*, 2008, pp. 2138–2141..

[22] J. W. Tschanz, J. T. Kao, S. G. Narendra, R. Nair, D. A. Antoniadis,A. P. Chandrakasan, and V. De, microprocessor frequency and leakage," *IEEE J. Solid-State Circuits*, vol. 37,1396–1402, 2002.

[23]L. Wei, Z. Chen, M. Johnson, K. Roy, and V. De, "Design and optimizationof low voltage high performance dual threshold CMOS circuits,"in *Proc. Design Automation Conf.*, 1998, pp. 489–494.

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Aparna.P ,was born in Kerala ,India on April 21,1990. She received B.TECH degree in Electronics and Communication from Vedavyasa Institute of Technology, Calicut University, India in 2009 and 2011and completed ME degree in VLSI design from Srinivasan Engineering college, Anna University in 2011 and 2013.

Her current research interest include Very Large Scale Integration and Image Processing