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Leakage Power Reduction in CMOS VLSI

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Abstract--**With rapid changes in semiconductor technology chip density and frequency have increased, making the power consumption one of the major concern. Thus low power design has become the major challenge for present designers. Report says that 45% or even higher percentage of total power consumption is due to the leakage power of transistors. So reduction of leakage power is a great challenge for current and future technologies.in this paper, we are going to discuss different techniques for reducing the leakage power like dual threshold, transistor stacking, sleepy approach and variable threshold in CMOS VLSI circuit.**

Index Terms: chip density, leakage power, low power design, dual threshold, sleepy approach, variable threshold

I. INTRODUCTION

With increasing demand of System on Chip, the number of transistors also getting increased in VLSI chip, which causes high power dissipation. Now a days the demand of portable devices like smart phones, PDAs, tablet PC also increasing, therefore low power designing has become a key parameter. More power dissipation also causes heating up the device which reduces the performance, reliability and durability. Hence the need of the low power VLSI circuit arises, so leakage power needs to be reduced.

II. POWER DISSIPATION IN CMOS

In the following sections, we will discuss different techniques to reduce leakage power in the VLSI circuit. There are mainly two types of power dissipation in the CMOS Circuit. They are dynamic power dissipation and static power dissipation or leakage power. The dynamic power dissipation mainly causes due to the switching of the transistors in the CMOS circuit. It is given by following equation,

$$P_{dynamic}=\alpha V_{load} V_{dd}^2 f \qquad (1)$$

Here 'α' is the switching activity i.e. the clock cycles in which the circuit switches, C_{load} is the load capacitance, V_{dd} is the supply voltage and 'f' is the clock frequency.

The second type of power dissipation i.e. static power or leakage power generally occurs when the circuit is not switching or in standby mode. As the technology is scaling, this has become significant now a days. The major component of static power are,

a) Reverse biased pn-junction leakage current b) Sub threshold leakage c) GIDL and GIBL leakage currents d) Gate oxide Tunneling current

a) Reverse biased pn junction leakage current

The junction leakage causes due to minority carrier diffusion and drift near the edge of depletion regions and also from generation of electron holes pairs in the depletion region of reverse bias junctions. The reverse biased pn junction current is given by,

$$I_D = I_S (e^{V/V_T} - 1) \qquad (2)$$

'I_S' depends on the doping level, area and perimeter of diffusion region.

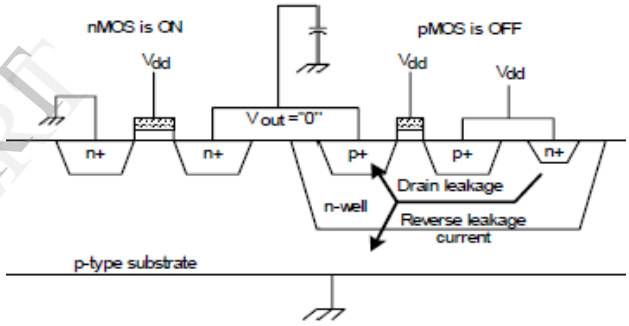

Fig: 1 Reverse biased pn junction leakage

b) Sub threshold leakage

Subthreshold leakage current is the weak inversion conduction current between source and drain in an MOS transistors, occurs when gate voltage is lower than threshold voltage. The subthreshold leakage current increases with respect to the temperature and it also increases as threshold voltage scaled down along with the power supply voltage for better performance.

$$I_{sub} = Ae^{\frac{q}{n'kT}(V_G - V_S - V_{th_0} - \delta' V_S + \eta V_{DS})}\left(1 - e^{\frac{-q V_{DS}}{kT}}\right) \qquad (3)$$

The various parameters that affects the subthreshold leakage current are, drain induced barrier lowering, body effect, narrow width effect , effect of the channel length and effect of the temperature.

c) GIDL and DIBL leakage current

The gate induced drain leakage (GIDL) is due to the high electric field, induced by the gate potential, in the gate drain overlap region. The drain induced barrier lowering (DIBL)

occurs when the drain potential increases. The pn-junction between the drain and the substrate becomes more reverse biased, so the depletion layer grows and reduces the volume controlled by the gate. As a result V_{TH} decreases as V_{DS} increases. It is given as,

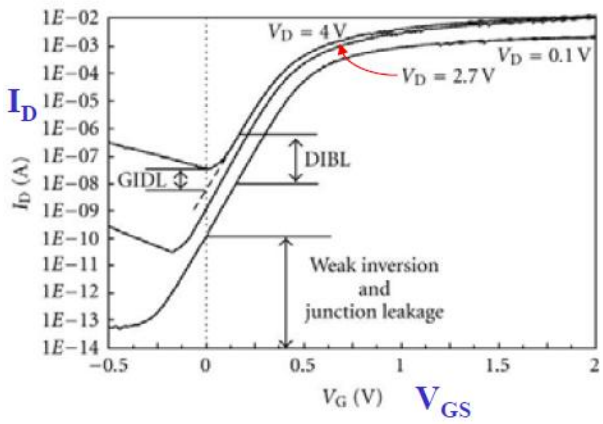

Fig: 2 Response of GIDL and DIBL

d) Gate Oxide tunneling leakage

When there exist a high electric field across a thin gate oxide layer, gate oxide tunneling electron can result in leakage. Electron may tunnel into the conduction band of the oxide layer, this is called Fowler-Nordheim tunneling. There can also be direct tunneling through the silicon oxide layer.

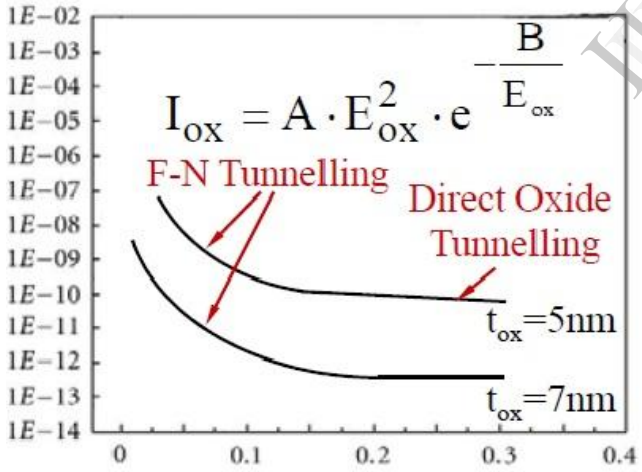

Fig: 3 Gate Oxide tunneling leakage, I_{ox}/E^2 vs 1/ E

We have seen the leakage power dominating the total power consumption, so it is necessary to reduce the leakage power. There are exists many methods to reduce the leakage power or static power in the CMOS VLSI circuit those are discussed below.

III. REDUCTION TECHNIQUES

1) Design time techniques

The design time techniques are static, they can't be modified or changed once they are fixed, while the circuit is

$$I_{off} = I_0 e^{\frac{V_{GS} - V_{th,0} + mV_{DS}}{\eta V_T}} \quad \textbf{(4)}$$

operating. To reduce leakage it exploit the delay slack.

a) Dual threshold CMOS

This technique compromise between the high performance and low leakage power. Transistors those are located on critical paths are assigned as low threshold voltage and the transistors that are not critical to timing can tolerate high threshold voltages and slow switching speeds. The selection of the control voltages are conducted at design times, no additional circuits are required. The below table shows the leakage current for high and low threshold voltage transistors in a 70nm process technology. We observe that leakage energy of transistors of low threshold voltage is larger than a factor of 75 than the high threshold voltage transistors. Hence if we replace the low $-V_t$ transistor with a high $-V_t$ transistor it will reduce the energy or power.

Table (1)

Tr type	V_{dd}	V_t	I_{off}
High-V_t	0.75	0.4	26
Low-V_t	0.75	0.2	1941

(Effect of V_t on leakage current)

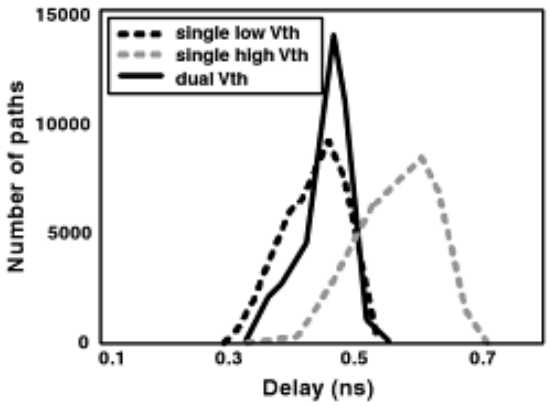

Fig: 4 path distribution of dual V_t vs single V_t

b) Multiple supply voltage

Supply voltage scaling also reduces the leakage power, because subthreshold leakage due to the GIDL and DIBL as well as the gate leakage component when the supply voltage is scaled down. To achieve low power with respect to high performance two methods can be employed i.e. dynamic and voltage scaling.

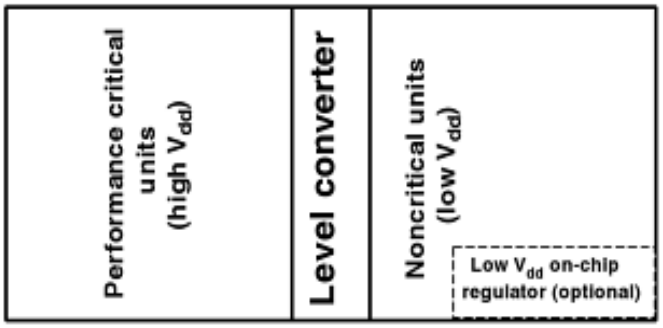

Fig: 5 two level multiple supply scheme

2) Runtime leakage reduction

a) Transistor stacking (self reverse biased)

Subthreshold leakage current reduces when it flows through a stack of series connected transistors. The below figures shows the transistor stacking process.

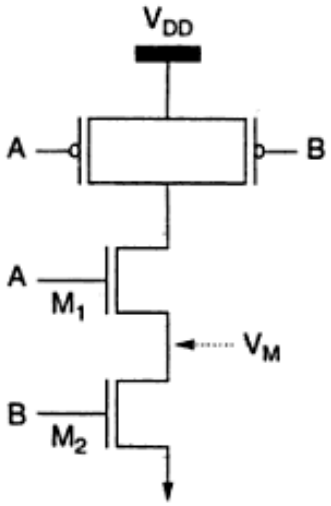

Fig: 6 stacking effect in NAND gate

When both M_1 and M_2 are turned off, the voltage at the intermediate node V_m is positive due to small drain current. Due to positive source potential, gate to source voltage of M_1 becomes negative, hence subthreshold current reduces.

b) Sleep transistor technique

The sleep transistor approach is most commonly used technique for the leakage power reduction. In this technique an extra "sleep" PMOS transistor is placed between pull up network and VDD and an additional NMOS transistor is place between the ground and pull down network. These transistors turn off the circuit by cutting off the power in the sleep mode. So this technique can reduce the leakage power in good margin by cutting off the power source. However this technique causes floating output in the sleep mode.

i) Sleepy stack approach

We have discussed the stack approach already, so when the stack approach effectively merged with sleep transistor technique, this sleep stack approach is developed. By using stack effect this technique divides transistors into two half-length transistors. Then the sleep transistors are connected parallel to one of the divided transistor. During the sleep mode sleep transistors are off, stacked transistors reduces the leakage current. The main cons of this technique is the power delay since we are replacing the transistors.

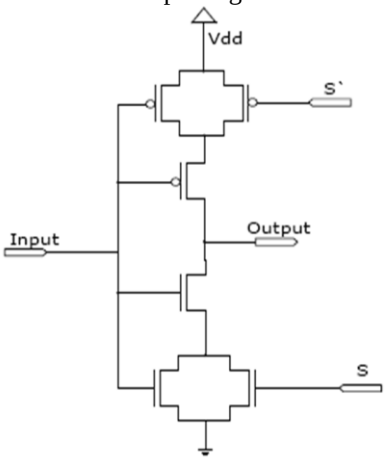

Fig: 7 sleepy stack approach

ii) Sleepy keeper approach

In sleepy keeper technique, sleep transistors is parallel in both pull up and pull down network. It uses the leakage feedback technique. In this technique a PMOS and NMOS is placed in parallel transistors. In sleep mode sleep transistors are turned off and one of the parallel connected transistors keep on track power rail.

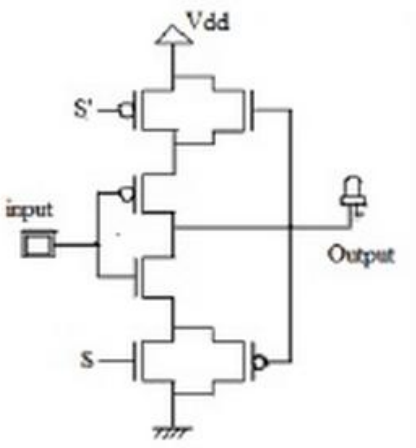

Fig: 8 sleepy keeper approach

iii) Dual sleep technique

In dual sleep methods two transistors are connected in parallel similar to the keeper approach. In both active or inactive mode sleep transistors is always in both pull down and pull up network. So output is connected to GND and VDD always. In this method less number of transistors is needed to apply a certain logic circuit. This method has good tradeoff between the delay, power and area.

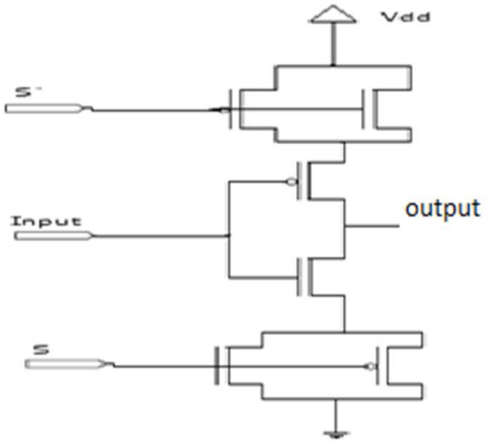

Fig: 9 dual sleep technique

iv) Dual stack technique

In dual stack method two PMOS and two NMOS transistors are used. The two PMOS transistors are used in the pull down network and two NMOS network are used in pull up network. The advantage of this method is, NMOS degrades at high logic level and PMOS degrades at low logic level. But the disadvantages of this technique compared to previous technique is delay, the delay increases.

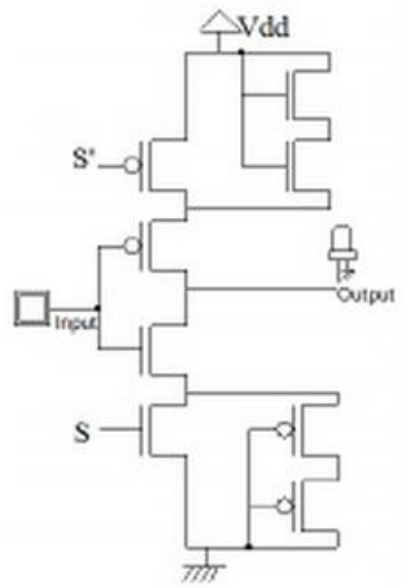

Fig: 10 dual stack technique

c) Variable threshold CMOS (VTCMOS)

This is a body biasing design technique. To achieve different threshold voltages, a self-substrate bias circuit is used to control body bias. In the active mode a zero body bias is applied, while in standby mode a reverse body bias is applied to control the threshold voltage and cut off leakage current.

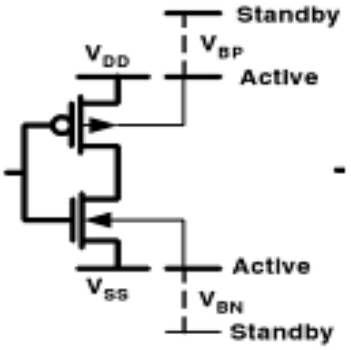

Fig: 11 Variable threshold CMOS

IV. CONCLUSION

We reviewed various sources of leakage current in CMOS circuit and described a number of reduction techniques for controlloing the leakage current. In a way of enumarating some of the design and conclusion that lie ahead,necessity of robust subthreshold leakage control techniques that do not affect circuit performance and devlopment of physical design tools that support multiple voltages on the chip. There is a need of more advanced technique to reduce the power consumption while maintaining the chip perforamance.

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