International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 2 Issue 1, January- 2013

Leakage current reduction techniques in SRAM

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Abstract

Leakage components are very important for estimation and reduction of leakage power especially in sub micron regimes in which threshold voltage, gate oxide thickness and channel length scale downwards. In present era it provides motivation to design a low power SRAM. This paper presents several techniques for leakage current reduction for SRAM cell.

Keywords: low power design, low leakage memory design, SRAM, gate leakage current, subthreshold leakage current

1. Introduction

Semiconductor memories are one of the most important subsystem of modern digital systems. A memory is a storage unit. In previous years many hardware devices like magnetic tapes, drives and optical disks were used. Random access memory (RAM) is widely used in all the devices for storage. In RAM, especially this paper concerns with the SRAM. In SRAM three modes are performed: read mode, write mode and standby mode. Here data is lost when power is removed means it is the volatile memory, but data does not 'leak away' as like in a DRAM, so no need of refresh cycle in SRAM. Scaling of this technology has going on so large amount of memory can be fabricated on a single chip and due to that memories can able to do the operation speedy. Because of high density of chip, power dissipation increases. So the need for low power memory arises. For low power operation unnecessary usage of power should be reduced and one of the most important parameter for that is the leakage current. In this paper overview of several techniques is given like dual threshold, gated-VDD, DRG and multi threshold technique.

2. Conventional 6T SRAM

As shown in figure.1 this cell built up of two cross coupled inverters and two access transistors, connecting the cell to the bit lines. The access transistors are used to communicate with outside and cross coupled inverters makes the storage element. The cell is symmetrical and fully compatible with CMOS processes. Mainly three modes of SRAM are: read mode, write mode and standby mode.

2.1 Read cycle

In read cycle the stored content in the cross coupled inverter can be red. Suppose that memory content is '1' and precharging both the bit lines at 1. Now assert the WL, which enables both the access transistors M5 and M6. Values of Q_bar and Q transferred to BL and BL_bar respectively. BL precharged and BL_bar discharge through M5 and M1 transistors to 0, here M1 is on because Q is 1. On BL side M4 is on because Q_bar is 0, it will try to pull up BL to VDD. If the memory content is '0' then the operation perform is vice versa. The difference of BL and BL_bar should minimum and it is called delta, which will sense by a sense amplifier. Here the sensitivity is more than the read speed will be more.

2.2 Write Cycle

Write cycle starts by applying value we wish to write to the bit lines. If we wish to write 0 then apply 0 to the BL and 1 to the BL_bar. If we wish to write 1 then the values applied to bit lines should be reversed. Then WL asserted and value to be

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stored is latch in. Note that the reason this works is that the bit line input drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

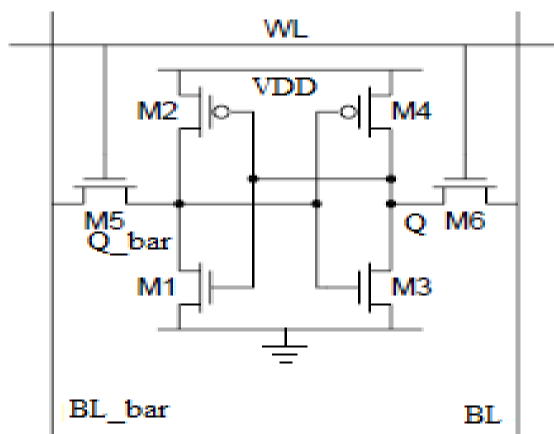

Fig. 1: 6T SRAM

2.3 Standby mode

If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are connected to the supply. In this mode no action could be taken and for retain the data the more power is consumed by SRAM, so the techniques are suggested to reduce the power consumption by reduction in leakage current.

3. Leakage power components

In SRAM conventionally two components are prime those are: dynamic power dissipation and static power dissipation. Dynamic power dissipation is occurs because of charging and discharging of load capacitance and nonzero rise and fall time of input waveforms. Leakage power contains mainly three components.

3.1 Gate leakage

The current flowing into the gate of the transistor is also called tunneling. It results when tunneling of electrons, holes from the bulk silicon into the gate in an NMOS, PMOS respectively. It composed of major three components:

- Gate to source and gate to drain overlap current.
- Gate to channel currents.
- Gate to substrate current.

Gate leakage is shown in fig.2

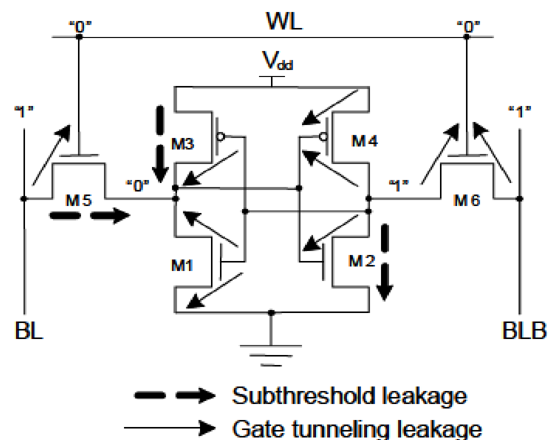

Fig. 2: Gate and subthreshold leakage current in 6T SRAM [1]

3.2 Subthreshold leakage

It happens when the transistor is operating in weak inversion region. It is the drain source current of a transistor when the gate source voltage (Vgs) is less than the threshold voltage. The subthreshold current depends on threshold voltage exponentially, which results in large subthreshold current especially short channel devices. In fig. 2 subthreshold leakage current is shown by the dotted arrow.

3.3 Junction tunnelling leakage

This is mainly a reverse biased pn junction leakage, which has mainly two components:

- Minority carrier diffusion near the edge of depletion region.
- Electron hole pair generation in depletion region of reverse biased junction.

The junction tunneling current is an exponential function of reverse bias voltage across the junction and junction doping. This component is a negligible contributor to the total leakage current.

4. Leakage current reduction techniques

4.1 Dual threshold technique

In this technique some parts of the circuit use higher threshold and remaining portion work with low threshold. Two ways are possible to implement this technique, first is the symmetric cell and second is the asymmetric cell.

Here in fig. 3, N3 and N4 are the driving transistors, so low threshold could be apply there and because of these thin channel devices switching time will be reduced, which provides fast access of the cell.

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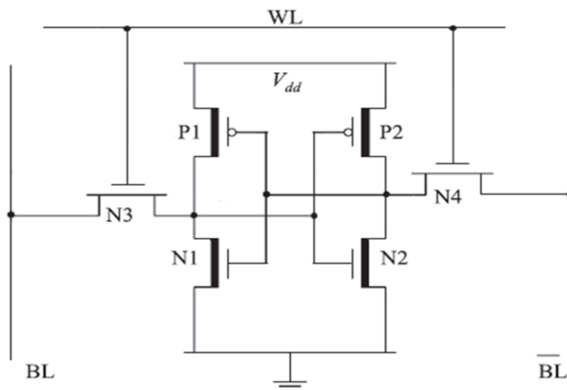

Fig. 3: Dual threshold 6T SRAM cell (symmetric)

Remaining transistors N1, N2, P1, P2 use high threshold means thick channel so they possess low subthreshold leakage current. So because of reduction in leakage current low power operation is possible in SRAM.

In fig. 4 reduce the leakage power but read access kept short. Depends on the stored value watch all transistors and transistors, which are contributing in leakage make their threshold high. Here read access time degraded because N2 and N4 contain high threshold so BL take long time to discharge.

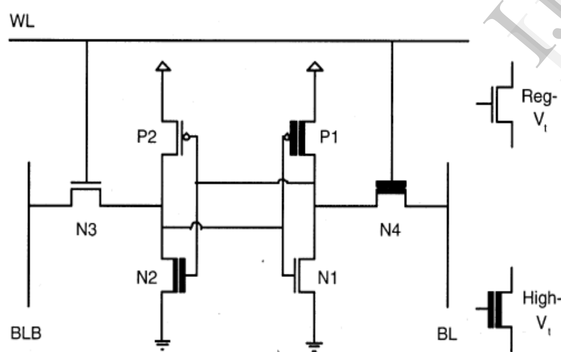

Fig. 4: Basic asymmetric cell [2]

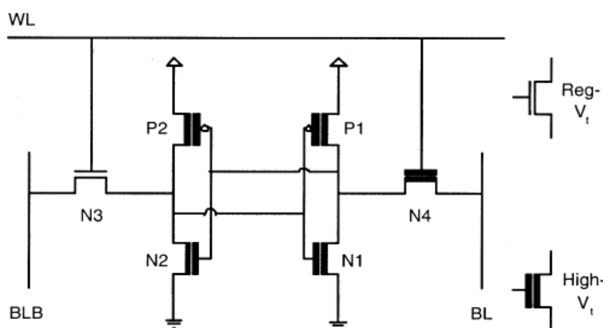

Fig. 5: leakage improved asymmetric cell[2]

In fig. 5 shows the improved leakage as compared to basic asymmetric cell. PMOS is very little affected on read access time, so make transistor P2 high threshold. And second improvement is making the N1 high threshold because there is no need for low threshold.

4.2 Gated VDD technique

Leakage current increases exponentially with the decrease in threshold voltage. The key idea behind an addition of one extra transistor in supply voltage or ground path is that the transistor turns on in the used portions and turns off during unused portions. Main reason of the leakage current reduction is the stacking effect.

It occurs because of the conjunction of the extra transistor with the cell's transistors when gated-VDD transistor is off.

In fig. 6 gated-VDD with NMOS transistor is shown. Here NMOS transistors are connected between NMOS transistors of SRAM and ground path. Same way gated-VDD with PMOS transistors can connect between PMOS transistors of SRAM and supply path. Gated-VDD transistor turns on when cell is in active mode and off when cell is in standby mode. It should contain enough width to carry currents during read, write cycle.

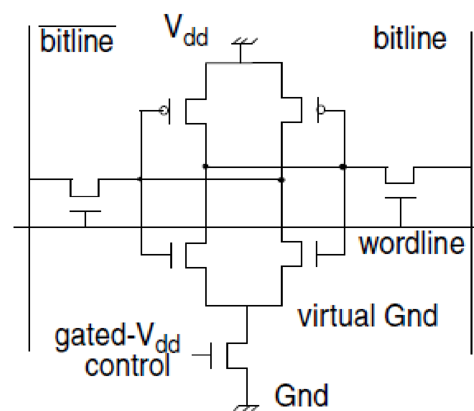

Fig. 6: SRAM with an NMOS gated-VDD[4]

In NMOS gated-VDD, transistor width can be calculated by multiplication of one of the NMOS transistor (because during read cycle only one NMOS transistor is in on state) width and total SRAM cells in one block. Standby leakage current reduces due to stacking effect which occurs due to three NMOS transistors available between bit lines and ground terminal. In PMOS gated-VDD, negligible area overhead and transistor width reduces because of no concern during the read

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cycle of SRAM. Good isolation is not provided here.

4.3 Multithreshold technique

The key idea in this technique is to insert a high threshold sleep control in series with low V_{th} circuitry. Here chip contain two types of transistors. Among them high threshold transistors are for lower subthreshold current and low threshold transistors to improve the performance. These two different types of threshold can be developing by changing the channel length, by changing the doping or by having two different oxide thicknesses.

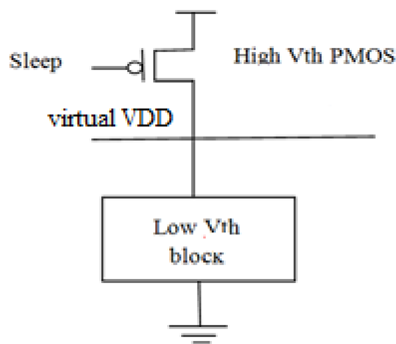

Fig. 7: MTCMOS using PMOS

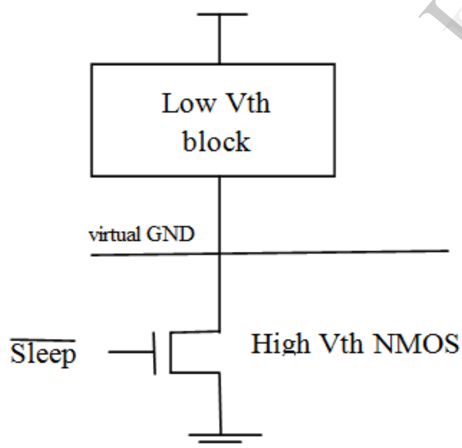

Fig. 8: MTCMOS using NMOS

In fig. 7 high threshold PMOS is used with the block and in fig. 8 same way NMOS is used. By this mechanism virtual power rail is created instead of the direct connection of the block with the main power rail.

4.4 DRG (data retention gated ground) scheme

Here the gated control is applied by WL. Before starting of the read operation particular row of cells turn on and all the remaining rows are inactive so no need to turn off the whole block.

When the cell is inactive, it retains its data with "1" storage node remaining at VDD and "0" storage node lying to an intermediate voltage of the NMOS transistor. When the gated transistor turns on the "0" node returns to ground and discharges one of the bit lines. The value stored in the SRAM cell can be retained till the gating transistor is off. The size of gating transistor should proper.

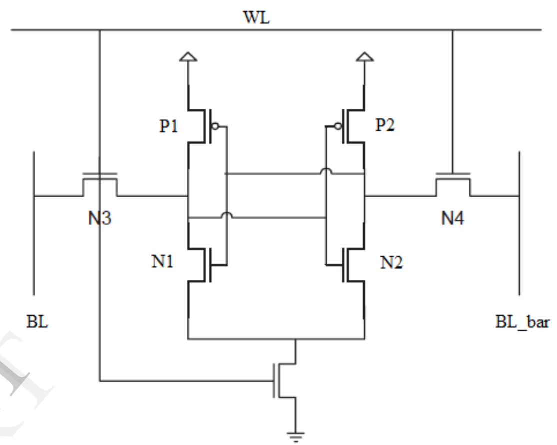

Fig. 9: DRG SRAM cell

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5. Conclusion

For leakage reduction, leakage components and four techniques: dual threshold, gated VDD, multi threshold and DRG scheme discussed here. The main parameters which are considered before designing are the leakage parameter, performance in terms of speed, read delay, write delay, transition overhead and stability. Still it is the tread-off between parameters in designing of SRAM. So before choosing of any technique checking is very important in all aspects then selects the best appropriate technique which is most suitable to our application.

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