Leakage Current Minimization in VLSI Design

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Abstract - To design high performance systems, more functions are integrated into single chip by scaling down the size of device. Leakage current is becoming an important factor of total power consumption of integrated circuits. As technology scales the size of chip leakage current grows exponentially and become large component of total power dissipated. The area of research is developing the circuit techniques to reduce the sub threshold leakage current in both active and standby mode to minimize the total power dissipation. This paper describes the need to consider gate leakage current while determining the sleep state pattern is explained. Circuit reorganization and sleep state assignment techniques demonstrated for gate and sub threshold minimization of static and dynamic circuits. The MTCMOS technology for the minimization of gate and sub threshold leakage current is also explained for the low power circuits.

Index Terms: - Introduction, Gate Leakage, Static circuits, Dynamic circuits, MTCMOS, Conclusion, References, About author.

I. INTRODUCTION

In earlier, VLSI Design is high speed, low cost and small area without much bothering about power dissipation but presently low power VLSI design is needed. In recent years, the scaling of device dimensions and threshold voltage have significantly increased sub-threshold leakage and its contribution to the total chip power dissipation. Also gate oxide thickness has been scaled to maintain proper control of the channel by the gate. Gate leakage is expected to be a major component of leakage in future technology generations and has been identified as one of the most important challenges to future device scaling. Gate leakage power, which was almost non-existent in the previous technology generations, is expected to contribute more than 15% to the total chip power dissipation in the today's technology generations. To date, most circuit-level leakage minimization techniques focus only on sub-threshold leakage reduction, without considering the effects of gate leakage. Gate leakage is primarily being addressed from a CMOS technology perspective and the use of high gate dielectric (k) have being proposed. One of the approaches that address gate leakage, BGMOS, uses multiple threshold voltages and multiple oxide thickness devices. The use of PMOS dominated circuits was proposed in, on the basis that PMOS devices exhibit lower gate leakage compared to identical NMOS devices. However, due to band-to-band tunneling and use of different dielectrics, the gate leakage through PMOS devices is no longer negligible and needs to be considered. In this paper, we account for the contribution of gate leakage on total leakage by considering forward and reverse gate tunneling through both NMOS and PMOS devices. Gate leakage in conventional sleep-state patterns (which focus only on sub-threshold leakage) are evaluated and new sleep-state assignments for transistor stacks are proposed for total leakage minimization. We also present circuit re-organization schemes for total leakage reduction of dynamic circuits in sleep mode. Finally, we look into the effect of gate leakage on the MTCMOS circuit scheme and propose the use of sleep-state assignment in conjunction with MTCMOS to obtain increased total leakage savings.

II. GATE LEAKAGE ANALYSIS

Gate leakage current for an NMOS transistor of 0.1m process shows an exponential dependence on the gate-to-source bias. At high gate bias, gate leakage current decreases with increasing drain-to-source bias. This can be attributed to the fact that a higher drain voltage results in a smaller electric field across the gate oxide at the drain end of the channel (lower VGD). At low gate bias, gate leakage was found to increase with increasing drain bias (due to the increase in reverse gate leakage with increasing drain bias, i.e., VGD). Thus, for a given gate-to-source bias, gate leakage is minimum when the gate-to-drain voltage is minimized. In addition, gate leakage current was found to be almost insensitive to the body-node voltage. The techniques presented in subsequent sections aim at minimizing the gate-to-source (VGS) and gate-to-drain (VGD) bias across a majority of devices, thereby obtaining a reduction in gate leakage and total leakage of the circuit.

III. STATIC CIRCUITS

Consider a three-high NMOS transistor stack (as found in the Nand3 cell shown in Fig. 1). The sub-threshold leakage through the transistor stack is minimized when all of the devices in the stack are turned 'OFF', (i.e. in case when <000> pattern is applied). Since conventional leakage minimization methods concentrate primarily on sub-threshold leakage, the <000> pattern is believed to be the lowest leakage vector for a Nand3 cell. However, when such a pattern is applied, the output is high and all of the PMOS devices experience high voltages from gate-to-drain and gate-to- source, resulting in high field across the gate oxide causing gate leakage, which can be substantially high due to the greater width of PMOS devices. To reduce gate leakage, it is necessary to maintain the terminals of most of the devices at same potential. This can be attained by turning 'ON' all but the lowest NMOS transistor in the stack using input pattern of <110>. Under such condition, only one PMOS device (P3) exhibits gate leakage. The gate leakage of the 'ON' NMOS transistors (N1, N2) is also negligible. Since the internal nodes in the stack are charged almost to the supply rail resulting in a low VGS/VGD for the device. The 'OFF' transistor (N3) at the bottom of the stack prevents sub threshold leakage from increasing tremendously. The total leakage for some of these vectors (fig-2) is clearly dominated by the gate leakage component. Even though sub-threshold leakage for the vector <110> is greater than sub-threshold leakage for the vector <000>, <110> is the minimum total leakage state for Nand3 cell. Thus, it is necessary to re-evaluate conventional leakage minimization schemes and input vector assignments to account for the effect of gate leakage. With gate leakage expected to increase more rapidly than sub-threshold leakage, we expect that turning 'ON' all but the lowest device in a transistor stack will be the lowest leakage state for a transistor stack in future technology generations.

IV. DYNAMIC CIRCUITS

This section focuses on sleep-state leakage minimization of dynamic circuits. Consider a typical 2-input dynamic AND cell as shown in Fig.3. During sleep state, the clock is held either in the pre charge phase (low) or the evaluate phase (high). If the clock is held in the evaluate phase, the dynamic node will be discharged, and the output will be at logic high. Since in a domino chain, the output of a dynamic cell drives other same kind of cells, it can be assumed that the inputs to the dynamic cell will also be at logic high. In such a state, all of the devices in the pull down n-stack and the output pull-up transistor (i.e., devices on the evaluate path) will exhibit gate leakage. Since these devices are sized to reduce delay, it can result in considerable gate leakage current. The sub-threshold leakage in this state is small, since it is mainly through the devices on the pre charge path. On the other hand, when the clock is held in the pre charge phase, the dynamic node is charged to high state, the output will be at logic low and the inputs can be considered to be at logic low. In this case, the devices on the pre charge path exhibit gate leakage, while the devices on the evaluate path contribute to the sub-threshold leakage. Though sub-threshold leakage of the NMOS pull-down tree is minimal due to stacking effect, sub-threshold leakage through the wide output pull-up transistor can be considerable.

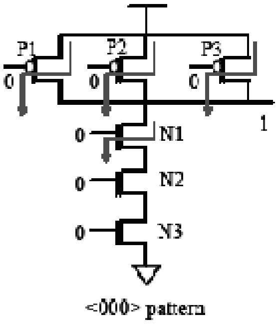

Fig.1 Input patterns for NAND3 cell

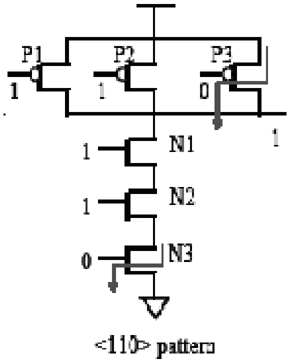

Fig-2 Total possible input vectors for NAND Cell

Thus, in either of the two states, the total leakage of the cell may be high, although due to different mechanisms. Conventional techniques claim that holding the clock in the evaluate phase is the lowest leakage sleep state, but this approach completely neglects gate leakage. Two proposed schemes are shown in Fig.4. Both of these aim to minimize the total (Sub-threshold plus gate) leakage current of the cell in sleep state.

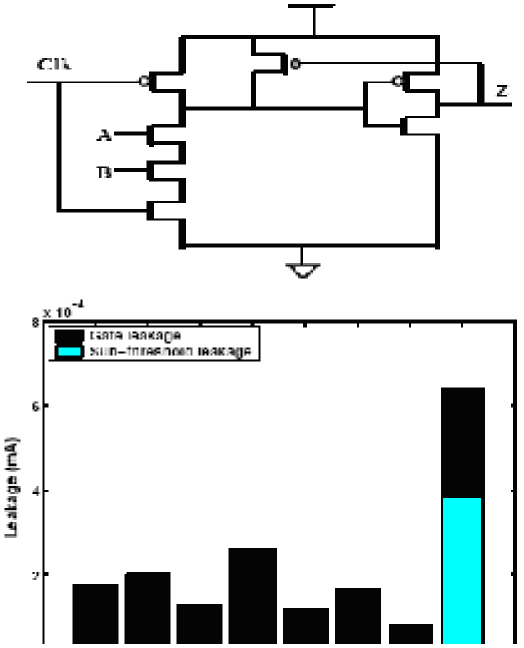

Fig-3 Typical two Input AND Gate

The output pull down tree is modified to incorporate two small devices (N1, P1) that are controlled by the sleep-state control signal S. The pre charge and evaluate clocks are separated in Scheme A. This will need additional circuitry for clock separation and can also result in clock skew problems. Scheme B uses a single clock same as in original configuration. In Scheme A, in sleep state, the pre charge clock is kept high, while the evaluate clock is kept low. The inputs to the cell can also be considered to be high. The activated conditional pull-up devices (P1, P2) therefore charge the dynamic node and the output received is logic high. In this state, gate leakage of both the evaluate and the pre charge paths are reduced (only the evaluate transistor exhibits reverse gate leakage current) since most of the devices see an identical voltage at all terminals. The sub-threshold leakage of the output pull-up PMOS device is also reduced due to the 'OFF' device N1, resulting in significant savings in total leakage power. Since all of the additional devices are small, the delay degradation on the critical path is minimal. The additional devices can be desirably sized to obtain requisite pre charge times and leakage savings. For Scheme B, the clock is held low in sleep state. The dynamic node and the output of the cell are high (similar to scheme A) reducing the gate and sub-threshold leakage of the output PMOS inverter. The savings in total leakage is slightly reduced, since the pre charge transistor exhibits gate leakage in addition to an increase in the sub-threshold leakage through the evaluate tree. However, in this configuration, no additional devices are needed for the evaluate tree, minimizing the delay degradation. The percentage savings obtained in gate leakage power and total power, along with the area overhead and degradation in pre charge and evaluate times, are listed in Table 1 for several commonly-used dynamic circuits. For instance, savings of about 73% in gate leakage and 13% in total leakage results in case of dynamic AND cell as shown in Fig. 3,4,5 by using Scheme A with an area penalty of less than 7% and over 1% degradation in delay. Fig 3,4 & 5 explains Dynamic circuit reorganization for gate and total leakage minimization.

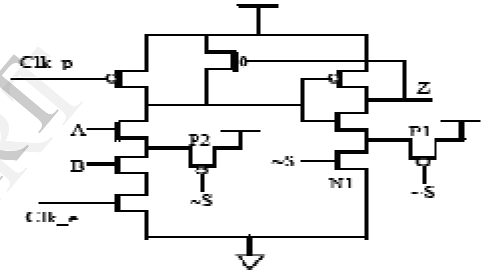

Fig-4 Scheme A, Separate Pre charge and Evaluate logic

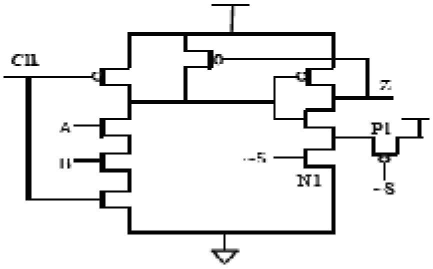

Fig-5 Scheme B, Single Pre charge and Evaluate logic

Table 1: Percentage savings and penalties for dynamic circuit reorganization schemes of fig.3, 4, & 5 compared to conventional dynamic circuit

Circuit	Scheme A	Scheme B

Circuit	Gate leakage savings	Total Leakage saving	Evaluate Penalty	Precharge penalty	Area penalty	Gate leakage savings	Total Leakage saving	Evaluate Penalty	Precharge penalty	Area penalty
3 i/p And	73.50	13.0	1.20	27.90	6.00	51.3	14.0	-0.51	27.3	4.03

V. MTCMOS CIRCUITS

The MTCMOS scheme has been introduced for reduction of sub- threshold leakage current in sleep state [5]. In this section, we investigate the effect of the MTCMOS configuration on gate and total leakage for which the three configurations as shown in Fig. 5 are considered. In the sleep state, the high VT footer and header devices are turned 'OFF' (thereby minimizing sub-threshold leakage current). This causes the virtual supply rails to be close to VDD or ground (in case either of footers or headers are used), or to be close to VDD/2 (in case both headers and footers are used). The total leakage is the sum of the sub-threshold leakage of the sleep devices, the gate leakage of the sleep devices and the gate leakage of the input stage. The devices of the first stage exhibit gate leakage according to input vector. For instance, if only footers are used, the virtual ground plane will be close to VDD. Thus, all of the devices in the logic circuit have their drain and source at nearly the supply rail. If an input vector of <0000> is applied, then all of the devices in the first stage will see a high VGS and VGD, and hence exhibit gate leakage. However, when an input vector <1111.> is applied, these devices will have identical voltage at all of their terminals, resulting in minimal gate leakage. This makes the leakage in sleep-state for the footer-only, configuration dependent upon the applied input vector.

A similar argument can be presented for the header only configuration. Here if Header only or footer only scheme is used, an appropriate input vector (00000... or11111....) should be implemented to obtain maximum savings in total leakage as shown in Fig. 6 which plots the gate leakage for an industry- standard decode circuit for all the schemes above. In this case, the first 23 vectors are randomly generated, while vectors 24 and 25 are the <000.> and <111..> vectors. Here the total leakage for the header only configuration with the <000...> input vector is almost 50% lower than the average leakage of remaining 24 vectors. Similarly, the application of the <111...> vector for the footer only configuration results in over 40% savings compared to the average leakage for the other 24 vectors. Further, the gate leakage of the sleep-state devices (Headers and footers) can be considerable enough since these devices experienced a high reverse VGS and VGD leakage can be reduced by using both headers and footers. When both headers and footers are used, the virtual supply and ground rails float close to VDD/2. The gate-to-drain and gate-to-source bias across the sleep devices is reduced by about half, and hence their gate leakages are reduced. The gate leakage of the input stage is also reduced. Table 2 lists the ratio of the leakage currents for the MTMOS configurations of Fig. 6 compared to the leakage of the original circuit for an industry standard decode circuit in advanced processes.

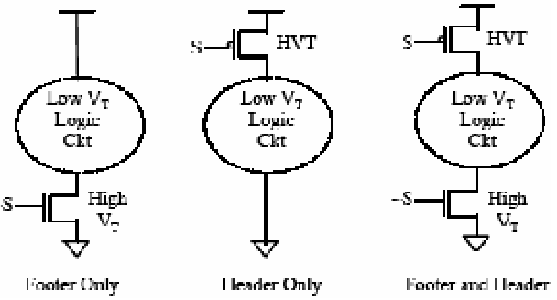

Fig-6 MTCMOS configuration (A, B, &C) evaluated.

Table 2: Leakage currents ratio for MTCMOS configurations of Fig. 6 compared to original circuit

	Sub threshold savings	Gate leakage Savings	Total leakage savings
Footer Only	15.1	39.6	80.8
Header Only	111.0	28.4	61.2
Header & Footer	720.3	270.1	505.3

VI. CONCLUSIONS

In this paper growing importance of gate leakage current has been shown and the need to consider gate leakage in any leakage minimization scheme has been demonstrated. An analysis of gate leakage and optimal sleep-state assignments for transistor stacks in static circuits is presented and also new dynamic circuit is introduced. The savings in total leakage current using these schemes lies in range of 2% to 38% with less than 7% increase in device area. Also tried to evaluate the MTCMOS from a gate leakage perspective and illustrated the need to use both headers and footers to obtain maximum leakage savings.

VII REFERENCES

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