Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 11, November - 2017

Leakage Analysis for Low Power Quasi-Adiabatic Architectures using Semi-Custom Design

Ms. K. Jayanthi
Department of Electrical and Electronics Engineerinng
Mepco Schlenk Engineering College
Sivakasi, India

***Abstract*— There exist a number of methods to reduce power dissipation. The most common is to reduce the power supply voltage. Adiabatic charging and discharging of capacitors can accomplish significant reduction in switching power dissipation. The term energy recovery depicts the nature of the circuits which recover a portion of the energy that is stored in the capacitances during computation, and recycle the energy for subsequent computations. These circuits offer significant reduction in power dissipation when compared with conventional static CMOS design. However, limited number of literatures is found so far in regard to the leakage effects in adiabatic circuits, though there has been a plethora of circuits using conventional CMOS design. This work presents the analysis of leakage power in the widely published 2N2P, 2N2N2P, PFAL, IPGL quasi-adiabatic circuits. The influence of the threshold voltage on leakage current and the method of reducing the same are presented. Analysis is done for different (W/L) ratios of the PMOS transistors that form the charge/recovery path of the adiabatic circuits, across a wide frequency and supply voltage range. The PMOS transistor size affects the speed of response, the output load capacitance, the maximum adiabatic frequency range, the Adiabatic Gain of the circuit and the layout area of the circuits. Simulation is done by varying the frequency around 500 MHz and supply voltage around 3.3V. The simulation is done and verified by using Tanner Spice Simulator using the AMS350nm process models obtained from Austria Microsystems.**

Keywords*— *Adiabatic Circuits; Charge Recovery Logic; Leakage Power.

I. INTRODUCTION

The importance of reducing power dissipation in digital systems is increasing as the range and sophistication of applications in portable and embedded computing continues to increase. System-level issues such as battery life, weight, and size are directly affected by power dissipation. Inroads into reducing power dissipation of the digital systems only serve to improve the performance and capabilities of these systems.

Power dissipation in static CMOS circuits consists of dynamic and static power components. The dynamic power is due to charging and discharging of node capacitance and is defined by

$$P = C_L V^2 f \qquad (1)$$

The static power is due to leakage currents and current drawn from the supply voltage. The power dissipation in conventional CMOS circuits can be reduced by reducing the decreasing the value of capacitance (C) or the supply voltage (V) [1] between the logic high and the logic low levels.

The power consumption is the most important decisive factor for the design and enhancement of portable and high performance applications. Hence, the growth have be on the road to look at for techniques to reduce the power dissipation, low power operation, and designing for energy recovery and recycling. Energy recovery technique proves to be a potential approach for the design of low power VLSI circuits. The most important advantage of adiabatic circuits results from its inherent nature of deriving a constant current from the power clock and the FETs working with minimum voltage between its source and drain terminals. These circuits are classified into fully adiabatic and quasi-adiabatic circuits, based on whether full energy recovery or partial energy recovery is obtained in the process.

II. ADIABATIC SWITCHING CIRCUITS

Adiabatic switching is a new approach for reducing power dissipation in digital logic. When adiabatic switching is used, the signal energies stored on circuit capacitances may be recycled instead of dissipated as heat [1]. For an energy recovery circuit, the ideal energy dissipated when a capacitance C is charged from zero to V_{dd}, or discharged from V_{dd} through a circuit of resistance R during time T is given by

$$E_{diss} = I^2 RT = \left(\frac{CV_{dd}}{T}\right)^2 RT = \left(\frac{RC}{T}\right) CV_{dd}^2 \qquad (2)$$

when the time T >> RC, the energy dissipation is much smaller than that occurring in the conventional complementary metal oxide semiconductor (CMOS) circuit, for which an energy of $\frac{CV_{dd}^2}{2}$ is required during a charge and an equal amount during the discharge cycle. As a result, when the charging time T is much larger than the RC time constant, the power consumption can be reduced.

A variety of adiabatic logic architectures has been proposed for low power VLSI design [2]–[5]. Most of them use diodes or diode like devices for precharge, which causes inevitable energy loss due to the voltage drop across the diodes. Other designs have been projected to purge the precharge diode; however, they have potential problems of floating output nodes and faulty logic [5]. The literatures have brought out several types of adiabatic circuits namely, 2N-2P, 2N-2N2P, PFAL, Improved Pass-gate Adiabatic Logic (IPGL). The Efficient Charge Recovery Logic ECRL [2] of 2N2P structure, which is generally used as a reference for evaluating the power dissipation of a new-fangled logic

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 11, November - 2017

family. Figure 1 (a) shows the structure of 2N2P buffer using two cross-coupled *p*MOS for precharge and recovery. This logic exhibits a non-adiabatic loss proportional to CV_{tp}^2, where V_{tp} is the threshold voltage of *p*MOS devices in the cross coupled transistor pair. The non-adiabatic dissipation occurs during a brief interval in the beginning of the evaluation phase [2].The 2N-2N2P logic as shown in Figure 1(b) derived from 2N2P, for the comparative advantage of eliminating the cross-coupled NMOS switching resulting in non-floating outputs for large part of the recovery phase. These devices present a balanced capacitive load and have better speed characteristics.

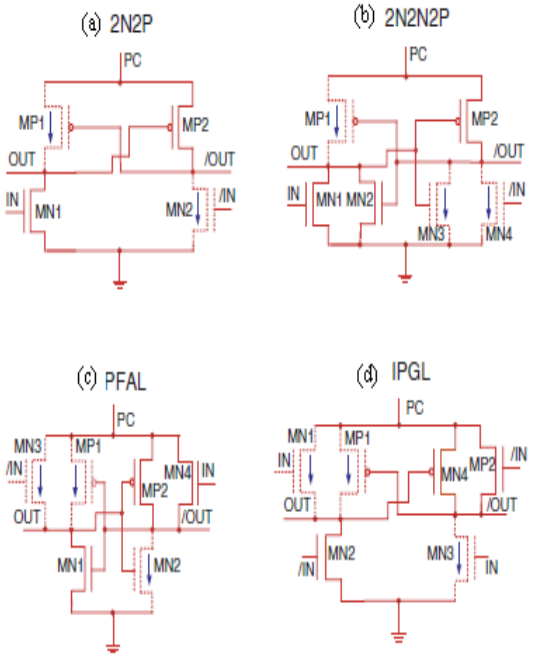


Fig 1 Schematic of Adiabatic circuit families

III. LEAKAGE POWER ANALYSIS OF ADIABATIC CIRCUITS

Figure 1 depict the leak model [6] of adiabatic circuits such as 2N2P, 2N-2N2P, PFAL, IPGL. Consider the leak model of 2N2P Buffer as shown in Figure 1(a) the two cross coupled *p*MOS, MP1 and MP2 provides output charging/discharging for evaluation and recovery processes. When the IN is rising and reaches the threshold voltage, MN1 conducts and makes the OUT low. Simultaneously PC rises and turns MP2 ON with node /OUT rising with PC. At that time, MP1 does not conduct because it is operating in weak inversion region i.e. $V_{th}<V_{gs}$, so it has some amount of subthreshold leakage current. The transistor MN2 passes negligible leakage current due to body effect posed by stacking *n*MOS transistor [7].

The power dissipation components of a CMOS circuit is given by

$$P_{CMOS} = P_{switching} + P_{short\_circuit} + P_{leak}$$
$$P_{CMOS} = C_L V_{dd}^2 + P_{sc} + P_{leak} \quad (3)$$

Where P_{sc} is the power dissipation due to short circuit current and P_{leak} is a combination of the subthreshold leakage power due to non-ideal off-state characteristics of the MOS transistors and gate leakage power caused by carrier tunneling through the thin gate oxides.

The most effective way to reduce the power dissipation is to lower the supply voltage. With the scaling of supply voltage and device dimensions, the transistor threshold voltage also be scaled in order to achieve the required performance. This is because of the decrease in propagation delay when the threshold voltage reduces. As a result, it will increase the leakage current. Due to the exponential nature of leakage current in the subthreshold regime of the transistor, leakage current can no longer be ignored. The transistor off-state current (I_{off}) is the drain current when the gate-to-source voltage is zero. I_{off} is greatly affected by threshold voltage, channel length, channel width, depletion width beneath the channel area, channel/surface doping profiles, drain/source junction depths, gate oxide thickness, supply voltage and the junction temperature.

The subthreshold leakage current plays a dominant role when the device size is below 0.5µm. The subthreshold leakage current can be expressed as

$$I_{leak} = I_0 \exp\left((V_{gs} - V_{th})/\eta V_T\right) \quad (4)$$

Where

$$I_0 = \mu_0 C_{ox} \left(W/L\right) V_T^2 e^{1.8} \quad (5)$$

where η is the subthreshold slope factor, V_T is the thermal voltage, and µp is the mobility of the pMOS transistor in the charging path, µ is the mobility of the leaking *n*MOS/*p*MOS transistor, V_{gs} is the gate to source voltage, Cox is the gate oxide capacitance and W and L are the channel width and length of the transistor under consideration.

The leakage current, due to subthreshold conduction, is computed from I_{leak} when Vgs=0. Then

$$I_{leak} = I_0 \exp\left(-V_{th}/\eta V_T\right) \quad (6)$$

The non-adiabatic energy due to leakage current is expressed by $P_{Leak} = V_{dd} I_{leak} kT$ where k is the number of phases per cycle when leakage current flows through the device. Then the total energy dissipation per full charge-discharge cycle including the leakage loss is

$$E_{diss} = \frac{2R_{on}C_L}{T} C_L V_{dd}^2 + \frac{1}{2} C_L V_{th.p}^2 + V_{dd} I_{leak} kT + E_{opn} \quad (7)$$

$$E_{diss} = \frac{2C_L^2 V_{dd}^2}{T\mu_P (W/L)_p (V_{dd} - V_{th.p})} + \frac{1}{2} C_L V_{th,p}^2 + V_{dd} \mu C_{ox} \frac{W}{L} V_T^2 \exp\frac{V_{gs} - V_{th}}{\eta V_T} kT + E_{opn} \quad (8)$$

From the above Equations (8), the third term is mainly contributed by subthreshold current. It increases exponentially with increasing threshold voltage and also for different technologies. The more number of wider transistors constitutes

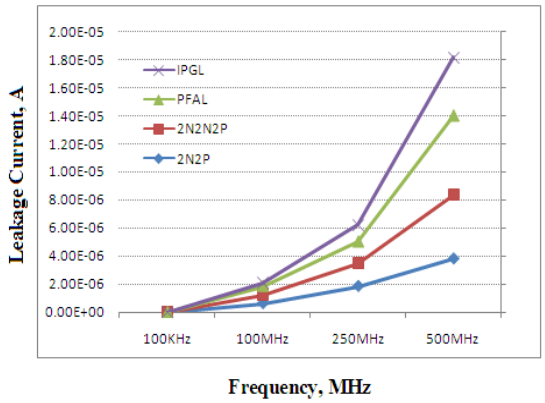
International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 11, November - 2017

the leakage path, the leakage current increases. From Equation (8) it can be inferred that the leakage current is directly proportional to (i) (W/L) x the number of parallel transistors, (ii) V_{dd} (iii) exp (V_{gs} - V_{th}), (iv) T.

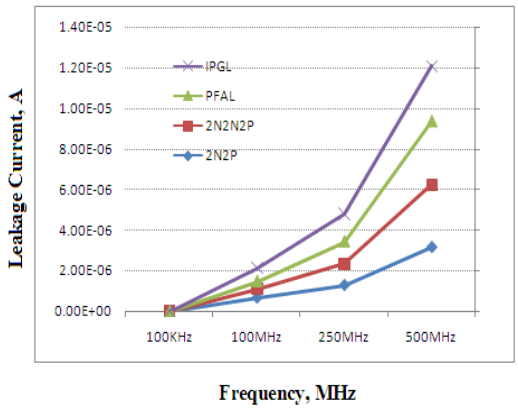
Various design techniques [8] are used to reduce the subthreshold leakage current is (i) by varying the size of the transistors (ii) by varying the threshold voltage. Multiple – threshold CMOS circuit technologies can be used to deal with the leakage problem. These circuits have both high and low threshold transistors in a single chip. The high threshold transistors can suppress the subthreshold leakage current, while the low threshold transistors are used to achieve the high performance.

IV. SIMULATION AND RESULTS

The adiabatic circuits are simulated using standard BSIM3V3 model parameters. Figures 2 (a) and (b) show the effect of different (W/L) ratios on leakage current. The (W/L) ratio for the graphs shown in Figure 2 (a) is $W_{P=}$9µm and (b) is W_P=6µm for V_{dd}=2.5V. L=0.5um was assumed for the simulations. From the graphs it is observed that for increased value of frequency, the leakage current increases as per Equation (5).



(a)



(b)

Fig 2 (a) , (b) Effect of (W/L) ratio on Leakage Current for various Frequency when V_{dd}=2.5V

Table.1 shows the leakage current for adiabatic buffer against the conventional CMOS buffer for different Frequencies with various (W/L) ratio of *p*MOS transistor and V_{dd}. The supply voltage can be varied from 2V to 3.3V. On comparing Figure 2 (a) and (b) the leakage current will increase on increasing the (W/L) ratio of the MOS transistors. In this, leakage current will be increased approximately 42.86%.

Figure 3 (a) shows the comparison of average power of various adiabatic circuits against conventional CMOS for different frequencies. Figure 3 (b) shows the average power comparison of adiabatic circuits. Figure 3(c) shows the average power of conventional CMOS circuits. The average power keeps on increasing when the frequency increases. Figure 4 shows the effect of threshold voltage on Leakage current. From the graph, it is observed that the subthreshold leakage current decreases on increasing the value of threshold voltage of leak transistor because it is directly proportional to exp (V_{gs}-V_{th}).

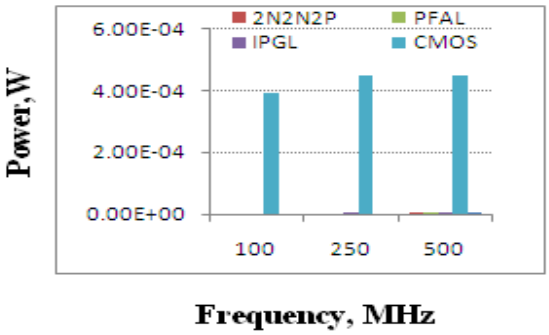


Fig 3 (a) Average Power comparison of 2N2P, 2N2N2P, PFAL, IPGL and CMOS for various Frequencies

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 11, November - 2017

Table.1 Leakage Current for Adiabatic Buffer against Conventional CMOS Buffer for Vdd=2.5v

State	Adiabatic Circuits(µA)				CMOS (mA)	(W/L)p (µm)	Freq
	2N2N	2N2N2P	PFAL	IPGL			
0	-2.61	-0.832	-3.18	-1.21	0.0821	(6/.5)	500MHz
1	-3.14	-3.09	-3.13	-2.72	-0.173		
0	-2.67	-0.868	-18.9	-1.43	0.0983	(9/.5)	
1	-3.83	-4.45	-5.67	-4.11	-0.223		
0	-1.25	-0.275	-2.34	-1.83	0.0798	(6/.5)	250MHz
1	-1.27	-1.07	-1.09	-1.35	-0.179		
0	-1.87	-0.279	-1.28	-0.432	.096	(9/.5)	
1	-1.86	-1.62	-1.55	-1.18	-0.223		
0	-.633	-0.321	-0.407	-0.594	0.0681	(6/.5)	100MHz
1	-0.652	-0.422	-0.40	-0.655	-0.134		
0	-.0153	-0609	-0.617	-0.938	0.0698	(9/.5)	
1	-0.633	-0.620	-0.611	-0.235	-0.155		

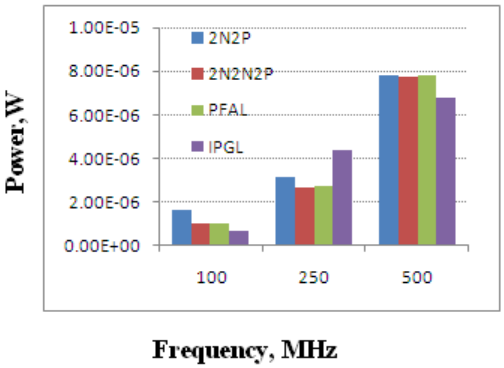


Fig 3 (b)
Average Power comparison of 2N2P, 2N2N2P, PFAL, IPGL for various Frequencies.

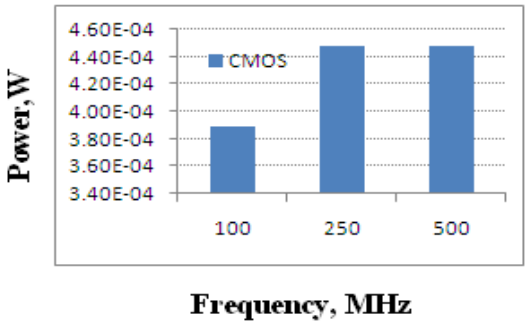


Fig 3 (c) Average Power for conventional CMOS for various Frequencies.

Figure 4 is drawn using the Equation (6).The value of $V_{th,\,p}$ have been taken around in the range of $0.2V_{dd}<V_{th}<0.5V_{dd}$. The threshold voltage of 0.6912V is taken into account for analysis purpose. The subthreshold leakage current can be reduced by varying the size of the transistor or by increasing the threshold voltage.

Figure 5 shows how the leakage current is varied for various (W*p*) values. This graph is computed using the Equation (5). Using the standard BSIM3V3 model parameters, the I_0 value is calculated. The following parameters are used to calculate I_0: μ_0=129e-8µm2/V-s, $V_{gs}=V_{dd}/2$ and V_{th}=0.6915v for varying V_{dd} from 2V to 3.3V.

Figure 6 shows the effect of V_{dd} on Leakage power. From the graph, it is observed that, the leakage power increases linearly with respect to V_{dd} because it is directly proportional to $I_{Leak.}$ The graph is drawn by using the Equation (7).

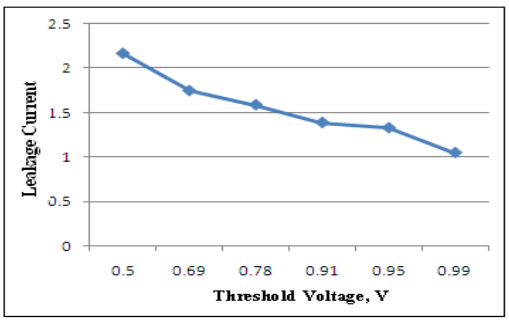


Fig 4 Effect of Threshold Voltage on Leakage Current

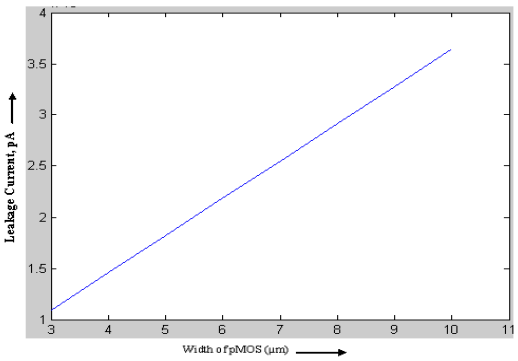


Fig 5 Effect of Width (W) on Leakage current

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 11, November - 2017

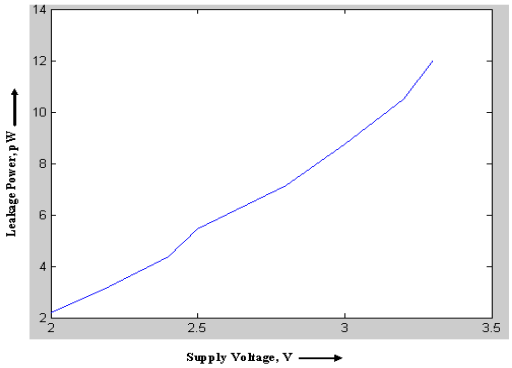


Fig 6 Effect of V_{dd} on Leakage Power

V. SIMULATION AND RESULTS

In this paper, we analyze the leakage current/power of adiabatic circuits such as 2N2P, 2N2N2P. PFAL, IPGL against conventional CMOS circuit. From the analysis, we conclude that, increasing the value of V_{th} reduces the leakage power and also increasing the width (W*p*) of *p*MOS transistor leads to the increase of leakage current. The leakage current can be reduced by increasing the threshold voltage of the MOS transistors. By implementing the Dual Vth design technique, the leakage current can be reduced and also the performance of the circuit will be improved to a great extent.

REFERENCES

[1] W. Athas, L. Svensson, J. G. Koller, N. Tzartzanis, and E. Y.-C. Chou, "Low-power digital systems based on adiabatic-switching principles," *IEEE Transaction., VLSI Systems*, vol. 2, no. 4, Dec.1994.

[2] J. S. Denker, "A review of adiabatic computing," in *Proceedings IEEE Symposium Low Power Electron*, 1994, pp. 94–97.

[3] A. G. Dickinson and J. S. Denker, "Adiabatic dynamic logic," *IEEE Journal Solid-State Circuits*, vol. 30, pp. 311–355, Mar. 1995.

[4] M. C. Knapp, P. J. Kindlmann, and M. C. Papaefthymiou, "Implementing and evaluating adiabatic arithmetic units," *Proceedings IEEE Custom Integrated Circuits Conference.*, 1996, pp. 115–118.

[5] A. Kramer, J. S. Denker, S. C. Avery, A. G. Dickinson, and T. R. Wik, "Adiabatic computing with the 2N-2N2D logic family," in *Proceedings IEEE Symposium, VLSI Circuits Digital Technology Papers*, June 1994, pp. 25–26.

[6] V. S. Kanchana Bhaaskaran, J. P. Raina, "Differential Cascode Adiabatic Logic Structure for Low power", *IEEE Journal Low Power Electronics*, vol.4, 2008, pp.178-190.

[7] M. C. Johnson, D. Somasekhar, L. Y. Chiou, and K. Roy, "Leakage control with efficient use of transistor stacks in single threshold CMOS", *IEEE Transaction on VLSI Systems*, vol.10, 2002.

[8] Low-Power CMOS VLSI Circuit Design," Kaushik Roy & Sharat c. Prasad" A Wiley Interscience Publication, 2000.