Junction Less Semiconductor Components using Nano Wires

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***Abstract*— In this paper , we explore a very new trend in the electronics industrywhich is proved to be a boon for technologies.basically mostly developed semiconductor devices contains a junction or called a potential; barriers for eg. A transistor. We will study here a transistor with no junction and with no doping concentration gradient. It greatly signifies the appropriance of "Moor's Law". Our study revolves around junction less FET as their future in electronics is very radiant. This is done by shielding the gate with uniformly doped nanowires in order to protect them from the . In these devices the channel is uniformly doped without the need for extremely good lateral doping abruptness at channel junction. This type of transistor are based on bulk conduction as in conventional FET's because the purpose of controlling output current is resolved by channel doping and mobility of carriers instead of gate capacitance. One of the most important features of this transistor is low doping of source, drain, channel and the lateral gate regions. Hence development of such devices is the step in the development of the future technology where the devices will be smaller and efficient with low energy consumption.**

Keywords*— *semiconductor, junction, doping, gate, depletion layer, nano-wires

I. INTRODUCTION

Junction less Nanowire Transistor (JNT), developed at Tyndall National Institute in Ireland, was the first transistor successfully fabricated without junctions. Based on the same study and extending it further other devices could easily be possibly made by replacing the junctions by the samal fabricated carbon nanowires or the graphene which will provide them the efficient effect as junctions. Normally Junctions are difficult and expensive to fabricate, and moreover a part of energy or current is being leaked or wasted at the junction which is a big loss if we consider a bulk, they waste significant power and generate significant waste heat. Eliminating them held the promise of cheaper and denser microchips. The JNT uses a simple nanowire of silicon surrounded by an electrically isolated "wedding ring" that acts to gate the flow of electrons through the wire. This method has been described as akin to squeezing a garden hose to gate the flow of water through the hose. The nanowire is heavily n-doped, making it an excellent conductor. Crucially the gate, comprising silicon, is heavily p-doped; and its presence depletes the underlying silicon nanowire thereby preventing carrier flow past the gate.

II. NEED OF TECHNOLOGY

According to **moor's law** transistors has been doubledevery year. So this law is known as the limit for the number oftransistors on the most complex chips. Recent trends show That this rate has been maintained into 2007. The law becamesomething of a self-fulfilling prophecy as microchip andelectronics manufacturers competed to develop faster, smaller,and cheaper electronic devices; by the early 21st cent., thenumber of transistors on a typical memory chip had gone farbeyond 1 billion. It is generally accepted that technologicalimprovements in miniaturization and microelectronics reach apoint where circuits are only a few atoms wide, making it
physically impossible to make them even smaller.Transistors are becoming so tiny that it is becomingincreasingly difficult to create high-quality junctions. Inparticular, it is very difficult to change the dopingconcentration of a material over distances shorter than about10 nm. Junction less transistors could therefore
Helpchipmakers continue to make smaller and smaller devices.

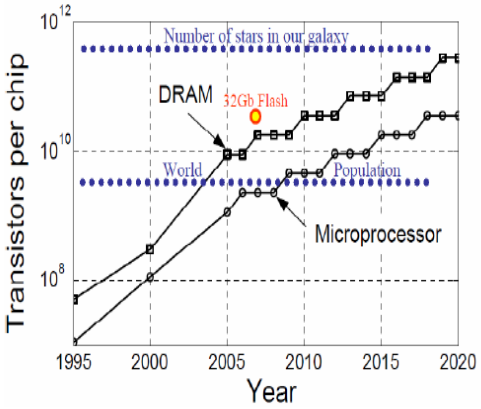


Fig1. Moor's law of evolution

III. BASICSTRUCTURE

The invention transistor and diode-action has dependedon controlling the flow of electrons across junctions givingrise to the familiar NPN and PNP notation for bipolar devices
and p- and n-type FETs with sources and drains. Controllingthe junction allows the current in the device to be

turned onand off and it is the precise fabrication of this junction thatdetermines the characteristics and quality of the transistor andis a major factor in the cost of production.

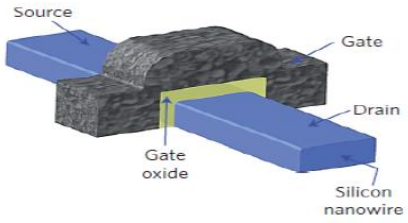


Fig2. Schematic of an n-channel nanowire transistor

The transistor is a field-effect device, much likemodern metal-oxide–semiconductor (MOS) devices. Itconsists of a thin semiconductor film deposited on a thininsulator layer, itself deposited on a metal electrode. The lattermetal electrode serves as the gate of the device. In operation,the current flows in the resistor between two contactelectrodes, in much the same way that drain current flows between the source and drain in a modern MOSFET. Thedevice is a simple resistor, and the application of agate voltage allows the semiconductor film of carriers to bedepleted, thereby modulating its conductivity. Ideally, itshould be possible to completely deplete the semiconductorfilm of carriers, in which case the resistance of the devicebecomes quasi-infinite. The transistor, unlike allother types of transistors, does not contain any junction.A transistor is a solid-state active device that controls currentflow, and the word 'transistor' is a contraction of 'transresistor'.The transistor is a gated trans-resistor; that is, it is a resistor with a gate that controls the carrierdensity, and hence the current flow. It is the simplest and first patented transistor structure; transistor would never have been able to produce a working device.

Modern transistors have reached such small
dimensions that ultra-sharp doping concentration gradients are required in junctions: typically the doping must switch from n-type with a concentration of 1× 1019 cm-3 to p-type with a concentration of 1× 1018 cm-3 within a couple of nanometres. This imposes severe limitations on the processing thermalbudget and necessitates the development of costly millisecond annealing techniques. In a junction less gated resistor, on the other hand, the doping concentration in the channel is identical to that in the source and drain. Because the gradient of the doping concentration between source and channel or
drain and channel is zero, no diffusion can take place, which eliminates the need for costly ultrafast annealing techniques and allows one to fabricate devices with shorter channels. The key to fabricating a junction less gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers When the device is turned off. The semiconductor also needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on. Putting these two constraints together imposes the use of Nano scale dimensions and high doping concentrations. The operation principle of the gated resistor has recently been investigated through simulations by several research groups.

IV. FABRICATION

The junction less nanowire transistor (JNT) is a heavily doped SOI nanowire resistor with an MOS gate that controls current flow. Doping concentration is constant and uniform throughout the device and typically ranges from 1019 and 1020 cm-3. The device features bulk conduction instead of surface channel conduction. Junction less fabrication process is greatlysimplified, compared to standard CMOS since there are no doping concentration gradients in the device.

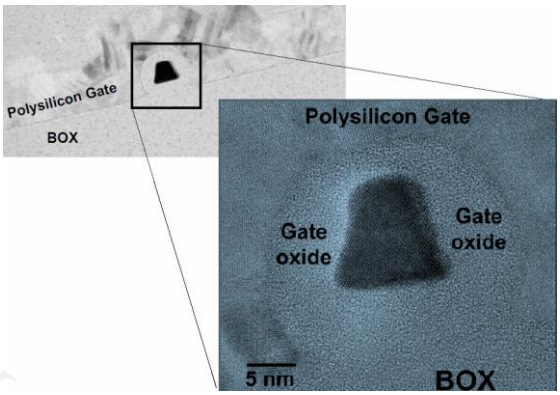


Fig3. Cross sectional TEM picture of transistor showing thestructure of the device.

Junction less nanowire transistors with gate length down to50 nm were fabricated using the process described. The gateoxide thickness is 5 nm and beam lithography was used topattern both the nanowires and the gates. The n-channeldevices were doped using arsenic to a channel concentrationof 5x1019cm-3 and P+ polysilicon was used as gate material.

V. COMPARISON WITH JUNCTION TRANSISTOR

The electric field perpendicular to the current flow is foundto be significantly lower in junction less transistors than inregular inversion-mode or accumulation-mode field-effecttransistors. Since inversion channel mobility in metal-oxidesemiconductortransistors is reduced by this electric field, the
Low field in junction less transistor may give them anadvantage in terms of current drive for manometer-scalecomplementary metal-oxide semiconductor applications. Thisobservation still applies when quantum confinement is present.The major carriers in channel region for a Junction transistormake itself a barrier to carrier scattering, whereas, theJunction less transistor does not have this problem, leading toget a high current drive. The advantage related to the JLtransistors is simple device fabrication due to the eliminationof junction implantation and annealing; hence, a simpleprocess results in a reduced cost. These advantages aredifficult to be achieved for junction transistors. That is whyexcluding the so-called short-channel effects (SCEs) theconventional CMOS devices face lots of critical issues

forachieving low-cost mass production.Both devices are biased in the sub threshold regime with*VDS*=1V and *VG=VTH*-200mV. As expected the peak electricfield of the inversion-mode device is at the drain junction andthe drain electric field extends to some distance in the channelregion, contributing to both increasing DIBL and reducing theoutput impedance. In the junction less device the region ofhigh electric field is in the drain, outside of the region coveredby the gate. It is wider than in the inversion-mode device, andthe peak value is lower. As a result, the influence of the drainelectric field on the channel region is much smaller than in theinversion- mode device, resulting in a smaller DIBL.

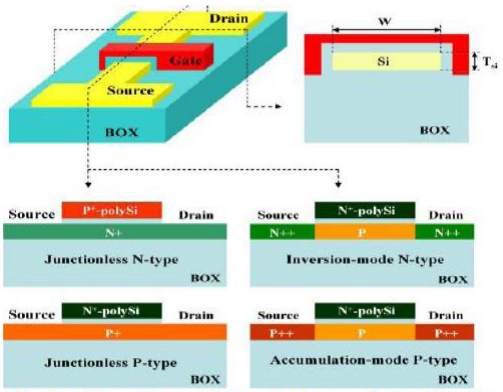
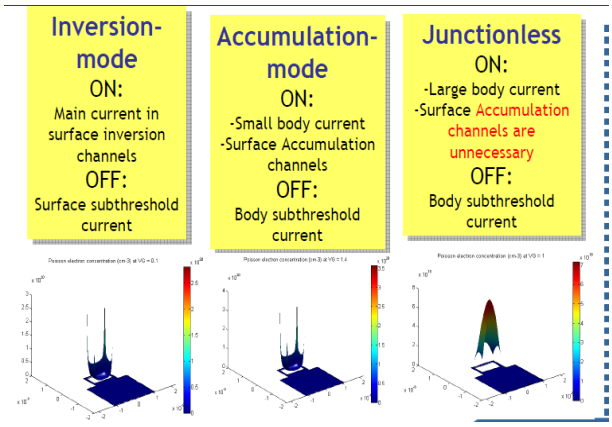


Fig. 6. Comparison of junctionless and junction-based transistors [6]

VI. MODES OF OPERATION OF JLIT

The physics of the JNT is quite different from that ofstandard mitigate FETs. The comparison between all modes is given in the table below.



VII. CHARACTERISTICS OF JLIT

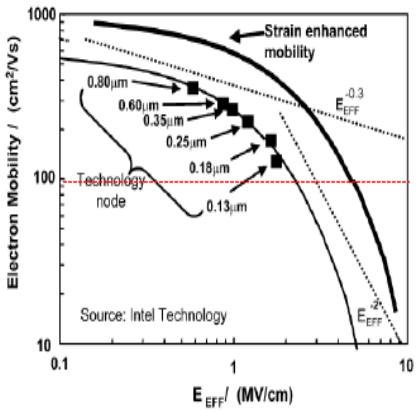


Fig. Mobility Vs. Doping

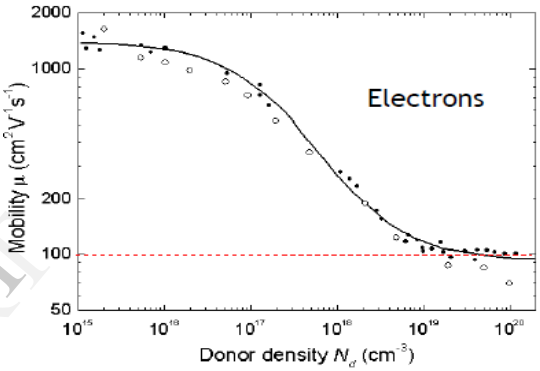


Fig.Relation between mobility and doping.

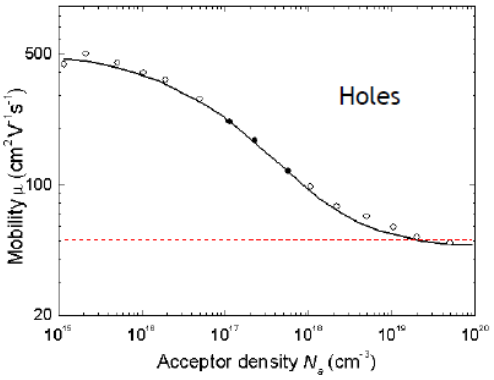


Fig. High doping and mobility

VIII. OTHER COMPONENTS

Various semiconductor devices other then the transistors can be synchronized to limited size with greater efficiency using the technology of nanotech and nano wires. A brief description is as follows.

DIODES: diodes are the combination of p-type and n-type heavily doped semiconductor devices. It could be improved by introducing the graphene between the two which will offers

the same characteristics as the present one is working with the minimum usage of current.it includes **DIAC TRIAC**, gun diode laser diode etc.

SOLAR CELLS: latest developed solar cells make use of the nanotubes for the passage of current through the junctions and to increase the efficiency and reduce the weight of solar cells.

INTEGRATED CIRCUITS AND MEMORIES: all memories and integrated circuits can use the same technologies which will result in the reduced size of it and efficient working.

ALL the sensors, transducers and convertors can be introduced with the internal carbon nanotubes so as to improve the structure and efficiency.

IX. ADVANTAGES

- ✓ Low weight and less size
- ✓ high conductivity
- ✓ quick response
- ✓ less transient time
- ✓ low cost
- ✓ low energy consumption

X. DISADVANTAGES

- ✓ Typical structure
- ✓ Complicated manufacturing
- ✓ High cost of manufacturing

XI. CONCLUSION

This paper presents the ofjunction less transistor and various semiconductor components andcompared with the present ones. Junction less can exhibit lowleakage currents and excellent short channel behaviour at shorter gate lengths.According to moor's law the junction less transistor is best toreduce the size of the transistor with excellent behaviourwhich makes the chipmakers work easy. The electrical characteristics of lightly doped junction less lateral gate silicon nanowire transistors. The fabrication method used is based on AFM nanolithography on SOI substrate. The performance of device is compared to junction less nanowire transistors.

The device uses bulk conduction instead of surface conduction. Controlling the cross section and gate gaps are key parameters for better performance of the device and particularly for sub threshold swing tuning.

XII. SCOPE OF FUTURE

Since coming is the world of small and efficient gadgets which gives us the better efficiency low cost and highly portable. Current technology has acquired much of it but it still demands more. Semiconductor devices play an efficient role in automation and almost every scroll of life. By the introduction of such junction less electronic devices the electronic industry will get a boon and forthcoming devices would be smaller cheaper and efficient. The main advantage of such devices Is the consumption of energy which is quiet low so such devices could easily be made to work in low voltage. This will lead to the decrease in power consumption in the whole world and ultimately in the saving of power which is needed in the world today. Huge transmitters and receivers are used today in order to establish the communication link in which heating is a general problem which could be easily eradicated.

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Sumit Kumar sharma is a 3rd year engineering student of Electronics and communication branch from Apex Institute of Engineering and Technology, Jaipur. He is keen and innovative in research work and has presented his papers in many national and international conferences and has research papers in many soverniers. He has been the project guide for many projects and has two international papers on wireless electricity transmission and winner of hardware presentations at many intercollege festivals. He has been awarded as the pride of the college.