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Inverter Based Transimpedance Amplifier with Capacitive Feedback Topology

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***Abstract*— Trans-impedance amplifier (TIA) is widely used in optical sensing applications (precision instrumentation) and optical communication such as fiber optics, IR communication, and VLC. TIA converts current (I) into voltage (V). Application of TIA design depends on objectives requirement systems, for high speed as well as high-band, low noise, low power, etc. Many different topologies have appeared in different optoelectronics fields, which makes the choice of the best TIA topology for a certain application a challenging task. The proposed TIA is based on shunt-shunt feedback topology as Inverter-based TIA with Capacitive feedback. This methodology is anchored by a design in a 50nm CMOS technology. The photodiode has a capacitance of 100fF, which permits the TIA to achieve a wide bandwidth of 7GHz with a data rate of 10Gbps. It is seen that the proposed TIA provides a Transimpedance gain of 32.7dB-Hz and input cross-referred noise-current spectral density of 13.0pA/Hz1/2 and total RMS noise with 135.23µA.**

***Index Terms*—Current Spectral Density, Photodiode, TIA, VLC.**

I. INTRODUCTION

In the past few years, the continuous trend toward efficient means information dissemination has revived Optical communications, paving way for detailed study in the field of fast and reliable components and the integrated circuit. Communication technology such as cell phones, portable computers with high-speed data processing and high-speed access to store data becomes an interesting issue [1].

CMOS technologies have drastically developed in recent years. Today's world need long battery life for the devices whether it is used in communication application or medical devices or any other field. Thus low power dissipation is the basic need of today's VLSI Circuits. The first structure block in the optical communication receiver is the Transimpedance amplifier, (TIA). The main task of TIA is to changes the small signal current to the output voltage signal. In order to have a better TIA, the two main parameters that must be reckoned with are the bandwidth and the input sensitivity deviation [2, 3]. TIA being the basic circuit for many applications to convert current signal to voltage signal, improvement in its power dissipation is also necessary. Trans-impedance Amplifier (TIA) or another name called as photodiode amplifier, has a function for converting the photodiode photocurrent output (Isc) to a voltage signal (VO). TIA has implemented in various optic application, not only for optical sensing (measurement purpose) but also for optical communication (i.e. IR, VLC, fiber-optic). They are can be built by discrete circuit mechanism, such as: [4], [5], or by MOS transistor circuitry. Its circuit design divided into several aspects, such as precision instrumentation TIA, high speed TIA, low noise TIA [6], gain stability TIA [7], manual programmable TIA [8] and other related objectives.

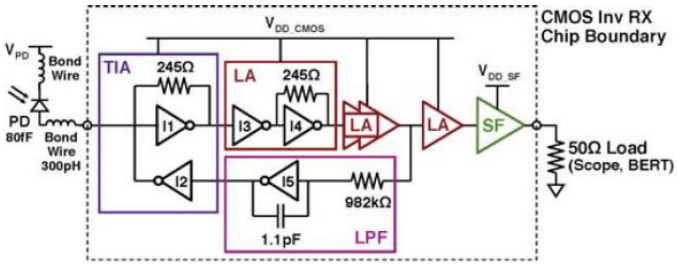

Fig.1 Block Diagram of Optical Communication Receiver [9]

To achieve the above specifications, namely, low input resistance, low output resistance and low noise and high Transimpedance gain, various topologies have proposed. Shunt resistance [12], common gate (CG) circuits [13]; regulated cascode circuits (RGC) [14], common source circuit with shunt feedback [15, 16] and cross-coupled current conveyor [17] are some of them. Each topology provides a part of the specifications required; moreover, it even allows the designer to make some tradeoffs. A designer uses a topology according to the specifications and need, which are required, and reaches those specifications by completing those tradeoffs. In other words, tradeoffs give some degrees of freedom to the designer to meet the specifications required. [18].

Primary parameters for consideration in selecting a Transimpedance amplifier are bandwidth, noise, signal bandwidth, and gain. Avoid a sensor with high capacitance value and even try to avoid creating a capacitance between your sensor and TIA. Avoid a TIA with high voltage noise (nV/√Hz) or high current noise (pA/√Hz). Consider the impedance of your sensor at the very best operating frequency of that sensor specified the product of voltage noise (of the TIA op amp), current noise (of the TIA op amp). Therefore, the aforementioned impedance of your sensor at the highest frequency are as low as you will be able to get them.

The steadily growing bandwidth requirement of data centers, high-performance computers in terms of power consumption, low noise and speed is the major aspects, the mainframe switches the demand for high-speed serial interconnects in optical lines. Electrical interconnect is unable to address this space in a power- and cost-efficient way due to the high-frequency dependent losses of copper wiring [22].

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The commercial optical modules used in high volumes in data centers are pluggable optical modules located at the board edge, distant from the host chip. Integrating optoelectronics on to the first-level package requires a low-cost packaging solution with an optical escape path. High-speed automated packaging tools are preferred, as they are lower cost per part than packaging tools using active optical alignment, where the optical engine is been actively used to optimize the optical coupling [21]. However, high-speed automated packaging tools have worse alignment tolerances, resulting in higher optical coupling losses that stress the optical link budget [21].

In section 2, the proposed topology is been introduced. A circuit based on the proposed topology is been shown in section 3. In section 4, the simulation results of the circuit together with a comparison of our result with other previously reported circuits are been presented. Finally, the conclusion is there in section 5.And at last, Appendix A kept for more information and details.

II. INTRODUCTION TO PROPOSED TOPOLOGY

A voltage amplifier composes Shunt-Shunt Feedback topology with capacitive feedback, with a transfer function given by A(s) and a feedback resistor RF connected between its input and the output. This configuration is been known by "voltage-current" feedback, where a negative feedback network (the feedback resistor) senses the voltage at the output and returns a proportional current to the input.

This type of feedback is chosen for a TIA circuit because it lowers both the input and output resistances, thus increasing the input pole magnitude and allowing the amplifier to absorb the photodetector current, and also yielding a better drive capability. Rest of the equations and information is mention in Appendix A.

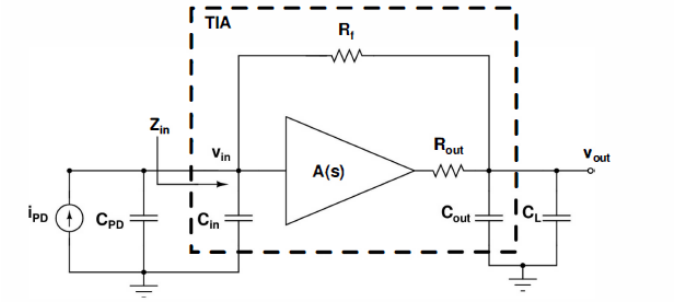

Fig. 2 Shunt-shunt feedback TIA [10]

The A(s) is replaced with inverter based TIA with capacitive feedback as shown in the Fig. 3 below.

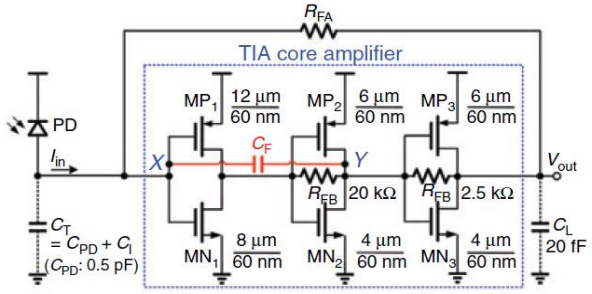

Fig. 3. Inverter based TIA with capacitive feedback [11]

Specifically, a bigger PD usually features a higher responsivity, but it also introduces larger parasitic capacitance at the TIA input, which limits the TIA trans-impedance gain for the specified BW and thus deteriorates the noise performance of the TIA and therefore the whole receiver. Therefore, it is significantly important to scale back the TIA input capacitance for better sensitivity. By employing a little capacitor because the capacitive feedback in the TIA core amplifier, an outsized negative equivalent capacitance is been generated at the TIA input to scale back its input capacitance.

As a result, a higher trans-impedance gain and lower input-referred noise (IRN) current are often achieved within the proposed TIA in comparison to a reference TIA with [11] and without [20,21] capacitive feedback for the BW and Normalized INR. The employment of CF also introduces a zero in the TIA trans-impedance gain, which is Gm/ (2πCF), and Gm is the equivalent transconductance of the non-inverted amplifier between node X and node Y. Since the zero is located far beyond the TIA BW (due to the CF), it has a minimum effect on the TIA frequency response. See Appendix A for more information on capacitive feedback principle and calculations.

III. CIRCUIT BASED OF PROPOSED TOPOLOGY

The proposed TIA is been designed with a 50 nm CMOS process, and the design parameters are presented in Fig. 4 and Table 1.

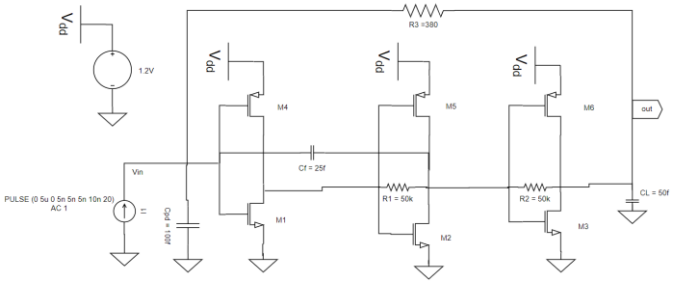

Fig. 4 Schematic of Inverter based TIA with Capacitive feedback.

TABLE I: DESIGN PARAMETERS

Parameters	Values
Vdd	1.2V
W(nmos) (M2,M3)	2µm
W(pmos) (M5,M6)	4µm
W(pmos_cs) (M4)	4µm
W(nmos_cs) (M1)	8µm

The reason of choosing the W (nmos) and W (pmos) as the values mentioned above is the Bandwidth-gain AC analysis. If another width were chosen it will give the Output of AC analysis shown in the figure 5 where, W (nmos) = 4µm and W (pmos) = 8µm.

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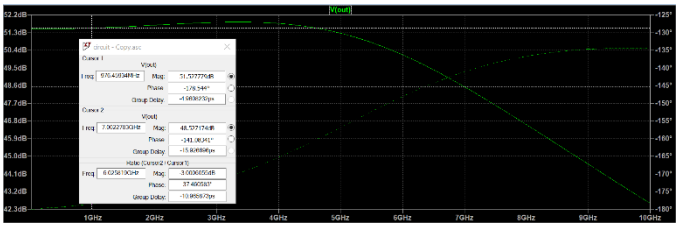

Fig. 5 AC analysis for greater width than proposed topology

Moreover, even if the width are chosen below the parameters shown in Table I, the output of AC analysis is like the figure shown below as Figure 6. As it is not matching the requirement of Bandwidth of 7GHz.

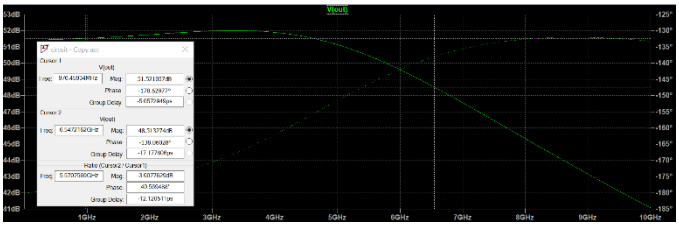

Fig. 6 AC analysis for lesser width than proposed topology

Therefore, the problem with this two approach is the zeta (damping factor) which is affecting the circuit as it produce that notch thing on the upper side.

Moreover, PRBS source is been added. PRBS is add as a source for random binary bits. Binary pulses are generate from pseudo random binary sequence generator as an output it is in a sequence of 1's (High) and 0's (Low) of a known and reproducible pattern. The frequency of an external clock determines the number of bits per second (bit rate) which is use to drive the generator.

From the generator a single bit is transmitted for each clock period, either it is "1" or "0" level, and the width is equal to the clock period and due to this, the external clock is referred to as a bit clock. Random (pseudo) manner is been generated for the distribution of 1's and 0's for a long sequence.

Eye diagram is check-using PRBS, as it required a random number of bits for verifying the output. Figure 7. shows the schematic level diagram of 5 level PRBS source using D-flipflop and gates where the sine wave is given according to the clock frequency = (1/10GHz).

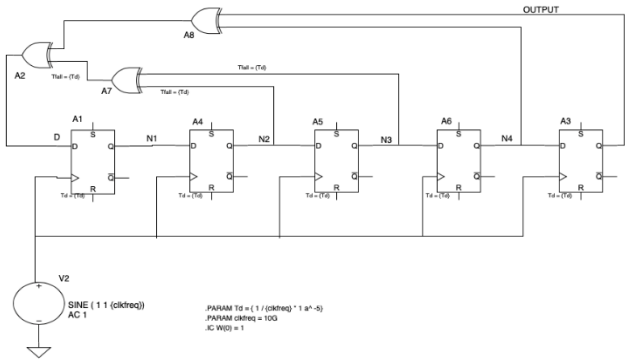

Fig. 7 PRBS source.

As PRBS source gives the output in terms of voltage so, it is needed to convert that into current, So, B1 is used as a source as shown in the Figure 8. Rest of all the parameters should remain constant.

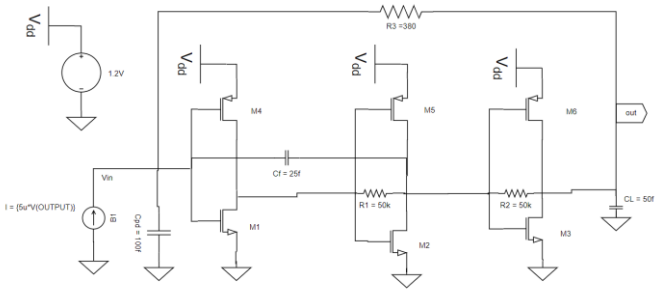

Fig. 8 Circuit with PRBS source.

So, in total the schematic with PRBS source as an alternative of the source is represent in Figure 9.

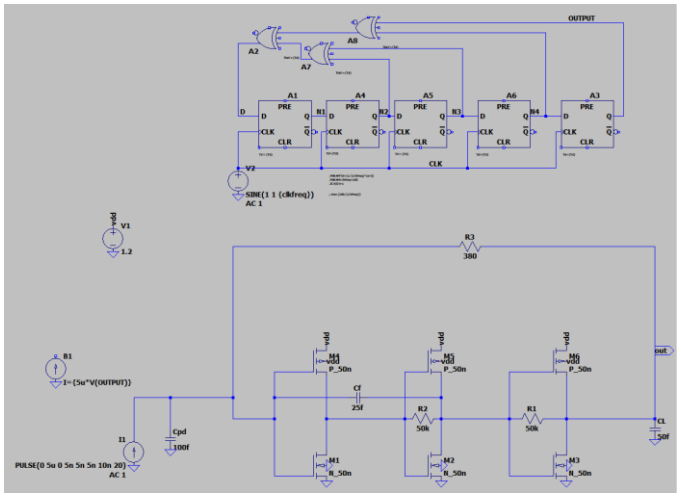

Fig. 9 Inverter based TIA with Capacitive feedback topology with PRBS source.

At 75℃ temperature the circuit is also been implemented with the command of ".temp 75". The results is been shown and described in Section 4.

IV. SIMULATION RESULTS

A. Bandwidth:

The equation to calculate the Bandwidth is BW= Fh-l. Fh is the upper cut off frequency. Fl is the lower cut off frequency. To find the cut off frequency first find the 3 dB points.

Considering the finite BW of its core amplifier, the proposed TIA can be model as a second-order system, and its BW is express as below:

$$BW_{-3dB} \approx \frac{\sqrt{2A_v}}{2\pi R_{FA}(C_T - C_F A_{CF})} \quad (2)$$

Where, A_v is the voltage gain of the TIA core amplifier.

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As shown in the Figure 11. The bandwidth gain (dB-Hz) at 0 ˚ C with -3dB graph fulfilling the condition of achieving 7GHz as a data rate.

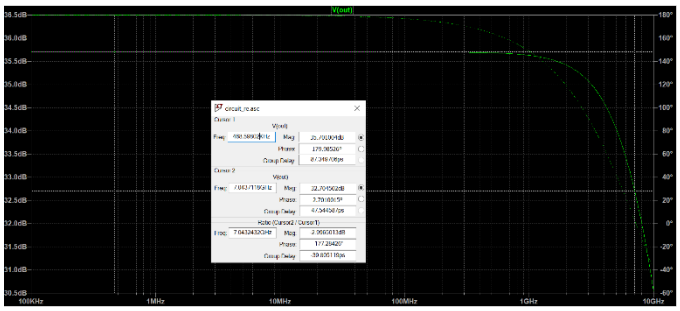

Fig. 11 Bandwidth-Gain Graph at 0 ̊C

Since there is no built-in gain (Vout/Vin) plotting function available in the software, we can just plot the output voltage by setting the input voltage amplitude equal to 1 for the AC analysis. To get the transfer function, you can just subtract the output voltage dB value by 0dBV, which indicates the dB value of the output voltage equals to the gain.

For temperature at 75 ̊C, the graph is improper or we can say it is unstable shown in the Figure 12. As the data rate decreases to 5.04GHz frequency which is not according to the requirement.

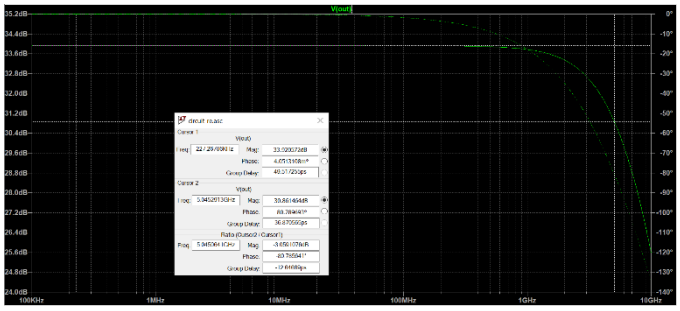

Fig. 12 Bandwidth-Gain Graph at 75 ̊C

Even if I increased my input 10 x to the sensitivity limit, my system should works the same and it is as expected as shown in the figure 13.

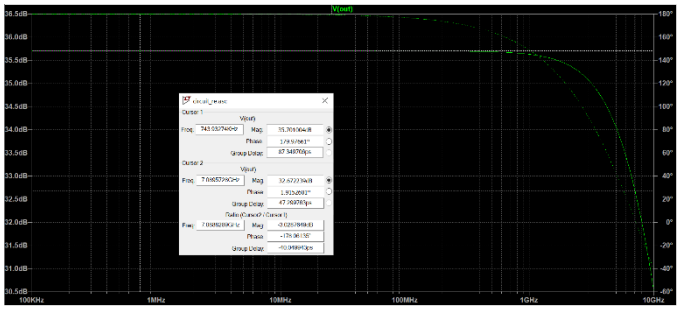

Fig. 13 Bandwidth-Gain Graph with 10x input

As Figure. 11 is simulated at 5µA and Figure. 13 is simulated at 50µA current input. See Appendix A for more information and details.

B. Noise Analysis:

The noise performance is a very significant issue of high-level characteristics of an RF transceiver. The small current of the photodiode is directly affects the signal to noise ratio (SNR) and the overall bit error rate (BER). The equivalent input noise level should be very small to ascertain that the receiver works at a reasonable sensitivity rate with a low bit-error- rate [19].

As the flicker noise does not have effect in MOS transistor, it can be neglected and the terminal noise becomes the main source of the noise.

At discrete frequencies, using a linearized version of the circuit small signal analysis can be carried out, as it is a noise analysis. The mechanics of small signal analysis are very similar to those of an AC analysis.

Assuming the TIA noise is been dominated by MP4 and MN1 and R3, then its IRN current power spectral density can be expressed as below (3):

$$I_n^2(w) = \frac{4kT}{R_{FA}} + 4kT\gamma \frac{1+(\omega R_{FA} C_T)^2}{g_m R_{FA}^2} \quad \text{, If } C_F << C_T \qquad (3)$$

The input referred noise (IRN) is shown in the Figure 14 below at 0 ̊C with 13.00pA/Hz$^{1/2}$ and the total RMS noise is 135.23µA.

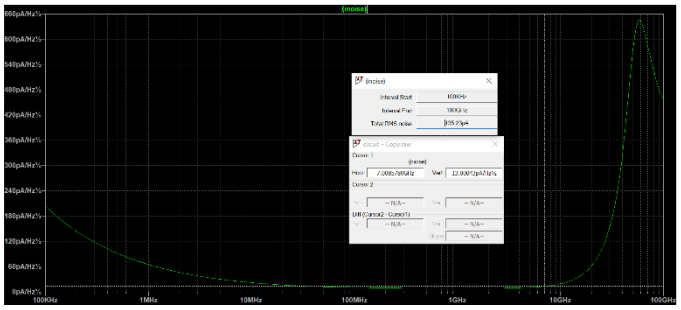

Fig. 14 INR at 0 ̊C

The output noise V(onoise) is shown in the Figure 15 below at 0 ̊C with 3.462nV/Hz$^{1/2}$ and the total RMS noise is 424.46µV. Voltage noise spectral density is a measurement of RMS noise voltage per square root hertz (or commonly nV/Hz$^{1/2}$)

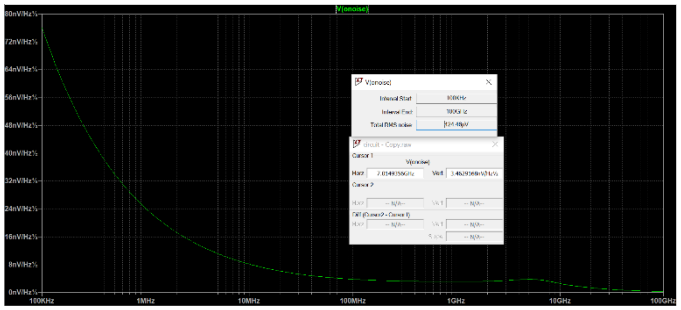

Fig. 15 Output noise in terms of voltage at 0 ̊C

At 75 ̊C, definitely, the system reacts due to increment in temperature over here the input referred noise (IRN) increases

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compared to 0 ˚C due to the capacitance, as due to the temperature increment the internal structure of capacitor get affected.
In addition, for resistor, as temperature goes up the resistance goes up as it shows linear characteristics. So, their presence affects the system, output is shown in the Figure 16, below with 14.86pA/Hz$^{1/2}$ whereas, the total RMS noise is 122.31µA.

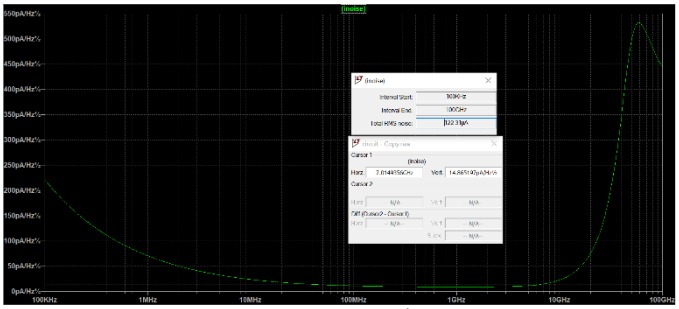

Fig. 16 IRN at 75 ˚C

Even if I increased my input 10x to the sensitivity limit, my system works same as shown in the figure 17 with same INR value. The normal system works as 5µA, which is increased, to 50µA to check the reliability of the system.

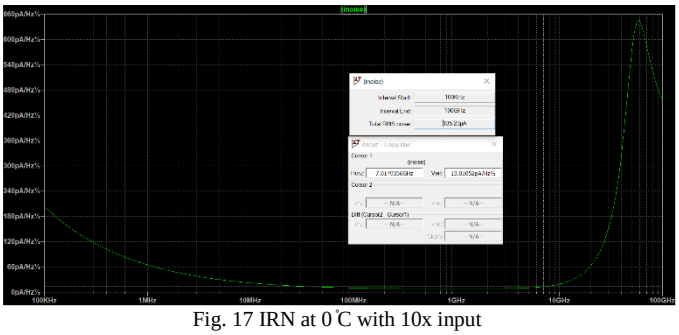

Fig. 17 IRN at 0 ˚C with 10x input

For more information and detail, see Appendix A.

C. Eye diagram

To be quick in visualization and determined the eye diagram that allows the key parameters of the electrical quality of the signal, as the eye diagram is a methodology to represent and analyze a high-speed digital signal data.
Just as a human eye appearance, the eye diagram takes its name. From superimposing the passive waveform to form the image, it is been created with very simplicity. For the purpose of recognizing the effects of distortion and finding its source, eye diagram is been used to look at digital signal in a primary manner.
The eye diagram is been shown below in Figure 18. At 0 ˚C,

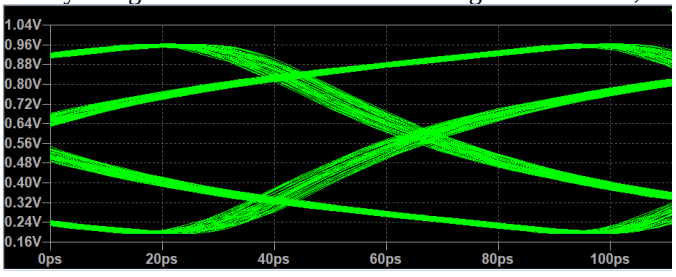

Fig. 18 Eye diagram of the circuit at 0 ˚C

The vertical eye opening on the Figure 18 is 420mV. The simulated data rate is 10 GB/s (BW/0.7) with a voltage swing of 760mV$_{p-p}$ as indicated in Figure 16.

For temperature at 75 ˚C, the system is getting worse, the vertical eye opening became smaller compared to the normal system with 390mV with an voltage swing of 730mV$_{p-p}$ as shown in the Figure 19 below.

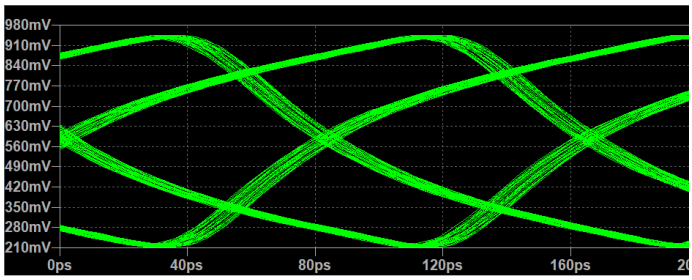

Fig. 19 Eye diagram of the schematic at 75 ˚C

Again, it is been simulated at the data rate of 10 Gbps (BW/0.7).
Even if increasing the input 10x to the sensitivity limit, the system should works the same and it is as shown in the figure 20 with same eye diagram value. The normal system works as 5µA, which is increased, to 50µA to check the reliability and stability of the system.

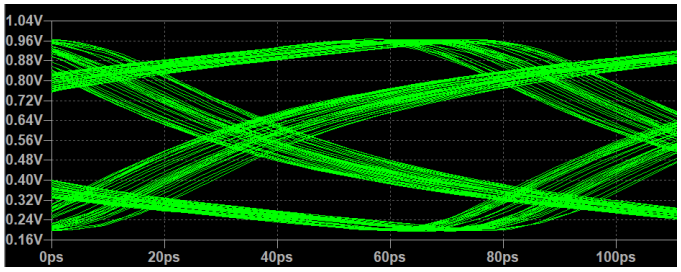

Fig. 20 Eye diagram of the schematic at 0 ˚C with 10x input

For more information and details, see Appendix A.
The PRBS source is added as a source instead of normal source for having random number of binary bits to check the reliability of the circuit. Usually 3, 5, 11 level PRBS source are available which will generate random number of bits using flip-flops and gates.
5-level PRBS source is been used as shown in the circuit, Figure 7 and Figure 8. The output of using PRBS is shown below in Figure 21.

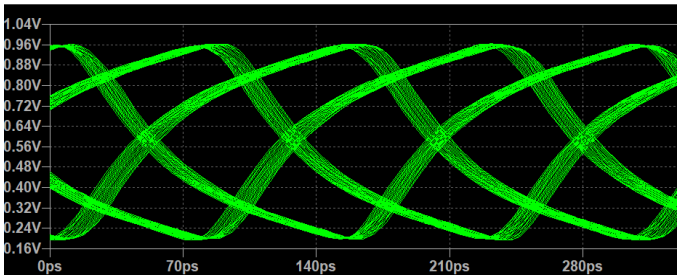

Fig. 21 Eye diagram of the circuit at 0 ˚C with PRBS source

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The VEO (Vertical Eye Opening) of the system output shown above is 430mV with the voltage swing of 780mV$_{p-p}$ at the desired data rate of 10Gbps.
For 75 ℃ temperature, the system output is been shown in Figure 22 below, the VEO is being smaller compared to the normal PRBS source system with 340mV having the voltage swing of 700mV$_{p-p}$.

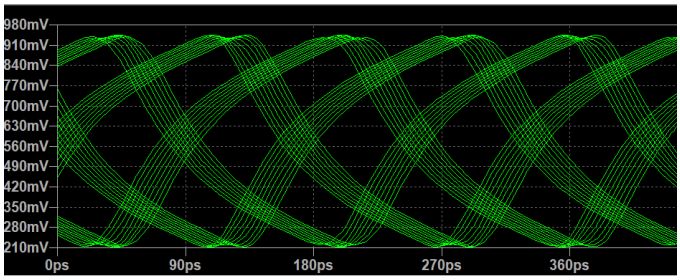

Fig. 22 Eye diagram of the circuit at 75 ℃ with PRBS source

Even if increasing the input 10x to the sensitivity limit, the system should works identical and it is as shown in the Figure 23 with same eye diagram value. The conventional system works as 5µA, which is increased, to 50µA to examine the reliability and stability of the system.

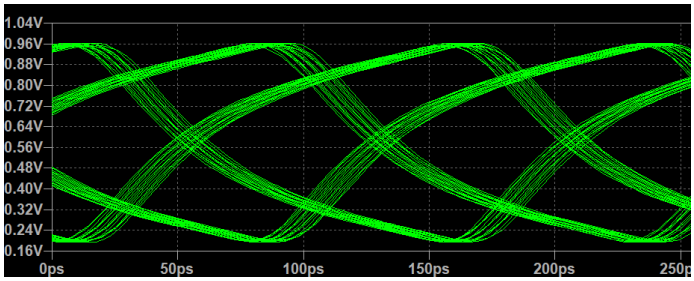

Fig. 23 Eye diagram of the circuit with PRBS source having 10x input.

An eye pattern provides the following information about a particular system. To estimate the bit error rate and the signal-to-noise ratio is the actual usage of eye-pattern. The Width of VEO defines the interval with respect to time over which the received signal can be sample without any error from ISI.

Table two, summaries the performance of different TIAs. Compared to the reference TIA, the proposed TIA is having low IRN, and achieving good VEO as shown:

TABLE II: COMPARISON OF PARAMETERS WITH DIFFERENT DESIGNS

	[20]	[21]	[11]	Proposed Design
Technology(nm)	65	14	40	50
Vdd(V)	1.2	1.2	1.2	1.2
Data Rate (Gbps)	10/12	32	4.3	10
Input Capacitance Cpd(fF)	100	69	500	100
Feedback Capacitance(fF)	N/A	N/A	12.3	25
Feedback Resistance (R3) (Ω)	20k	700	29.9k	380
-3dB bandwidth (GHz)	3.5	8	3	7
IRN(A_{rms})[b]	0.4µ	0.83µ	0.43µ	135.23µ
Normalized IRN[a]	4.6m	4.4m	3.7m	1.93m
INR current power spectral density (pA/Hz$^{1/2}$)	N/A	N/A	0.75	13
VEO(V)	61m	5m	70m	420m

[a]Normalized IRN = INR (A_{rms})/$\sqrt{(C_T \times (BW(GHz))^3)}$, based on (1) in [21].
[b]Simulated result.

The proposed TIA has the lowest input referred noise current when compared to other state of design. The outstanding performance was been achieved by applying the design flow methodology, optimizing the design and the noise modeling proposed in this work.

Circuit Optimization works in a great manner for having low Normalized INR. As the width of the nmos and pmos gets half compared to [11]. The value of feedback resistance is also decreased which plays an important role in that, whereas the value of feedback capacitance increases to achieve the proper result. The principle of capacitive feedback is been discussed in Appendix A.

In order to verify the effective nature of proposed capacitive feedback, a reference TIA is been taken to compare [11]. The difference is that the reference TIA is having different value of feedback capacitance C_F, and even a reference TIA is been taken where no capacitive feedback is there [20] to compare the performance.

CONCLUSION

A complete design flow and implementation of low-noise CMOS Transimpedance inverter based capacitive feedback system were proposed in this work. TIA have wide range of applications such as communication, medical devices and so on. All application demand the long life for proper functioning and portability of devices. The proposed circuit is based on shunt-shunt feedback topology. The experimental results show that the proposed schematic has the lowest normalized input referred noise (INR) compared to other state of art design. The proposed circuit has 50nm CMOS technology and the obtained transimpedance bandwidth ensure a 10Gbps data rate with 7GHz Bandwidth. It uses 380Ω feedback resistor and generally improves the noise performance with 13.00pA/Hz$^{1/2}$ and A_{rms} of 135µA. By employing capacitive feedback of 25fF in the proposed TIA, a higher trans-impedance gain and better noise performance are been achieved.

APPENDIX A

To calculate different parameters different analysis at different stages are been done. Transient analysis is performed for Eyediagram whereas, AC analysis is been done to perform Bandwidth-Gain graph. Moreover, operating points are the first thing, which is been carried out for checking the regions of nmos and pmos. Noise analysis is perform to check input refereed noise current and output refereed noise voltage. Certain aspect like changing the temperature and increasing the input to 10x with sensitivity limit is been done using command like, for temperature ".temp 75" is used.

The first and the foremost thing after selecting the circuit is to create the transfer for it and to select the parameters like resistor

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and capacitor. The value of resistors (R1 and R2), which are used as feedback between the MOS transistors, are carried out by taking, performing and verifying different values of it. Over here, R1 and R2 are been taken as 50kΩ and 50kΩ both as if any another value is taken it is affecting the AC analysis i.e., Bandwidth graph by giving the damping factor (ζ) more than 0.707, and having a zeta more than that will affect the output of the graph by giving the notch shown in Figure 5.

The value of load capacitor is even been chosen like that only by varying it with different values and verifying it while doing AC analysis to get the Bandwidth-gain graph (dB-Hz).

A. *Transfer Function of the circuit:*

The Transfer Function of a circuit is been defined as the ratio of the output signal to the input signal in the frequency domain, and it applies only to linear time-invariant systems.

$$H(s) = \frac{V_{out}}{I_{PD}} = \frac{\frac{Vin}{\frac{Vin-Vout}{R}}}{1+j\omega R_C}$$

$$= \frac{R3}{K+1} \frac{1+j\omega\tau}{1+j\omega\left(\frac{\tau}{K+1}\right)(1+j\omega RC)}$$

$$= \frac{R3}{K+1} \frac{1+j\omega\tau}{1+j\omega\left(\frac{\tau+RC_{PD}}{K+1}+RC_L\right)-\omega^2\left(\frac{\tau R(C_{PD}+C_L)}{K+1}\right)}$$

$$= \frac{R3}{K+1} \frac{1+s\tau}{1+s\left(\frac{\tau+RC_{PD}}{K+1}+RC_L\right)-s^2\left(\frac{\tau R(C_{PD}+C_L)}{K+1}\right)} \quad (A.1)$$

Where, τ = Time constant, K = voltage gain

B. *Principle of Capacitive Feedback:*

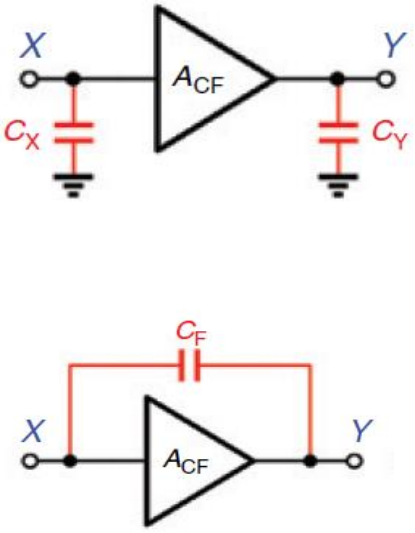

Fig. A.1 Capacitive Feedback Principle Explanation figure between point x and y[.11]

With reference to figure 3. The calculation of C_F is been done using this principle between the point X and Y.

If $A_{CF} >> 1$, then

$C_X = C_F(1-A_{CF}) \approx -C_F A_{CF} < 0$ (A.2)

$C_X = C_F(1-1/A_{CF}) \approx C_F.$ (A.3)

It is clearly shown in (2) and (3) that the employment of CF reduces the TIA input capacitance from (C_T to (C_T–C_F*A_{CF})), and therefore a higher R_F can be applied to achieve a higher trans-impedance gain and a lower IRN while maintaining the same BW and the same A_V.

C. *Bandwidth:*

Even at 10x input when, that 75°C aspect is been checked it shows the following result:

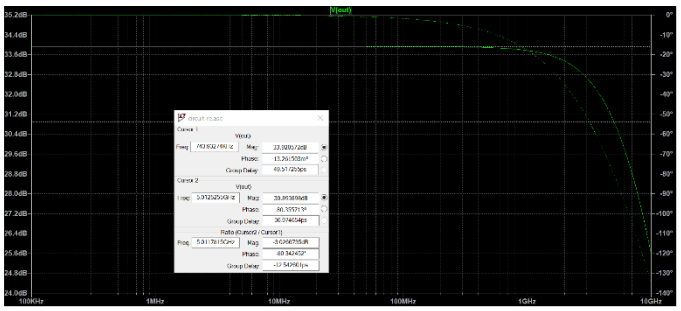

Fig. A.2 Bandwidth-Gain graph at 75°C when 10x input is provided

The output of the bandwidth-gain graph comes at 5.01GHz rather than 7GHz, which is the aimed Bandwidth.

D. *Noise Analysis:*

For Noise analysis, there are certain equations, which we have to follow:

$$i^2_{n,in,TIA} \cong i^2_{n,Rf1} + i^2_{n,Rf2} + i^2_{n,ind} + i^2_{n,incas,cas2} \quad (A.4)$$

$$V^2_{n,in,cas} = \frac{V^2_{n,out,cas}}{A^2_{v,cas}} \quad (A.5)$$

Where, $A^2_{v,cas}$ is the voltage gain.

$V^2_{n,in,cas}$ Is the input referred noise voltage and

$V^2_{n,out,cas}$ Is the output noise signal

For, input referred noise current,

$$V^2_{n,out,cas} \cong i^2_{n,in,cas}\left(\frac{1}{C_{in}\omega}\right)^2 (g_m * R_{out}, cas)^2$$

Where, $i^2_{n,in,cas}\left(\frac{1}{C_{in}\omega}\right)^2 = V^2_{n,in,cas}$

$$i^2_{n,in,cas} \cong (i_n\omega)^2 * \{\frac{4kTR3[\gamma R0gm_i]+1}{(g_{m,Rout,cas})\text{^}2}\}$$

After simplifying according the circuit diagram,

$$I^2_n(w) = \frac{4kT}{R_{FA}} + 4kT\gamma\frac{1+(wR_{FA}C_T)^2}{g_m R^2_{FA}} \quad (A.6)$$

Output Voltage noise at 0°C is been added in the paper, whereas at 75°C it is shown below with 3.53nV/$Hz^{1/2}$ and the total RMS noise is 448.38μV.

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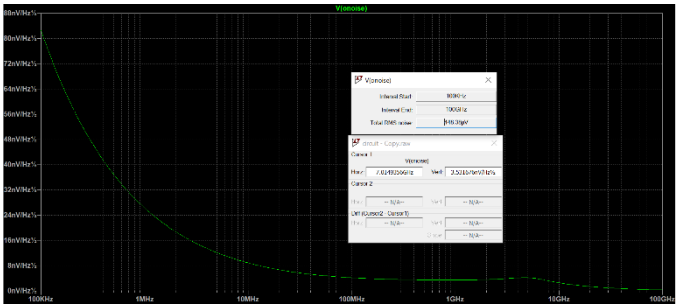

Fig. A.3 Noise analysis in terms of Voltage graph at 75℃

Even if I increased my input 10x to the sensitivity limit, my system works same as shown in the figure below. The normal system works as 5µA, which is increased, to 50µA to check the reliability of the system with the value of 424.46µV as a total RMS noise value and 3.462nV/Hz$^{1/2}$ as the output noise voltage.

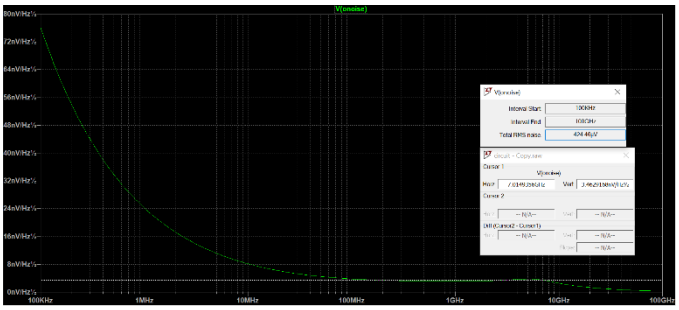

Fig. A.4 Noise analysis graph in terms of voltage at 75℃ when 10x input is provided

E. Eye-Diagram

Eye diagram at input with 0℃ is been shown in the figure below which is having the Vertical Eye opening of 200mV.

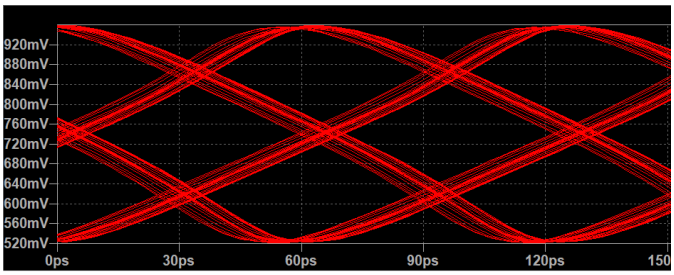

Fig. A.8 Eyediagram at input side with 0℃

Eye diagram at 10x input than sensitivity at 75℃ is shown below in the figure:

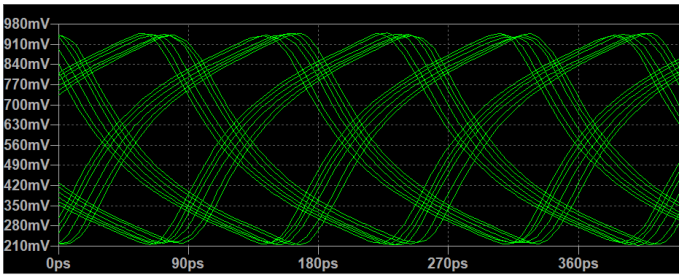

Fig. A.6 Eyediagram at 75℃ when 10x input is provided

The VEO of the figure above is 340mV with 720mV$_{p-p}$.While adding PRBS source as an input.
In the circuit, I1 is been replaced with IB, where IB should be a current source; therefore, the V (OUTPUT) is converted as,

IB = {(input-current of the system)*V (OUTPUT)} (A.7)

e.g., IB = {5u*(V (OUTPUT))}

While, increasing the output at 75℃ to 10x times than the sensitivity limit the system reaction is been indicated in the figure below:

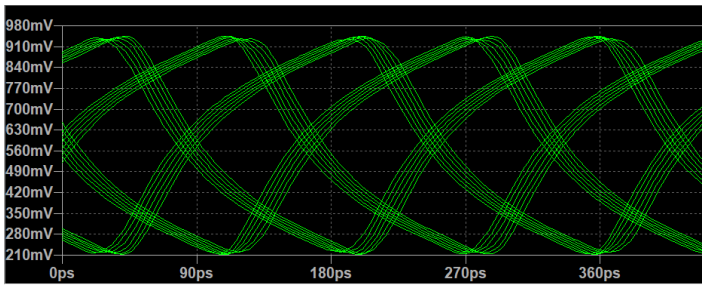

Fig. A.7 Eyediagram at 75℃ when 10x input is provided with PRBS source.

The VEO of the above figure is 390mV with 720mV$_{p-p}$.

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