Interface Trap Analysis of HIGH-K MOSCAP Using T-CAD

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Abstract- Considerable challenges are encountered with poly silicon gate as the channel length and gate-oxide thickness is aggressively reduced in case of CMOS devices when scaled into submicron regime. Metal gates and alternative gate dielectrics with high permittivity shows promising results to overcome the limitations like high gate resistance, high gate tunneling leakage current and boron penetration into the channel region. Therefore, there is immense interest in electrical characterization of a metal-oxide-semiconductor (MOS) capacitor structure with high-K dielectrics. Here capacitance-Voltage (C-V) characteristics of metal-oxide-semiconductor (MOS) capacitor is plotted for high-k dielectric materials such as, Al2O3, HfO2, TiO2, Y2O3 as oxide material, Si as substrate and compared it with conventional SiO2 based MOS device. The MOSCAP structure was simulated to obtain the C-V characteristics using TCAD. From the results various parameters such as threshold voltage, flat band voltage, interface trap density etc. were calculated. The simulation results were then verified with the reported experimental values.

Key words: Al2O3, HfO2, TiO2, Y2O3

I. INTRODUCTION

Considerable challenges are encountered when bulk CMOS devices are scaled into the sub-45nm regime for higher integrated circuit (IC) density and performance. The problems of polysilicon gate depletion, high gate resistance, high gate tunneling leakage current, and boron penetration into the channel region become more severe as the channel length and gate-oxide thickness are aggressively reduced. Therefore, there is immense interest in metal gates and alternative gate dielectrics with high permittivity K [1]. To date, Hf- and Zr-based high-k gate dielectric materials are the most common studied by academia and industry. Other alternative high-k dielectrics available for submicron MOSFET are Al2O3, TiO2, Y2O3 and HfO2. In this paper these above dielectrics are used as insulator in MOS instead of SiO2 due to their wide bandgap, high decomposition temperature, and low electrical, but high thermal conductivity [3]. This will in fact enhance the lifetime, stability, reliability and signal to noise ratio of such devices. The high-k/metal gate combination is also important for enabling future high-performance and low gate leakage emerging nano electronic transistors built upon non-silicon high-mobility materials, e.g. Ge, carbon nanotubes, and III-V substrates. The aim of this paper is to study the capacitance-voltage characteristics of Al/high dielectric/Silicon structure, measure the interface trap charges and the very cause of leakage current are brought into focus.

II. MODEL DETAIL

A. Properties of high K dielectrics

With the scaling of the MOS-device ultra-thin SiO2 suffers some unsolvable issues. Therefore, it is necessary to replace the SiO2 with a thicker layer of higher dielectric constant. For high-k dielectric the K value should be greater than 10 where as 25-30 is preferable. However there is a trade off between high K value and band offset. The energy band gap and band offsets of some dielectric are summarized in table I.

<table>
<thead>
<tr>
<th>Gate Dielectric Material</th>
<th>Dielectric Constant (k)</th>
<th>Energy Band Gap Eg (eV)</th>
<th>Conduction Band Offset ΔEg (eV)</th>
<th>Valance Band Offset ΔEc (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO2</td>
<td>3.9</td>
<td>9</td>
<td>3.5</td>
<td>4.4</td>
</tr>
<tr>
<td>Al2O3</td>
<td>8</td>
<td>8.8</td>
<td>3.7</td>
<td>4.7</td>
</tr>
<tr>
<td>Y2O3</td>
<td>13</td>
<td>6</td>
<td>2.3</td>
<td>2.6</td>
</tr>
<tr>
<td>HfO2</td>
<td>25</td>
<td>6</td>
<td>1.5</td>
<td>3.4</td>
</tr>
<tr>
<td>TiO2</td>
<td>80</td>
<td>3.5</td>
<td>1.1</td>
<td>1.3</td>
</tr>
</tbody>
</table>

TABLE- I: Electrical Properties of High K dielectrics
B. Preparation

In the present work, simulation was carried out on Al/Gate Oxide/Silicon MIS structure using atlas version 5.10.0.R TCAD of SILVACO. The structure of MOS capacitor is with an area of 3.976 x 10^-4 μm^2. Here the insulator part is selected to be of thickness 0.225μm. The semiconductor is 280um thick p-type silicon, uniformly doped with 5 x 10^14 cm^-3 acceptors. In our structure the bulk dimension is very large. Here Aluminum is used for forming gate and substrate contact of area 3.1459 x 10^-8 μm as shown in fig.1 below. While simulation material properties of gate oxide at room temperature like band gap, permittivity, etc. has been declared from [15] so as to include it into the material library. Appropriate models were declared such as cvt and _srh to take care the physics [15]. The CV curve was obtained and analyzed by applying a small AC voltage with different frequencies from 10Hz – 1MHz in steps.

III. RESULT AND DISCUSSION

A. High Frequency CV Plots:

The bulk of the MOS capacitor structure is consisting of both majority charge carrier and minority charge carrier. With external applied voltage the majority carriers can respond immediately but for minority carriers the response time is more. If the applied potential changes so quickly that the polarity across the MOS gate changes before the minority carriers could respond to the applied field, the applied field is said to have a high frequency [7]. Here with negative gate bias, p-type „Si” is in accumulation and we measure simply the capacitance of the parallel plate capacitor with various dielectric layers as dielectric. As gate voltage is more positive then the flat band voltage (Vfb), a depletion layer is formed in the semiconductor. This creates a capacitor in series with the oxide capacitor and produces a drop in total capacitance. When the gate voltage exceeds the threshold voltage a layer of inversion charge is formed, and if the gate voltage is slowly increased further, the inversion layer increases till charge to balance of the gate but for the measurement of positive charge the depletion layer doesn’t widen further. Since the depletion region width is reached maximum, the total capacitance pegged to minimum. The structure is simulated at relatively high signal frequency i.e. 1MHz.Fig.3 (a). As shown in Fig. the HF-CV characteristics of MOS capacitors with tox= 0.225um were measured for a small signal frequency, f = 1MHz, and at a slow DC sweep rate, 1 V/s.

As there is no charge is generated in ideal condition, the capacitance value is decrease in a rapid rate compare to the SiO_2. Hence the high frequency capacitance value is less in this case.

B. Interface Tarp Density (Dit)

The interface states are located at or very close to the semiconductor/oxide interface with energy distributed along the band gap of the semiconductor. Electrons or holes get trapped in these states and act like charges at the interface. It is due to the incompletely oxidized „Si” atom with unsatisfied dangling bond located in the oxide. The charge associated with Dit may be positive, neutral or negative or in fact may change during normal device operation because of capture of electron or holes. Interface trap charges also known as interface trap or interface state Fig.3(b) [8].When a voltage is applied the interface trap levels move up or down with the valance and conductance band, while Fermi level remain fixed. An interface trap is considered as a donor if it can become neutral or positive by donating an electron. An acceptor interface trap can become neutral or negative by accepting an electron [9].
In order to evaluate the interface trap density $D_{it}$, we can use either capacitance measurement or the conductance measurement. Here the $D_{it}$ is determined in the room temperature 1 MHz C-V curves with the standard high frequency capacitance method. Using the relation between depletion region capacitance, insulating capacitance and the slope of a surface potential $\Phi_s$ and C curve $\frac{d\Phi_s}{dV}$ we can calculate the interface charge density $D_{it}$. Here the structure is simulated at gate voltage 0V to +15V Fig.3(c). As the DC voltage increases the $D_{it}$ increases, and at higher voltage there is hardly any changes in interface trap charge density.

Again the reduction of depletion region capacitance reduce the interface electronic state density, which indicates the reduction of interface trap charge density and presence of dangling bond.

gradually increases in ideal condition compare to the experimental condition near the interface. The capacitance value is minimum in this case. So the Dit values of the mos capacitor using various dielectrics are given in table-II.

<table>
<thead>
<tr>
<th>Dielectrics</th>
<th>$D_{it}$ (cm$^{-2}$ eV$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>$6.4 \times 10^{11}$</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>$4.48 \times 10^{11}$</td>
</tr>
<tr>
<td>Y$_2$O$_3$</td>
<td>$3.89 \times 10^{11}$</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>$2.19 \times 10^{11}$</td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>$2.02 \times 10^{11}$</td>
</tr>
</tbody>
</table>

IV. TEMPERATURE DEPENDENT CHARGE BEHAVIOR

It is obtained by correlating the effect of temperature on the charges present at interface and in insulator (gate oxide) deposited on silicon substrate. Figure below shows the attained result of an analysis made by using capacitance-voltage (C-V) techniques at different measured temperatures [6]. The shift in the C-V curves towards positive voltage with increase in temperature, which indicates diminish in the positive insulator charges (sum of the fixed insulator charges, mobile ionic charges, and the trapped charges in the insulator). Theoretically at room temperature ($25^\circ$C), the minority carriers do not follow the high frequency (1 MHz) signal, but at higher temperature the deviation was clearly visible towards the higher positive voltage range of the C-V curve. But here in ideal case as there is no charge is generated in device, such effects are rare to be noticed. In ideal condition the interface trap charge density measured in
25°C is more than the interface trap charge density measured in 100°C, (Table III). The dielectric constant measured from the highest capacitance (Cox) at accumulation region.

Fig.4 (a) Simulated result of Interface Trap Charge Density using Al/SiO2/Si Structure.

Fig.4 (b) Simulated result of Interface Trap Charge Density using Al/Al2O3/Si Structure.

Fig.4 (c) Simulated result of Interface Trap Charge Density using Al/Y2O3/Si Structure.

Fig.4 (d) Simulated result of Interface Trap Charge Density using Al/HfO2/Si Structure.

Fig.4 (e) Simulated result of Interface Trap Charge Density using Al/TiO2/Si Structure.

It is observed from the stretched out of CV curve that Dit increases with increasing temperature from 25°C to 150°C as shown in table-III [fig no.4(a),(b),(c),(d),(e)]. This may be due to the generation of thermally induced defects. It is also reported that the higher temperature produces more defects due to dislocations near the valance and conduction band.

TABLE III: Measured Dit of various dielectrics films at different temperature.

<table>
<thead>
<tr>
<th>Temp (°C)</th>
<th>Al2O3 (Dit x10^11)</th>
<th>Y2O3 (Dit x10^11)</th>
<th>HfO2 (Dit x10^11)</th>
<th>TiO2 (Dit x10^11)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>5.9</td>
<td>4.1</td>
<td>5.1</td>
<td>5.1</td>
</tr>
<tr>
<td>125</td>
<td>6.15</td>
<td>5.2</td>
<td>7.7</td>
<td>7.2</td>
</tr>
<tr>
<td>150</td>
<td>9.05</td>
<td>8.12</td>
<td>9.4</td>
<td>9.1</td>
</tr>
</tbody>
</table>
V. TEMPERATURE DEPENDENT OTHER ELECTRICAL PROPERTIES

As the temperature decreases Device performance improves and as temperature increases, the device performance degrades. As the Temp decreases Vth increases. The threshold voltage increases at low temperature due to the increase in Fermi potential $\phi_f$, depletion charge [16].

### TABLE IV: Measured Vth of various dielectrics at different temperature.

<table>
<thead>
<tr>
<th>Temp $(^\circ C)$</th>
<th>SiO$_2$</th>
<th>Al$_2$O$_3$</th>
<th>Y$_2$O$_3$</th>
<th>HfO$_2$</th>
<th>TiO$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>0.19</td>
<td>0.16</td>
<td>0.16</td>
<td>0.16</td>
<td>0.16</td>
</tr>
<tr>
<td>100</td>
<td>-0.04</td>
<td>-0.04</td>
<td>-0.08</td>
<td>-0.04</td>
<td>-0.03</td>
</tr>
<tr>
<td>125</td>
<td>-0.11</td>
<td>-0.13</td>
<td>-0.16</td>
<td>-0.12</td>
<td>-0.12</td>
</tr>
<tr>
<td>150</td>
<td>-0.19</td>
<td>-0.19</td>
<td>-0.20</td>
<td>-0.20</td>
<td>-0.20</td>
</tr>
</tbody>
</table>

A flat band voltage that is different from zero will cause dielectrics are there whose permittivity is higher than AlN. For e.g. HfO$_2$, Al$_2$O$_3$, ZrO$_2$. So a better result can be obtained from these above dielectrics by considering the discussed parameters. We have already discussed here the behavior of the different electrical parameter at high temperature. Now we can expect a better understanding of the mechanism of this material at the influence of the lower temperature.

### TABLE V: Measured Vfb of various dielectrics at different temperature.

<table>
<thead>
<tr>
<th>Temp $(^\circ C)$</th>
<th>SiO$_2$</th>
<th>Al$_2$O$_3$</th>
<th>Y$_2$O$_3$</th>
<th>HfO$_2$</th>
<th>TiO$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>-0.35</td>
<td>-0.35</td>
<td>-0.35</td>
<td>-0.37</td>
<td>-0.37</td>
</tr>
<tr>
<td>100</td>
<td>-0.43</td>
<td>-0.43</td>
<td>-0.44</td>
<td>-0.43</td>
<td>-0.42</td>
</tr>
<tr>
<td>125</td>
<td>-0.44</td>
<td>-0.44</td>
<td>-0.44</td>
<td>-0.46</td>
<td>-0.45</td>
</tr>
<tr>
<td>150</td>
<td>-0.46</td>
<td>-0.46</td>
<td>-0.48</td>
<td>-0.48</td>
<td>-0.49</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

After modeling the material, the simulated data for Capacitance-Voltage, interface trap charge density, and other electrical parameters with respect to the temperature have been validated with that of the reported ones. And from that were reached at the conclusion that because of the high permittivity, thermal stability of AlN, the discussed parameters are expected to improve considerably at high temperature, than the SiO$_2$. We studied the various parameters taking AlN as a dielectric.

REFERENCE