Improvement In The Power Quality With The Application Of Current Source Multilevel Inverter

Kavyashree. G. V, Dr. V. Venkatesh, Venkateshmurthy. B. S

PG Scholar (Power Electronics) Dr.Ambedkar Institute of Technology, Bangalore†

Professor, Dept. of ECE, Channabasaveshwara Institute of Technology, Gubbi, Tumkur††

Asst. professor EEE Dept. ShirdiSai Engineering College, Anekal, Bangalore - 562106†††

Abstract

A generalized three-phase multilevel current source inverter (CSI) structure is proposed in this paper. The three level CSI topology consists of three-phase six-value converters. The multilevel inverters when compared with the conventional two-level inverters, exhibit higher output voltage for the same device rating, lower harmonic content, and dv/dt and lower electromagnetic interference levels. Also they draw input currents at lower distortion content and they can operate with a lower switching frequency [1]. The operation principle and control strategy of the three-level inverter are analysed in detail. The implementation of carrier phase-shifted SPWM scheme is investigated for digital control of the novel CSI structure. Simulated and experimental results are demonstrated.

Introduction

The fast continuing development of power devices working at high switching frequencies for medium and high power applications such as metal-oxide-semiconductor field-effect transistors (MOSFETS) and insulated gate bipolar transistors (IGBTs) has improved the power convertor performance. In some high switching frequency applications, SiC (Silicon Carbide) based power switching devices because their maximum voltage ratings and switching speeds can be about ten times of the conventional Si based devices. In addition, the ON-state resistance of SiC-MOSFETs will be reduced down to 1/500 of the country available devices and their operating temperature can be over 300^0C, which is considerably effective to improve efficiency and power density of the power converters. Development of high performance semiconductor switches also increases the research interest because they have capability to output higher output power with low voltage rating devices and less distorted output waveforms compared with the conventional two level inverters. The multilevel inverter topologies can generally be classified into voltages source inverters (VSI) and its dual, i.e., current source inverters (CSI). Multilevel voltage source inverters (VSIs) are widely used for medium voltage adjustable speed drives. Recently the technology is seen wide acceptancepower and medium voltages are needed. Typicaland fast advances in industry applications where high topologies of multilevel VSIs include diode clamped inverters, cascaded H-bridge inverters and flying capacitor multilevel

inverters [2]. Large number of voltage levels is required in very high power applications due to high utility supply voltage. For diode clamped multilevel inverter, the large number of voltage levels results in complex control of dc capacitor voltage balancing [2-3]. The cascaded H-bridge multilevel inverter [4] requires a costly phase shifting transformer with many secondary windings. It uses many low voltage components, leading to the increased component count and reduced reliability. The flying capacitor multilevel inverter requires large amount of capacitors and associated pre-charge circuits, which reduces its practicality in industry applications [5]. On the contrary, current source inverters (CSI) generally do not have the above mentioned drawbacks. In addition, it has the advantages such as inherent four quadrant operation and short circuits protection [6]. In this paper, a 3-level current source inverter is proposed. A phase shifted PWM (SPWM) scheme is developed for the multilevel CSI to reduce the total harmonic distortion while maintain the low device switching frequency.

2. Current Source Inverter

It consists of n modules of current source, three phase six valve converters and 2(n-1) inductors. This n module structure can output 2n+1 current level. The chosen unidirectional switch is the gate turn off thyristor (GTO), or an IGBT in series with a diode. The dc sides of every CSI module are paralleled through inductors [6]. These inductors, here after called sharing current inductors, play a role of smoothing dc side currents of every module and divide the dc currents source into different current source into different current ratings. Because of the filter capacitors applied directly across the ac terminals of the 6-valve converter bridge, at most only one valve of upper set of three valves and only one valve of the lower set can conduct at any one time. That is, three valves in upper (or lower) set of one module operate in a complementary way. For a multilevel CSI composed of n modules, in steady state, all sharing current inductors on the upper (or lower) bus are carrying different current ratings, respectively.

3. Switching States

It can be easily concluded that, for the proposed n-module structure, the total number of switching combination is Nc = 32n (2) for a five-level CSI (n=2), there are 81 combinations, for a seven level CSI (n=3), there are 729 combinations, and so on. From the switching combination every odd output order such as 1, 3, 5….11, there is only one switching state [7]. The voltage uL11 across sharing current inductor L11 and the voltage uL12 across L12 are both zero because of the short circuit created by the two switches of the same phase. Hence iL11 and iL12 will stay almost constant during these odd output orders.

4. PULSE WIDTH MODULATION

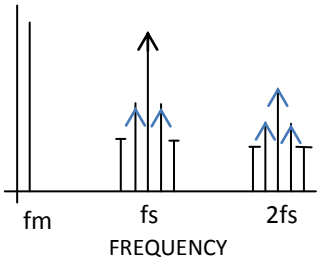

FIGURE 4.1.1 LINEAR MODULATION

PWM is the most popular method for producing a controlled output for inverters. They are quite popular in industrial applications.

4.1LINEAR MODULATION

The simplest method is to vary the ON time proportionally with the modulating signal. Its

advantage is that it is easy to demodulate. The modulating or information signal can be recovered by low pass filtering. A low frequency (Fm) sine wave modulating the width of a fixed frequency (fs) pulse train is shown in the figure 4.1. As can be seen a low pass filter can extract the modulating signal (fm).

4.2 SAW TOOTH PWM

A fixed frequency PWM can be generated by comparing with a linear slope waveform like a saw tooth waveform. As seen in the figure the output goes high when the sine wave amplitude is greater than saw tooth. It can be achieved by comparator with logic HIGH when non-inverting input is greater than the inverting one.

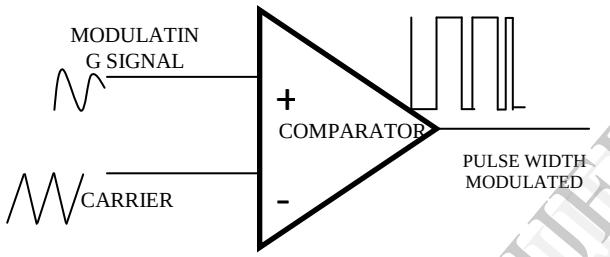

FIGURE 4.2.1 SAW TOOTH PWM

4.3MULTIPLE PULSE WIDTH MODULATION

The harmonic content can be reduced by using several pulses in each half cycle of output voltage. The generation of gating signals for turning ON and OFF transistors by comparing a reference signal with a triangular carrier wave. The frequency Fc, determine the number of pulses per half cycle. The modulation index controls the output voltage. This type of modulation is also known as uniform pulse width modulation (UPWM).

4.4SINUSOIDAL PULSE WIDTH MODULATION

Instead of, maintaining the width of all pulses of same as in case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency Fc. The frequency of reference and its peak amplitude Ar, controls the modulation index M, and rms output voltage V_0. The number of pulses per half cycle depends on carrier frequency [8].

ADVANTAGES FO PWM

The output voltage control is easier with PWM than other schemes and can be achieved without any additional components.

The lower order harmonics are either minimized or eliminated altogether.

The filtering requirements are minimized as lower order harmonics are eliminated and higher order harmonics are filtered easily.

It has very low power consumption.

The entire control circuit can be digitized which reduces the susceptibility of the circuit to interference.

5. Simulation Results

To verify the above proposition, the operation process of the three-level CSI is simulated. During simulation, the dc voltage source is 100V, both of the sharing current inductors are 50mH, output frequency is 50Hz. The average voltages across the inductors in one cycle are nearly zero; the inductors current ripple is tiny and current equilibrium is reached.

The CPS-SPMW is adopted to check out the proposed SPMW scheme when frequency ratio of

the carrier signal to the modulation signal is 21 and the modulation index is 1.

To validate the use of the structure, a laboratory prototype for a three level CSI system has been constructed. In the experimental setup, the chosen active switches are MOSFET in series with a diode; the dc link current source is obtained from a dc voltage source Vdc series with a 100mH smoothing inductor, and the dc voltage source Vdc is gained from an uncontrollable rectifier of three phase ac voltage source.

The carrier frequency is 1050Hz and the modulation index is 1. The three phase modulating reference signals are generated by microcontroller through looking up sinusoidal table, and triangular carriers are produced by the counters embedded in microcontroller.

6. CONCLUSIONS

For higher power applications, as one of typical multilevel converters, multilevel current source inverters can have particular advantages in some circumstances. A novel three phase multilevel CSI topology structure is proposed in this study. The structure has many features such as no any bulky transformers, inductor current balance, and equal current division among switches and modularized configuration. The detailed analysis has been introduced to show these advantages. Aiming at digital control of the multi module CSI, the implementation of tri-logic SPMW scheme for current source inverter is investigated. With the development of superconducting magnetic energy storage technique, the structure with all these characteristics, especially with the digital control, are very desirable in high power applications. The multilevel inverter topology can drastically reduce complexity of the gate drive circuits and the control circuit in the multilevel CSI. This remarkable feature never fades away even if the number of the power switches is increased to achieve higher level number of the output current waveform. Chopper circuits working as DC current sources are also discussed which are able to reduce the input inductor size down to micro-h order.

7. REFERENCES

[1] Lai JihshengPengFangzheng, “Multilevel converters a new bleed of power converters,” IEEE Trans. on Industrial Application, vol.32, no.3, pp.509-517, 1996.

[2] S.M.R.Sadriyen, M.R.Zolghadri and J.Mahdavi, “Application of a current source inverter for a linear piezoelectric step motor drive,” power electronics and drive systems, IEEE PEDS Indonesia, 22-25 oct. 2001, vol.2, pp.892-897.

[3] V.DelliColli, P.Cancelliere, F.Marignetti and R.DiStefano,”Influence of voltage and current source inverters on low-power induction motors,” Electric Power Application, IEEE proceedings 2005, vol.152, no.5, pp. 1311-1320.

[4] D.Xu, B.Wu, “Multilevel current source inverters with phase shifted trapezoidal PWM,” Power Electronics specialists conference, PESC 2005, Brazil, 11-14 sept., pp.2540-2546.