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Improved Sample and Hold Circuit using MOSFET

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***Abstract* - The focus of this paper is the design of low distortion sample and hold circuit. The main idea behind avoiding distortion is to make gate-to-source voltage of the MOSFET independent of input voltage. The preferred circuit of the present paper is capable of performing at high speed since it does not need an operational amplifier in its operation [9]. This feature also reduces power consumption. Another advantage is that in some aspects transistor device S1 is in closed matched to the switching device, which helps in minimizing distortion. Also the circuit does not have any problem with drain induced barrier lowering (DIBL). Sample and hold circuits find use in linear systems. In some types of analog-to-digital converters, the input voltage is compared to a voltage produced internally from a digital-to-analog converter (DAC). The circuit takes a series of values, and conversion stops once the voltages are equal, within a defined error margin. If the value of the input were allowed to change during this comparison, the outcome of the conversion would be skewed and might be completely unrelated to the actual input value [2].**

***Index Terms*- Sample and Hold, DAC**

I. INTRODUCTION

A sample and hold circuit is an analog device that samples the voltage of a continuously varying analog signal and holds its value at a constant level for a specified period of time. These circuits and related peak detectors are the fundamental analog memory devices. They are typically used in analog-to-digital converters to eliminate variations in input signal that can disturb the conversion process.

II. BACKGROUND

Figure 1 below shows the block diagram of a basic sample and hold circuit. This circuit consists of a switch S0 coupled in series with a capacitor C_{out}. In operation, the switch S0 is closed at the sampling rate and the voltage across capacitor C_{out} represents input voltage V_{in} [9].

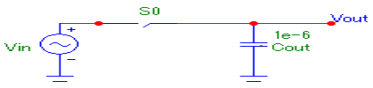

Fig. 1 Basic Sample and Hold Circuit

Figure 2 below shows the schematic of the basic NMOS sample and hold circuit. In this circuit, switch S0 in figure 1 is replaced by an NMOS transistor. We have used Micro-Cap 11.0.0.2 for simulation of results. The NMOS MOSFET used are of W=20µm, L=2µm, V_T =1.33Volts. Figure 3 shows a timing diagram for the pulse f1 that applies to the gate of transistor S0 [9].

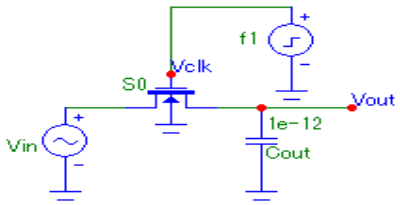

Fig 2. Basic Sample and Hold circuit using NMOS

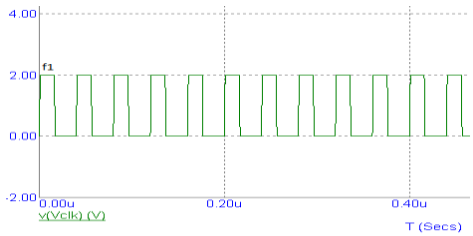

Fig. 3 Timing diagram for f1

When the clock f1 at the gate of S0 goes high (V_{DD}), the switch S0 is switched on and capacitor C_{out} is shorted to the input. In this case NMOS is in sampling mode. For S0 to work in tracking mode it should work in triode mode and for that $V_{GS} > V_T$ and $V_{DS} < (V_{GS} - V_T)$. Gate-to-source voltage is given by

$$V_{GS} = V_G - V_s \quad \text{Eq. 1}$$

$$V_{GS} = V_{DD} - V_{in} \quad \text{Eq. 2}$$

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)} \quad \text{Eq. 3}$$

From equations 2 and 3, on resistance of the NMOS S0 is dependent on the input voltage V_{in} and this resistance results in distortion of the hold voltage of capacitor during hold mode of operation. The power spectral density of noise

associated with this on-resistance of switch capacitor is given by

$$S_{R_{ON}} = 4KT\,R_{ON} \quad \text{Eq. 4}$$

And mean square value of noise voltage across capacitor is given by

$$V^2{}_n = \frac{KT}{C} \quad \text{Eq. 5}$$

From equations 2 and 3 we can say that if we apply V_{DD} at the gate of transistor then V_{GS} will depend on $V_{in.}$ In order to remove the effect of clock, voltage should be equal to $(V_{DD} + V_{in})$. This will make V_{GS} independent of $V_{in.}$

When the input becomes low (zero), the switch goes into off mode. This results in the input voltage value being held on the hold capacitor. Thus in this case NMOS is in the hold mode.

We have used NMOS for the design of sample and hold circuit instead of PMOS because

- Electrons, which are carriers in an n-channel device, are about two times as mobile as holes, the carriers in a p-channel device. An n-channel device is therefore faster than a p-channel device.
- Since electron mobility is almost twice that of a hole, the on-resistance or impedance of an n-channel device will be half that of an equivalent PMOS device operating under same conditions with the same. Thus n-channel transistors that are only half the size of p-channel devices will have the same impedance. Therefore, complex n-channel ICs can be implemented without any increase in area of silicon.
- N-channel circuits have a speed advantage over PMOS as the junction areas are smaller [6][1]. Considering the fact that the speed of the operation of an MOS IC is significantly reduced by internal RC time constants, and also the capacitance of the diode is proportional to diode size, an n-channel junction might have smaller capacitance. This, in turn, enhances its speed [3].

While the circuit in figure 2 has the advantage of being simple in construction, it also has a few disadvantages. When switch S0 is turned off, some of the channel charge of the NMOS transistor gets heaped on to the hold capacitor. As this charge depends on the signal and is nonlinear, this will cause distortion in the output voltage of the hold capacitor C_{out}. Plus, the exact sampling instant is dependent on the gate-source voltage V_{gs} of the switch S0 and transistor threshold voltage V_t.

In order to remove the effect of input voltage on $V_{GS,}$ bootstrapping is used which will ensure a constant gate source drive of the switch.

Figure 4 below shows a bootstrapped sample and hold circuit consisting of a sample switch S0, comprising an NMOS transistor, and hold capacitor C_{out}. In this case, however, the gate of the transistor is coupled to a bootstrap circuit which includes the bootstrap capacitor C_{bias} and switches S2 to S5. Figure 5 below shows the timing diagram of the waveforms f1 and f 2.

In the first phase, f1 is high and the bootstrap capacitor C_{bias} is charged to bias voltage $V_{bias.}$ During the second phase, when f2 is high, the bootstrap capacitor C_{bias} is put across the source and gate terminals of the switch S0. Now V_{GS} is given by

$$V_{GS} = V_G - V_S = (V_{bias} + V_{in}) - V_{in} = V_{bias} = V_{DD} \quad \text{Eq. 6}$$

This will make sure that the V_{GS} of the MOSFET is held constant at V_{bias} irrespective of the input voltage V_{in} [9].

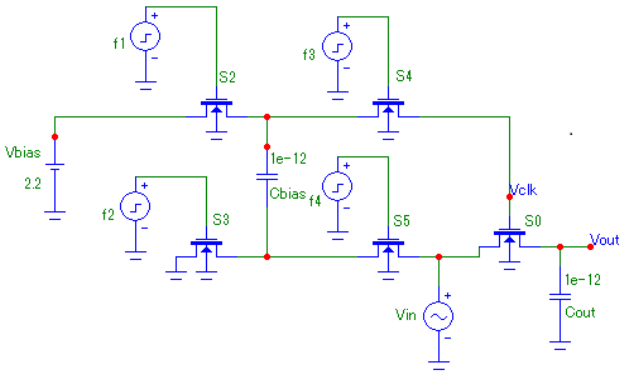

Fig. 4 Bootstrapped Sample and Hold Circuit

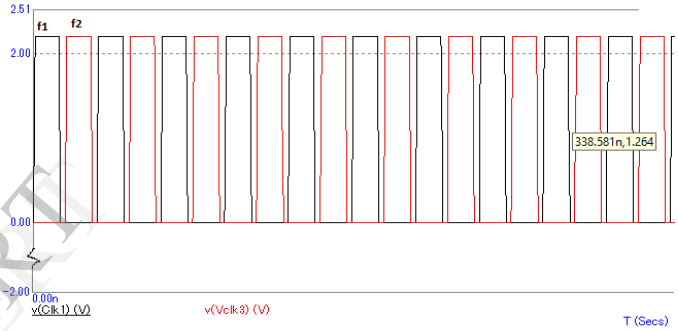

Fig. 5 Timing diagram for f1 and f2

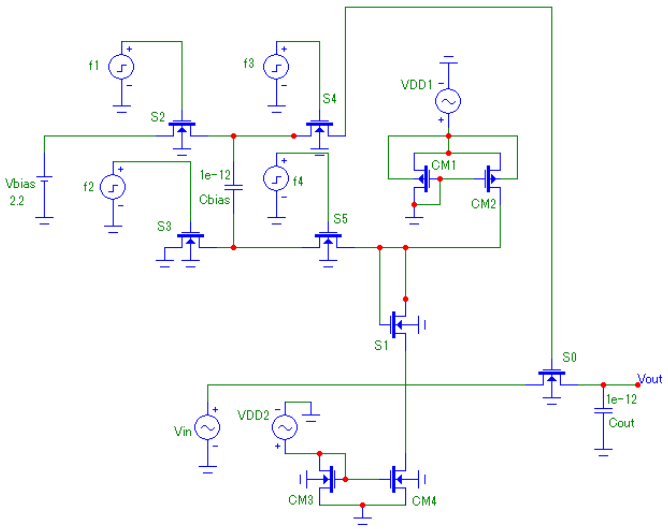

Fig. 6 Proposed Sample and Hold Circuit

Although this circuit gives a good performance, it cannot be implemented using an n-well technology. Resistance of S is depend on channel charge which in turn depends on the input voltage V_{in} through the threshold V_t.

III. PROBLEM DEFINITION

The objective is to keep the gate source (gate-to-source voltage) drive of the S/H switch at a constant value, irrespective of input voltage V_{in} through the threshold V_t so that there is no effect of input voltage on the switching transistor and hence no distortion during sampling.

IV. PROPOSED CIRCUIT

Figure 6 shows a sampling transistor S0 and hold capacitor C_{out} is an NMOS transistor. The transistor S1 is a diode connected NMOS transistor. In this circuit, an NMOS transistor with its drain is coupled to its gate. The conductivity type of the transistor S1 is preferred to be the same as that of transistor S0. Currents through transistor S1are made to flow in and out by the current source formed by CM1 and CM2, and the one formed by CM3 and CM4. These current sources can be implemented by current mirror.

During the first phase of the operation, switch signal f 1 is high and causes switches S2 and S3 to be conductive. At that same time, switch signal f 2 is low causing switches S4 and S5 to be open. If different types of switches are used for the switches, the switch signals f1 and/or f2 can be modified accordingly. As per figure 6, during this first phase, bootstrap capacitor C_{bias} has a potential of V_{bias} across it [9].

In the second phase, when f1 is low and f2 is high, bootstrap capacitor C_{bias} is put in series with transistor S1 and coupled to the gate of transistor S0. Accordingly, the voltage Vg at the gate of the transistor S can be computed as

$$V_g = V_{in} + V_{t-s1} * V_{in} + V_a + V_{bias} \quad \text{Eq. 7}$$

The resistance of the NMOS S0 is proportional to $V_{gs} - V_{t-s0} * V_{in}$. In these equations, V_{t-s1} is the threshold voltage for the transistor S1 and V_{t-s0} is the threshold voltage for the transistor S0. Since transistor S1 is prototype of the transistor S0, these threshold voltages are nearly equal.

Of course, $V_{gs}$is the difference between V_g, which is given above, and V_s, which is coupled to V_{in}. Accordingly,

$$V_{gs} = V_{t-s1} * V_{in} + V_a + V_{bias} \quad \text{Eq. 8}$$

$$V_{gs} - V_{t-s0} * V_{in} = V_{t-s1} * V_{in} - V_{t-s0} * V_{in} + V_a + V_{bias} \quad \text{Eq. 9}$$

Therefore when the threshold voltage of the transistor S1 is equal to the threshold voltage of the transistor S0, V_{gs} is at a constant value $V_{gs}(V_a + V_{bias})$. During the sample phase f 2 of the operation, the channel charge is

$$Q_{ch} = C_{ox} * V_a \quad \text{Eq. 10}$$

Which is also a constant as Va and C_{ox} are constants.

The current source (formed by CM1 and CM2) is implemented using PMOS as a current source. PMOS current source provides current from positive supply [5].

The current source (formed by CM3 and CM4) is implemented using NMOS as a current sink. NMOS current source sinks current to ground [5].

The circuit in figure 6 has a number of benefits. The channel charge and resistance are not dependent on the input voltage V_{in}, implying that distortion can be minimized. Furthermore, the body effect is adjusted for, certainly to the first order at least. Further drain-source voltage of the switching device S0 remains constant, which reduces non-idealities caused by drain induced barrier lowering (DIBL) and finite output conductance of the MOSFET. Since there is no operational amplifier, it results in a fast and low power circuit.

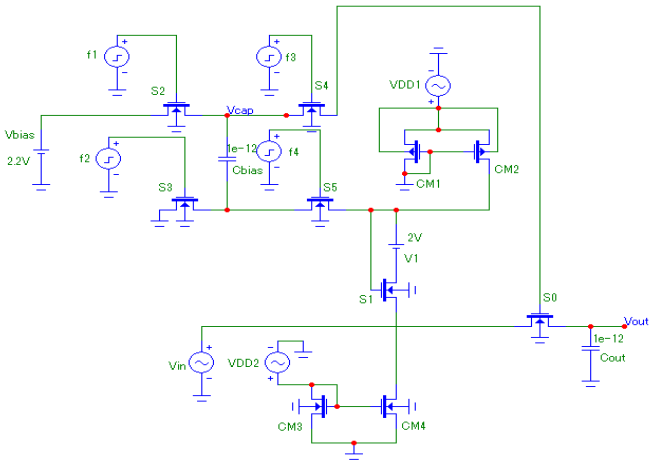

Fig. 7 Modified proposed sample and hold circuit

A potential issue with the circuit in figure 6 is that transistor S1 operates in the inversion region while switch S0 operates in the triode region. This difference might mean that their threshold voltages are different, which could impact the accuracy of the circuit [9].

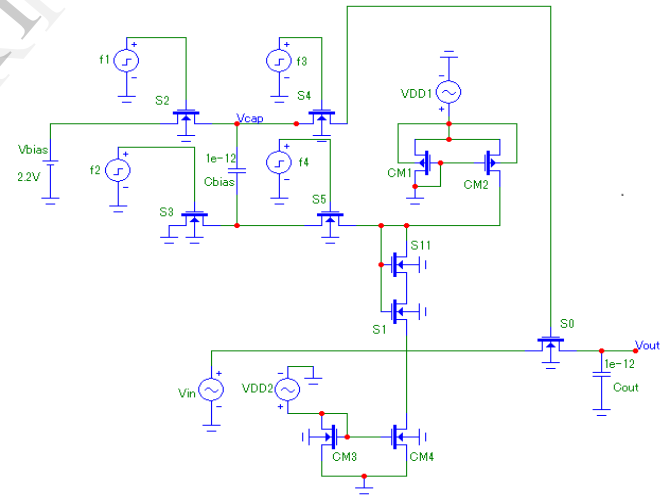

Fig 8 Modified proposed sample and hold circuit - Voltage source implementation

Figure 7 above shows the solution to above problem. Here, a voltage source V is inserted in the drain circuit of the transistor S1 as shown below.

The voltage source V1 supplies an additional voltage designed to push transistor S1 into triode mode operation, which would make it a better prototype of the switch device S0. Hence, better performance can be expected. Threshold voltage for transistor S1 is provided by voltage source V1.

There are number of ways to implement voltage source V1. One example of implementation of the voltage source V1 is shown in figure 8. In figure 8, a diode S11 is coupled between the drain and gate of the transistor S1. Upon the

inclusion of this diode, transistor S1 begins operating in the triode region [9].

V. Experimental Result

Waveforms showing relationship between input and output of the above circuits are shown below. It can be seen from the waveforms that as we make improvements in the circuits for keeping V_{GS} independent of $V_{in,}$ difference in the voltage at which sampling occurs and the voltage during hold period decreases and sampling occurs smoothly, i.e. circuit characteristics improves. Table 1 shows this voltage difference.

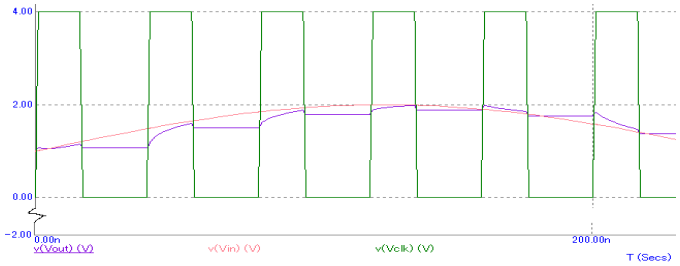

Fig. 9 Basic circuit input output relationship

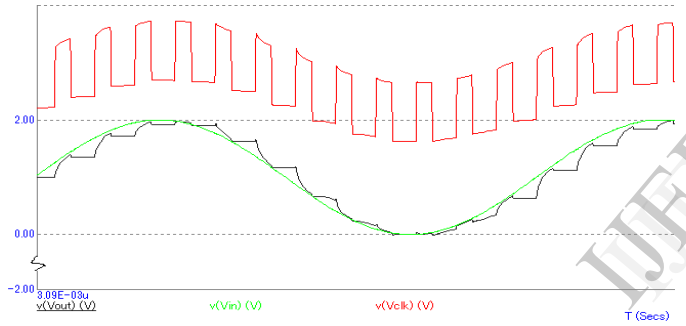

Fig. 10 Bootstrap circuit input output relationship

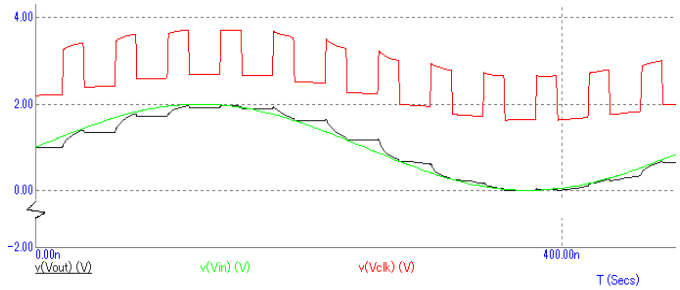

Fig. 11 Proposed circuit input output relationship

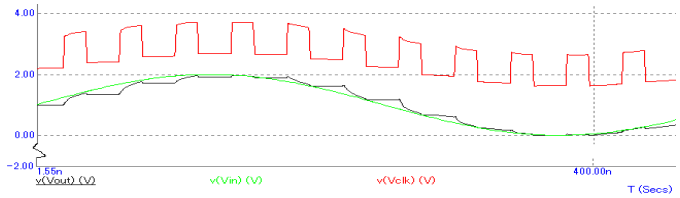

Fig. 12 Modified Proposed circuit input output relationship

Table 1 Circuits Comparison

Sr No	Circuit	Distortion (Volts)	Reason For Distortion
1	Basic Circuit	0.22	1. MOS switch charge injection 2. Sampling moment distortion 3. Clock Feedthrough 4. ON resistance of the NMOS
2	Bootstrap Circuit	0.044	1. Duty cycle and ON time is limited by requirement to refresh the charge in bootstrap capacitor 2. Channel charge and switch S0 resistance depends on input through threshold
3	Proposed Circuit	0.038	Transistor S1 operates in inversion while switch S0 operates in triode region. This difference might mean that their threshold voltages are different, which could impact the accuracy of the circuit.
4	Modified Proposed Circuit	0.032	Very low distortion.

VI. CONCLUSION

The implementation suggested in this paper can perform much smoother sample and hold operation. Power consumption is minimized as operational amplifier is not used. Another benefit is that the device S1 is closed matched to the switching device, which again minimizes distortion. Additionally, this circuit does not have a problem with drain induced barrier lowering (DIBL).

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