International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 07, July - 2017

Improved De-blocking Filter for Baseline Profile H.264 /AVC

Yogesh G S
Visvesvaraya Technological University
Belagavi,India

S. G. Hiremath
Department of ECE,
East west Institute of Technology,
Bengaluru, India

***Abstract*— This paper proposes an innovative deblocking filter for H.264 decoder. Base line profile of H.264 is taken into consideration. Improved deblocking filter uses a modified filtering order for vertical and horizontal processing. The proposed order of filtering reduces the LUT and slice registers of fpga architecture. It also reduces the power consumption .peak signal to noise ratio and structure similarity index matrix it taken has for the measurement of quality for picture frames, the coding is done in verilog hdl. Quarter common intermediate format i.e. 176*144 resolution picture frames are used for the processing.Virtex6 series of Xilinx FPGA is the target device. The simulation results show that look up tables, power consumption and slice registers are reduced which results in improved deblocking filter design. Same deblocking filter can be used in encoder also.**

Keywords*— *De-blocking filter, HDL, FPGA, slice Look-up-tables and slice registers.

I. INTRODUCTION

The present digital world uses plenty of multimedia contents for communication. It requires huge amount of memory and high bit rates .so compression of data becomes the very much necessory.H.264 [1] compression standard satisfies this compression needs. It is also named has advanced video codec(AVC),H.264 is an ITU standard for encoding and decoding video with target coding efficiency twice that of its previous version H.263[2].AVC is the result of joint effort by ITU-T and ISO/IEC. The computational requirement of encoding and decoding H.264 video vary depending on video resolution, frame rate and level of compression used. At low end mobile phone applications favor videos encoded in the QCIF resolution. At the higher end High Definition video (1920*1080) videos. Transforms based compression and variation in the quantization levels leads to blocking artifacts.AVC uses transforms, quantization and their inverse with prediction in encoding and decoding process. This results in blocking artifacts. A video frame is partitioned into blocks and transforms are applied on this .Integer transform is used in AVC. Increase in quantization parameter to more values for better compression also leads to more artifacts. These artifacts have more annoying effect at low bit rates. Deblocking filter is used to overcome this problem of blocking artifacts in H.264. Visual quality of decoded video is improved by deblocking filter.

In this paper we propose a hardware implementation of a deblocking filter with a novel filter processing order. Many works have been carried out on deblocking filters. Sebastian Lopez *et al*. [3] propose a deblocking architecture with less hardware cost and also a better latency. A deblocking algorithm is introduced in paper [4] to remove artifacts. A hardware architecture using field programmable gate array (FPGA) is designed. Improved hardware blocks are used to decrease the power consumption of overall deblocking filter. Reduction in the power consumption is achieved using a novel approach called clock gating. The results shows that 30% power reduction using clock gating approach at the hardware cost of 2.3 % and clock speed of 5.8% was achieved by this method. A new approach for processing order is presented by [5]. Still there is a need for efficient hardware implementation of deblocking filter. Very few works have been done using less resources of field programmable gate array.

The rest of the paper is presented in deferent sections. Second section gives over view of existing processing order of deblocking filter. Next section gives proposed novel processing order for filtering. Section four explains simulation results. Finally section five presents conclusion.

II FUNDAMENTALS OF DEBLOCKING FILTER

The block based coding results in the visual artifacts due to this reason H.264 uses a deblocking filtering process. The filtering is applied to every macro block decoded to decrease the blocking noise. Filtering helps in improving the quality of decoded frames and also better compression. The filtering operation depends on the values of certain parameters has defined by the standard. The detailed deblocking filtering can be studied from [6].

H.264 uses integer transform on a 4x4 block of samples of the frame. The deblocking filter is also applied on 4x4 block except the boundary of the picture. The ordering sequence of the filtering is first luma samples and then chroma samples. The vertical edges are filtered first and then horizontal edges are taken into consideration. The concept of vertical and horizontal edges or boundary is shown in Figure.1 it shows the four pixels on either side of the horizontal boundary and vertical boundary in the adjacent blocks a and b. a block samples are a0, a1, a2, a3 and b block samples are b0, b1, b2, b3.the filtering operation depends on the boundary strength variable BS. If boundary strength is zero no filtering operation is performed .if its value is greater than zero and with certain conditions satisfied according to H.264 standard [7] then the filtering operation is performed. The concept of Switching off the filter operation is needed when there is a drastically changes across the boundaries of the block in the original frame. Figure.2 describes the principle of deblocking filter which is very fundamental with the help of one dimensional edge representation. Which pixels will be

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 07, July - 2017

considered for filtering among a0 and b0 as well a1 and b1 will be decided using the thresholds and

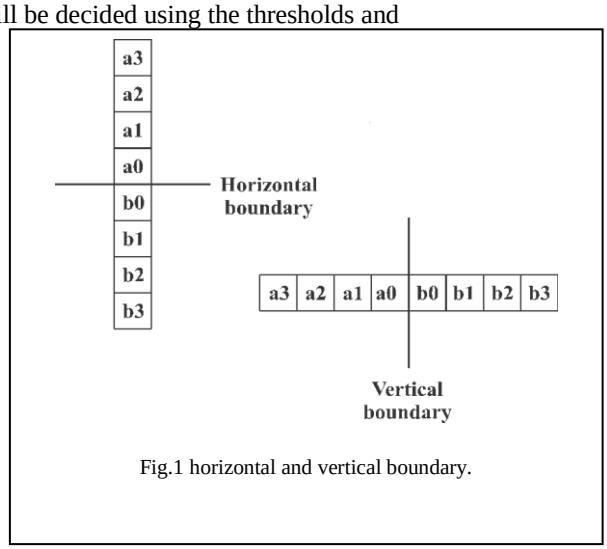

Fig.1 horizontal and vertical boundary.

Quantization parameter defined by the standard. Normally up to three samples on either side of the edge are used for filtering which is represented has a0, a1, a2 on one side and b0, b1, b2 on the other side which is shown in Figure.2.

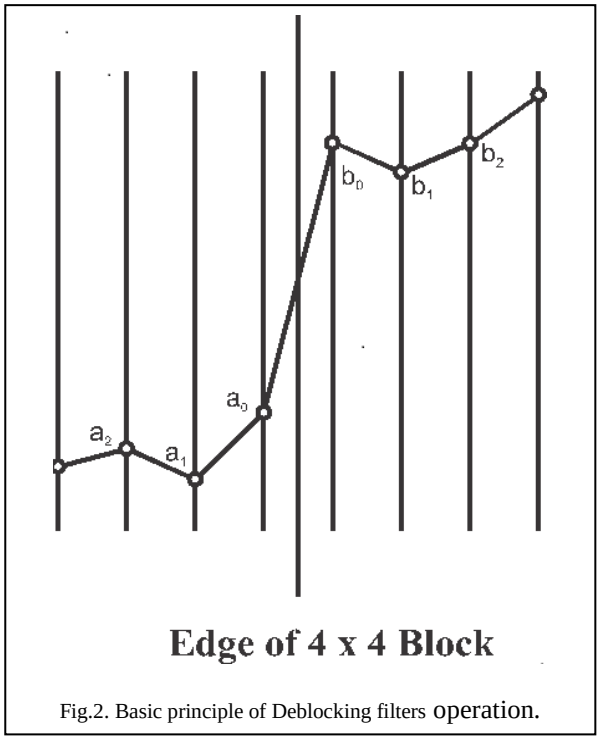

Fig.2. Basic principle of Deblocking filters operation.

III. DEBLOCKING FILTER EXISTING FILTER ORDER

Here we present the existing order of filtering .the standard h.264 has defined the filtering order to be followed. The vertical boundary values of the luminance and chrominance blocks are filtered first. Then horizontal boundry values of the luminance and chrominance components are filtered. Since vertical filtering results are used in the horizontal filtering process, the results of intermediate have to be stored. This processing results in more memory requirement. It becomes expensive in terms of resources of hardware implementation using FPGA. This also results in improper horizontal filtering.

IV PROPOSED FILTERING ORDER OF DEBLOCKING FILTER

The standard deblocking filtering order of vertical and horizontal has been modified and developed in this paper. Reordered processing order is clearly shown in Fig.3.according to this order vertical filtering is performed initially and horizontal filtering is performed later. Luma component is represented has Y, 1 and 2 are vertical edges and 3 is horizontal edge. When 3rd horizontal edge is being filtered, third vertical edge will be considered for filtering. When chroma components comes into consideration we use pipelining concept their by allowing chroma component pixels to perform vertical filtering in the presence of luma pixels still under processing. The number of clock cycles needed for filtering is reduced here. The same order is extended for the rest of the pixel edges. Using above method of ordering memory required for processing blocks are reduced. It results in reduction of FPGA resources.

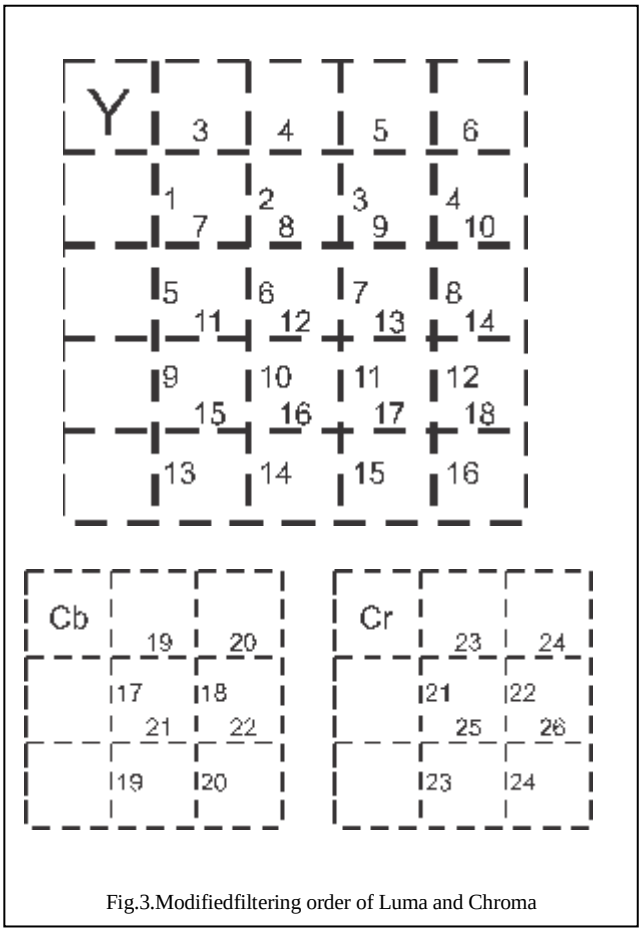

Fig.3.Modifiedfiltering order of Luma and Chroma

This is very necessary for the processing of high resolution Real time videos.

V. EXPERIMENTAL RESULTS

The deblocking filter was implemented using verilog hardware description language. The target device was Xilinx vertex 6.The General processor used is Intel Pentium dual core. Initially existing standard order filtering was taken has reference and verilog coding was developed result of this is

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 07, July - 2017

existing resource values which is referred has Existing. Later verilog coding was performed for reordered filtering which is treated has proposed. Table I depict the two values existing and proposed.

TABLE I

	Existing	Proposed
Slice LUTs	2147	2112
Slice registers	488	462

A foreman video frame of QCIF (176x144) resolution was processed The simulation results shows that reduction in the size of the slice LUTs is 35 with reference to standard existing filtering order. This leads to a very improved architecture of deblocking filter in terms of usage of look up table .since LUTs are reduced it results in reduction of ram memory. It is also observed that the proposed ordering gives a reduction of 26 numbers of slice registers when compared to existing filtering order implementation. Even other parameters were analyzed which has not been presented here. The table I clearly represents the number of LUTs and Slice registers required to design the existing and proposed filtering orders. Figure.4 shows the quantitative representation of two resources for the existing and proposed deblocking filter.ESL represents existing slice LUT and PSL corresponds to propose slice LUT.ESR represents existing slice registers and PSR represents proposed slice registers.

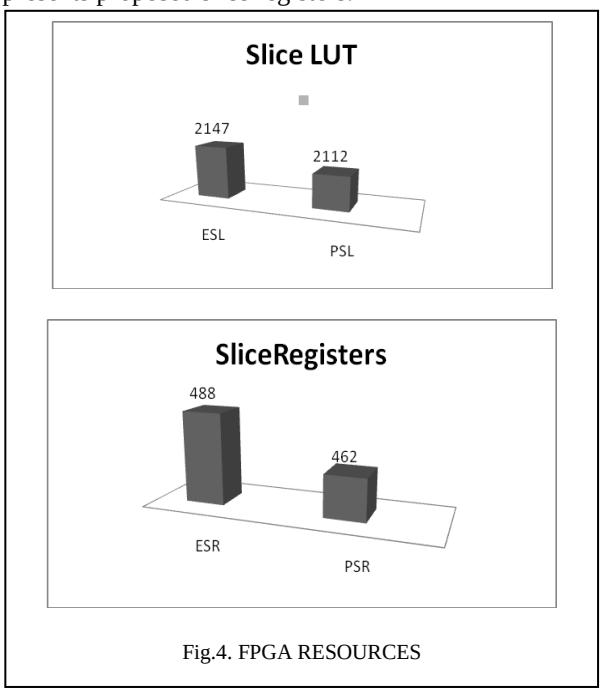

Fig.4. FPGA RESOURCES

A test bench was written in verilog for the reordered deblocking filter and tested in Model-Sim simulator. The resultant wave's forms are showed in the Figure.5.

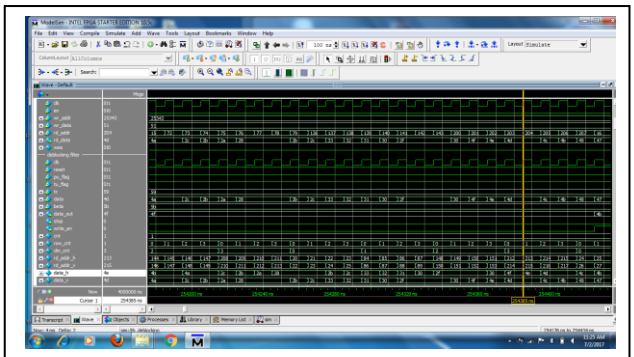

Fig.5. Simulation results

The device utilization summery is obtained by running the proposed deblocking filter verilog code in Xilinx ISE 14.4 platform which is targeted for Virtex -6 XC6VLX130T device. The results obtained after execution is shown in Figure.6.

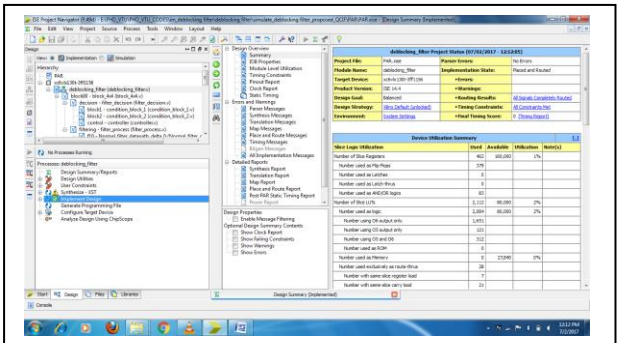

Fig.6.Utalization Summery Report

VI. CONCLUSION

In the present work a FPGA implementation of deblocking filter for H.264/AVC was developed. Initially we explained the basic concepts of deblocking filter algorithm. then an rearranged filtering order of vertical and horizontal filtering was proposed which resulted in improved deblocking filter of H.264.the simulation results depicts that the new processing order reduces the FPGA Vertex 6 resources such has slice registers and look up tables. Finally our implemented deblocking architecture is very novel design for the latest H.264 encoder and decoder.

REFERENCES

[1] Thomas Wiegand,Gary J. Sullivan, Gisle Bjontegaard, and Ajay Luthra,Senior Member, IEEE "Overview of the H.264/AVC Video Coding Standard", IEEE Transactionson Circuits and Systems for Video Technology,vol 13, No 7,july 2003

[2] "Video coding for low bit rate communication" Draft ITU-T Recommendation H.263, Dec 5,1995.

[3] Sebastian lopedz, Felix Tobajas,Gustavo M.Callico,Perez, Valentin de Armas, *et al* " A Novel high performance architecture for H.264/AVC Deblocking Filter" ETRI Journal .2007.Jun,29(3),pp 396-398

[4] C.Karthikeyan and Dr. Rangachar "Implementation of deblocking Filter algorithm using Reconfigurable architecture", International Journal of Application or Innovation in Engineering & Management, Volume 2,Issue 12,2013

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 07, July - 2017

[5] Correa, Guilherme, Luciano Agostini, and Luis A. Cruz. "Sample-Level Filtering Order for High-Throughput and Memory-Aware H. 264 Deblocking Filter." ISRN Signal Processing 2012 (2012).

[6] ITU-T Recommendation H.264(06/2011). Advanced Video Coding for Generic audio visual services.

[7] Richardson I. E. G. "H.264 and MEG-4 Video Compression (Video coding for next Generation Multimedia)", John Wiley.

[8] Shriram K Vasudevan, Subashri V, Sasikumar P, " H.264 decoder designusingverilog(withsimulationresults)",International Journal of computer Applications,Vol.1No.4,pp.92-97.2010

[9] Jignesh Patel, Haresh Suthar, Jagrut Gadit, " VHDL Implementation of H.264 Video Coding Standard", International Journal of Reconfigurable and Embedded Systems (IJRES), Volume 1, 2012.