Improved 10-Bit 30-Ms/s SAR ADC using Switchback Switching Method

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***Abstract*— This brief presents an Improved 10-bit 30-MS/s Successive approximation register analog to digital converter (ADC) that uses a power efficient switchback switching method. Compared with the monotonic switching method and Vcm Based methods, the common mode voltage variation (Vcm) reduces which improves the dynamic offset and the parasitic capacitances variation of the comparator. The comparator consists of pre-amplifier and a dynamic latched comparator. The pre-amplifier is adopted to block kickback noise and enhance the comparison speed. The proposed ADC uses an asynchronous circuit to internally generate the signals. The switchback switching procedure does not consume any power at the first digital to analog converter switching conversion, which can reduce the power consumption. This method does not require fast settling reference buffer to charge MSB capacitor in the conversion phase as it provides longer settling time. The proposed switching procedure consumes only $127.5CV^2_{ref}$. The prototype is fabricated in a 90nm CMOS technology. At 1V supply and 30MS/s, the proposed ADC consumes 0.98mW.**

Keywords*— *Analog to Digital Converter (ADC), energy efficient switching method, low input capacitance, successive-approximation-register (SAR) ADC

I. INTRODUCTION

Successive approximation register (SAR) analog-to-digital
Converters (ADCs) require several comparison cycles to complete one conversion, and therefore have limited operational speed. SAR architectures are extensively used in low-power and low-speed (below several MS/s) applications. As the feature size of CMOS devices is scaled down, the propagation delay of logic circuit reduces. SAR ADCs have achieved several tens of sampling rates with 5 to 10-bit resolution.

Several power efficient techniques have been proposed for the capacitive digital-to-analog in the past. If we compare the conventional switching technique, the energy saving [1], monotonic [2], and Vcm based [3] switching techniques reduce 69%, 81%, and 90% switching energy, respectively. The Vcm based reduces most of the switching energy but requires more switches and reference voltages which increases

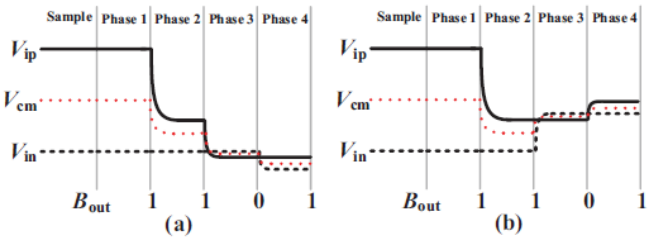

Fig. 1. (a) Waveform of monotonic switching procedure. (b) Waveform switchback switching procedure.

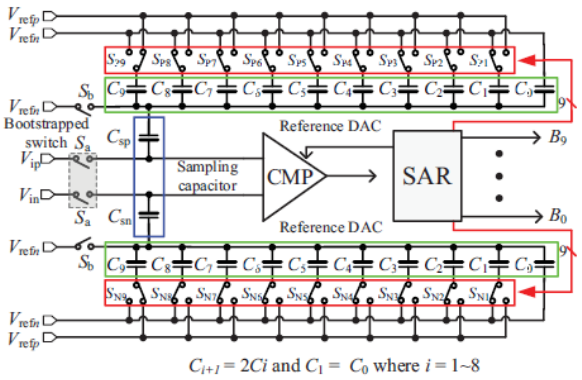

Fig. 2 Block Diagram of the proposed SAR ADC

complexity of the digital circuits. The monotonic switching technique has less switches and reference voltage but during conversion phase common mode voltage varies from Vcm to Vref which induces dynamic offset and the parasitic capacitance variation.

This brief proposes a SAR ADC which uses less switches and reference voltages and reduces 50% of common mode voltage variation. It does not consume energy at first switching hence reduces power consumption.

II. ARCHITECTURE AND DESIGN OF PROPOSED SAR ADC

A. *SAR ADC Architecture*

Fig 2 shows the block diagram of the proposed SAR ADC.

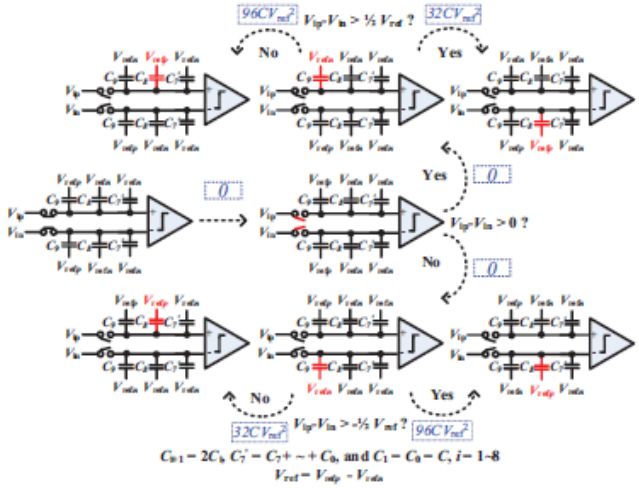

Fig. 3. Switchback switching procedure of 10-bit SAR ADC.

Its core consists of two sampling capacitors, two capacitive reference DACs, dynamic-latched comparator and SAR control logic. The capacitive DAC is split into two parts: a reference DAC and a sampling capacitor. The analog signal is captured by sampling capacitor and reference signal is provided by the reference DAC.

The switches Sa and Sb are turned during sampling phase and the signal is sampled onto sampling capacitors. The bottom plate MSB are connected to Vrefp and all LSBs are connected to Vrefn and reference DAC is at reset state. Next, the switches are turned off and the ADC begins the first conversion. The comparator compares whether Vip is higher than Vin if it is then MSB is set to 1 and if it is not then MSB is set to 0.

The switchback switching method switches only one capacitor in each bit cycle, which reduces power dissipation. The common mode voltage of the switchback switching method would be downward for the first switching and then upward for the remaining cycles. The common mode voltage is reduced to ¼ Vref and approaches to Vcm.

In fig. 3, first three switching phases is shown. According to switchback switching method, the bottom plate of MSB is connected to Vrefp and the rest are connected to Vrefn at the sampling phase. As soon as the sampling switches are turned off, the comparator directly performs first comparison without switching any capacitor and hence energy consumption is saved. The MSB is precharged in switchback procedure in sampling phase and allows longer settling time.

B. *Equations*

For switchback switching method, the average switching energy is given by

$$E_{avg,\,switch} = \sum_{i=1}^{n-2} (2^{n-3-i})\, CV^2_{ref}$$

For monotonic [2] and Vcm [3] based techniques, the average switching energy can be expressed by the following equations. For 10-bit, the monotonic technique consumes $255.5CV^2_{ref}$ and the Vcm based consumes $170.2CV^2_{ref}$.

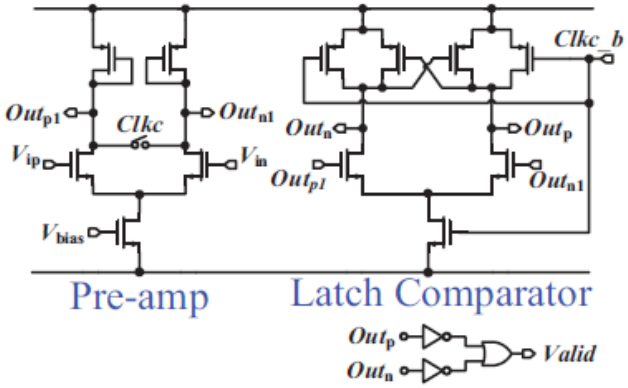

Fig. 4 Dynamic Comparator with Pre-amplifier

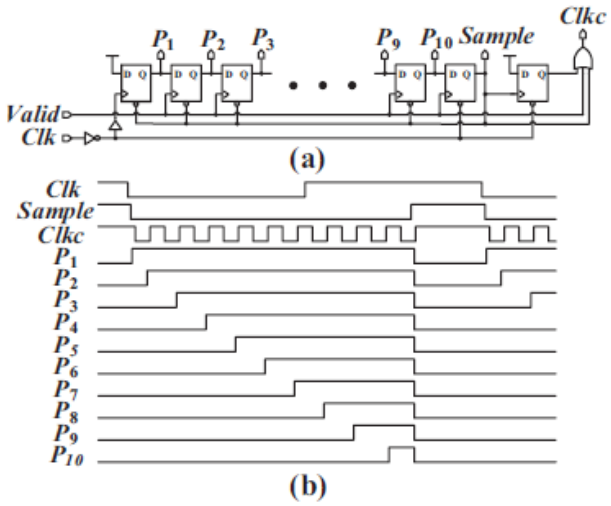

Fig. 5 SAR Logic (a) Schematic (b) Timing Diagram

$$E_{\text{avg,mono}} = \sum_{i=1}^{n-1} \left(2^{n-2-i}\right) CV^2_{\text{ref}}$$

$$E_{\text{avg,Vcm}} = \sum_{i=1}^{n-1} \left(2^{n-2-2i}\right)\left(2^{i}-1\right) CV^2_{\text{ref}}$$

For 10 bit, the switchback switching method consumes $127.5\ CV^2_{ref}$. This technique requires almost 50% less energy than monotonic and 25% less than Vcm based techniques.

III. DESIGN OF BUILDING BLOCKS

A. S/H Circuit

The proposed SAR ADC uses sampling capacitors to sample input signal C_{sp} and C_{sn}, via the bootstrapped

switches, S_a and S_b [9]. During conversion phase, Sa and Sb are turned off hence parasitic capacitance in drain terminal is less than 0.01fF. The Vdac are the voltages of comparator output and reference voltages and is given by

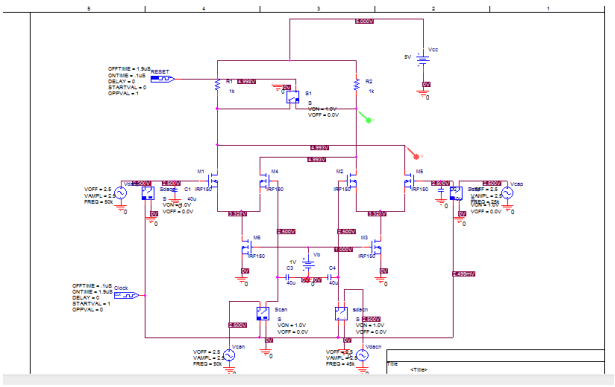

Fig. 6 Schematic of Preamplifier

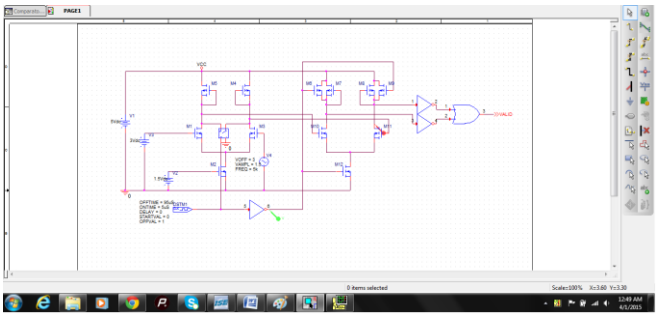

Fig. 8 Schematic of Comparator

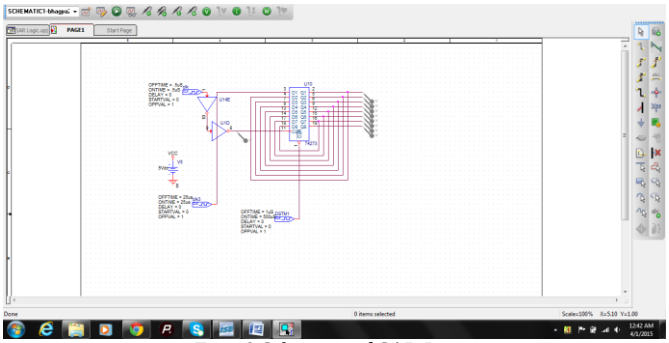

Fig. 10 Schematic of SAR Logic

$$V_{\mathrm{DAC}} = \frac{\sum_{i=1}^{9} Di \cdot 2^{i-1} \cdot C}{\sum_{i=1}^{9} 2^{i-1} \cdot C + \frac{C_{sp} \cdot C_{p1}}{C_{sp} + C_{p1}}} V_{\mathrm{ref}}.$$

B. Dynamic Comparator

In Fig. 4, schematic of comparator is shown which consists of a pre-amplifier and a dynamic latched comparator. The proposed architecture uses preamplifier to block kickback noise which is generated by floating sampling capacitors and latched comparator due low capacitance and this increases speed.

C. SAR Logic

The proposed ADC uses an asynchronous control circuit to internally generate the necessary clock signals [5] to avoid a high-frequency clock generator and a pulse-width modulator. asynchronous phase generator.

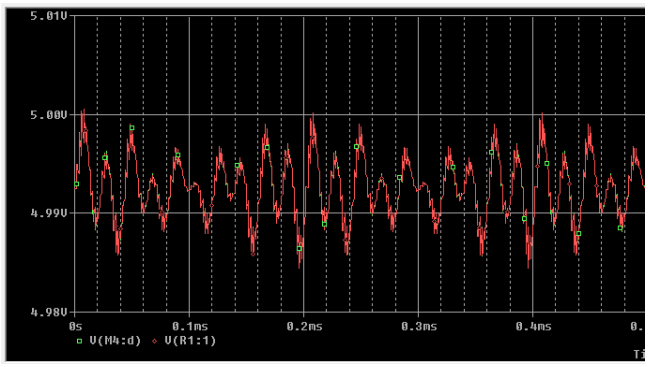

Fig. 7 Simulation result of Preamplifier

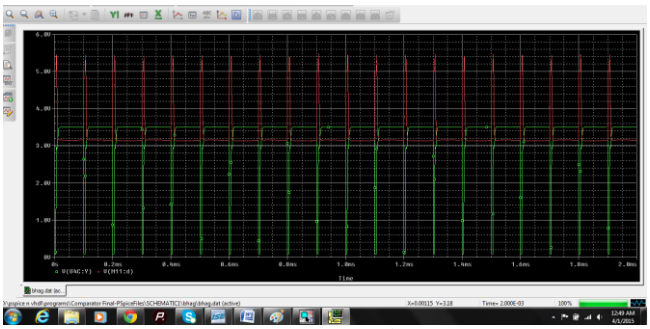

Fig. 9 Simulation result of Comparator

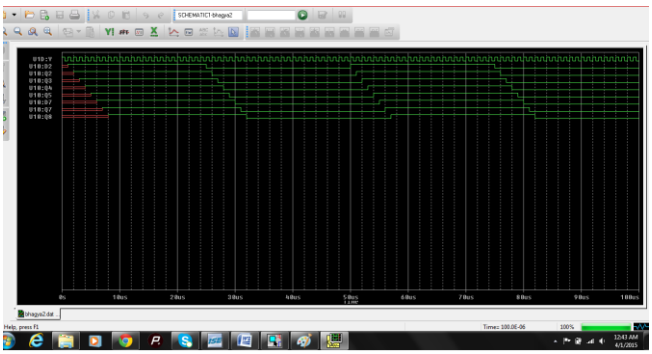

Fig. 11 Simulation of SAR Logic

Fig. 5 shows a schematic and a timing diagram of the .When the clock is switched to low conversion process starts. Sampling switches are turned ON by *Sample* which is the sample signal. After ten comparisons, *Sample* will be set to 1 to sample the input signal until the system clock, *Clk*, switches to 0. Therefore, the duty cycle of the system clock, *Clk*, is 50% and no PWM is needed for the integration application. The dynamic comparator generates the *Valid* signal after each comparison. *Clkc* is the control signal of the dynamic comparator. P_1 to P_{10} sample the digital output codes of the comparator and serve as control signals for the capacitor arrays to perform the switchback switching procedure.

D. Results

Fig 6, Fig 8 and Fig 10 shows the schematics of preamplifier, comparator and 10 bit SAR logic respectively. The above schematics have been created in PSPICE. Fig 7, Fig 9 shows simulation results of preamplifier and comparator respectively.

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