Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 07, July-2020

Implementation of Low Voltage Sub-Bandgap Voltage Reference in 90nm CMOS

Ritesh Soni
M.Tech in ECE
Department of Electronics and Communication Engineering
Goverment Engineering College,
Idukki Kerala, India

Prof. Sumam M J
Associate Professor
Department of Electronics and Communication Engineering
Goverment Engineering College,
Idukki Kerala, India

***Abstract*—The paper introduces a new low voltage design Sub-bandgap reference circuit consists of the MOSFETs and BJT subthreshold. The proposed sub-BGR circuit shall be implemented in a standard CMOS technology of 90 nm. The results achieved low power consumption in sub-BGR circuit and operated from 0.7v to 2v supply voltage. The simulation was carried out at voltage variations and temperature variation at range of -20°C－140°C on the cadence virtuoso using spectre simulator.**

Keywords—Subthreshold, voltage reference, Bandgap reference, Temperature coefffificient

I. INTRODUCTION

The increase in portable device usage has boosted to emphasis on minimizing power, speed and area. With the advancement of the semiconductor manufacturing technology the feature size of the devices had been reduced to nanometers. More devices are integrated on the same area of the chip, thus significantly improving system performance. The CMOS subthreshold voltage references (VRs) were operated with low supply voltage and consumed low power [1]. The VRs can be categorized as two types: one type relating to the bandgap voltage of Silicon or a fraction of it (i.e., subbandgap) with BJTs and resistors, The other was related to other factors such as MOS transistor threshold voltages and MOS transistor subthreshold parameters (For resistors with or without [1]–[4]. Although several low-power VRs were developed in [1]–[20], the other output voltage either increases exponentially or decreases linearly with temperature. The most popular on–chip integration solution is the Bandgap Voltage Reference (BGR), which can be used in standard CMOS technology that exploits parasitic vertical BJTs. Conventional BGRs produce an independent reference for low temperature, approximately 1.25 V and thus require a higher supply voltage that may not satisfy the low–voltage requirements for low–power applications. However, many approaches have been introduced using the BGR concept to maintain sub–1V Operation [3]. Bandgap references (BGRs) are widely used for generating a temperature-insensitive reference voltage determined by the bandgap of silicon[5]–[6]. The BGR typically uses PN diodes to produce both proportional-to-absolute (PTAT) and complementary-to-absolute (CTAT) temperature. The circuits given in [6] and [7] The switched-capacitor voltage divider and charge pump were used to achieve a complementary-to absolute-temperature division (CTAT) voltage (VBE) and low voltage power supply, but the temperature coefficient (TC) is as high as 75 ppm/°C and the temperature range is limited to be only 0°C–80°C [7]. CMOS VRs [8]–[12] has several issues remaining, such as leakage current consumption , low reference voltage of 257.5mv and wide area. In this work, we propose a CMOS subthreshold voltage reference (VR) implemented in a circuit. The reference voltage is biased with the temperature-independent , increasing performance and accuracy of circuit with very low sensitivity to variations in process, supply voltage. For the rest of the paper, Section II present the materials and methods of the voltage reference. The measurement results of a prototype design in a standard 0.90-µm CMOS process are introduced and analyzed in Section III.

II. PROPOSED VOLTAGE REFERENCE

Fig. 1 shows the proposed sub-BGR circuit using a single parasitic vertical PNP BJT, i.e., Q_0 to generate CTAT Voltage and poly-resistance R_2 for PTAT voltage generation. The circuit process can be described as the summation of two currents (one PTAT and the other CTAT). BJT 's base emitter forward voltage indicates a negative TC, for a bipolar system collector current I_C and saturation current I_S depends on temperature as shown below

$$I_C = I_s \exp\left(\frac{V_{BE}}{V_T}\right) \quad (1)$$

$$I_S = bT^{(4+m)} \exp\left(\frac{E_g}{KT}\right) \quad (2)$$

The current I_R flowing through the resistor R_2 is given by

$$I_R = \frac{V_{BE}}{R_2} \quad (3)$$

where VBE is the emitter-base voltage of Q_0 as shown in equation (3), the voltage V_{BE} should be decreased and R_2 increased in order to reduce the current I_R and thus the power consumption. Although, improving R_2 will eventually increase the chip area consumption.So the best way to do that is to

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 07, July-2020

minimize the V_{BE} value. Decreasing the Q_0 current often reduces its base-emitter voltage. Reducing V_{BE}, however, also where V_{BE} is the emitter-base voltage of Q_0 as shown in equation (3), the voltage V_{BE} should be decreased and R_2 increased in order to reduce the current I_R and thus the power consumption. Although, improving R_2 will eventually increase the chip area consumption.So the best way to do that is to minimize the V_{BE} value. Decreasing the Q_0 current often reduces its base-emitter voltage. Reducing V_{BE}, however, also reduces the negative TC or increases the absolute value of V_{BE} TC since V_{BE} derivative analysis is given as

$$\frac{\delta V_{BE}}{\delta T} = \frac{V_T}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{KT^2}V_T \quad (4)$$

$$\frac{\delta V_{BE}}{\delta T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \quad (5)$$

where m is the nonidentical factor of transistor, V_T is the thermal voltage, Eg is the bandgap energy of silicon, and q the elementary charge. The current through Q_0 should not be too small so as not to increase the required positive TC of the proportional-to-absolute-temperature (PTAT) voltage. To optimize the power and area, the current I_R through R_2 is chosen to be three times of the current through Q_0. The combination of the PMOS with a P+ poly resistor R_2 produces a PTAT current flow. Reference voltage with nominally zero temperature coefficient is obtained with negative and positive TC voltage. The circuit is designed using 90nm CMOS technology.

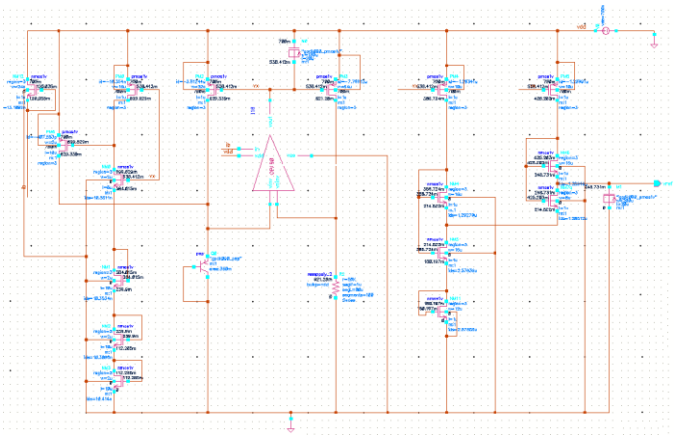

Fig. 1. Schematic of the proposed sub-BGR

The operational amplifier OPA shown in Fig. 2 enforces that nodes to have equal potential. The OPA uses the folded cascode structure to improve the loop gain and Power. The offset voltage of the OPA can be minimized by using large-size input transistors and coupling capacitor. The transistors PM_2- PM_3 are current mirrors and the size of PM_3 is approximately two times of PM_2 similarly PM_4-PM_5. The transistor NM_{11} work as diode connected NMOS , So the current through NM_{11} is the same as that of R_2.

The PTAT voltage generator consists of transistors NM_4-NM_7 all of which work in the subthreshold region. The subthreshold drain current I_D of a MOSFET is an exponential function of its gate source voltage V_{GS} and drain source voltage V_{DS}.

For $V_{DS} > 0.1$ V, drain current I_D is almost independent of V_{DS} and is approximately given by

$$I_D = K\mu C_{ox}(\eta - 1)V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (6)$$

$$\Delta V_{GS} = V_{GS5} - V_{GS4} = \eta V_T \ln\left(\frac{nK_4}{K_5}\right) \quad (7)$$

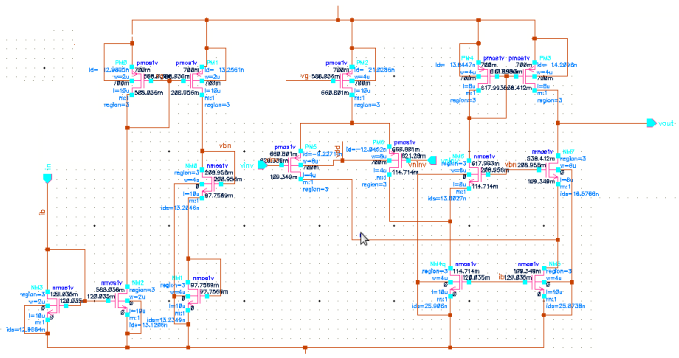

Fig. 2. Schematic of the OPA used in the Sub-BGR circuit..

where K is the aspect ratio (W/L) of the transistor, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, V_T is the thermal voltage, V_{TH} is the threshold voltage of the MOSFET, and η is the subthreshold slope factor. The drain source voltage V_{DS} of transistors NM_4-NM_7 are designed to be larger than 0.1 V. The threshold voltages of NM_4 and NM_5 are the same, and the drain current of NM_5 is two times that of NM_4, so the drain-source voltage of NM_5 can be derived from (6) is given by

$$V_{DS5} = \Delta V_{GS} = V_{GS5} - V_{GS4} = \eta V_T \ln\left(\frac{nK_4}{K_5}\right) \quad (8)$$

In a similar way, the voltage V_{DS7} is given by

$$V_{DS7} = \Delta V_{GS} = V_{GS7} - V_{GS6} = \eta V_T \ln\left(\frac{nK_6}{K_7}\right) \quad (9)$$

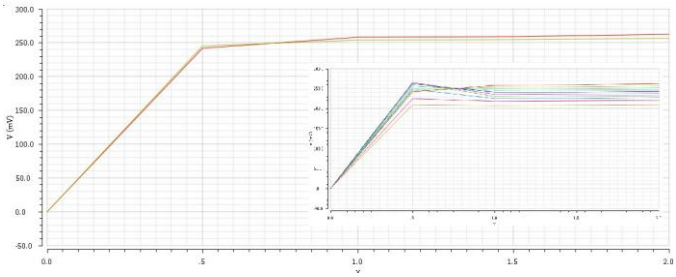

Fig. 3. Practically measured V_{ref} with respect to change in supply voltage.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 07, July-2020

Fig 3. Shows the simulated output voltage determined against 0v to 2v. Fig. 3. Simulated output voltage measured was also shown by temperature variation -20°C–140°C. The generated V_{ref} of the proposed sub-BGR is 248 mv and also associated in the PTAT term with the process parameter η in the PTAT term ,which is not constant in actual system and depends on the capacitance of the gate-oxide and depletion layer. Still the variance is not too large. The TC of V_{ref} is also related to the process parameter and the effect of parameter η on V_{ref} and TC of V_{ref} are similar , so output V_{ref} variation is very small . Therefore, the output voltage V_{ref} is given by

$$V_{ref} = V_{GS} + \frac{V_X}{R_2} V_{BE} + V_{of} \tag{10}$$

$$V_{ref} = nV_T \ln\left(\frac{nK_4K_6}{K_5K_7}\right) + \frac{V_{BE}}{R_2 gm_{11}} + V_{of} \tag{11}$$

The derivative of V_{ref} over temperature is given by

$$\frac{\delta V_{ref}}{\delta T} = \eta \frac{k}{q} \ln\left(\frac{nK_4K_6}{K_5K_7}\right) + \frac{K_N}{R_2 gm_{11}} \tag{12}$$

where K_N is the negative TC of V_{BE}. A zero TC can be obtained since the two terms of (12) can cancel each other with proper design, and hence V_{ref} would be stable across a temperature variation range. The absolute value of the negative TC is reduced by $1/gm_{11}R_2$ times compared with the traditional current-mode bandgap voltage reference . So the PTAT compensation factor of ($K_4K_6K_5K_7$) can also be reduced, which helps reduce the power and area of the PTAT circuit.

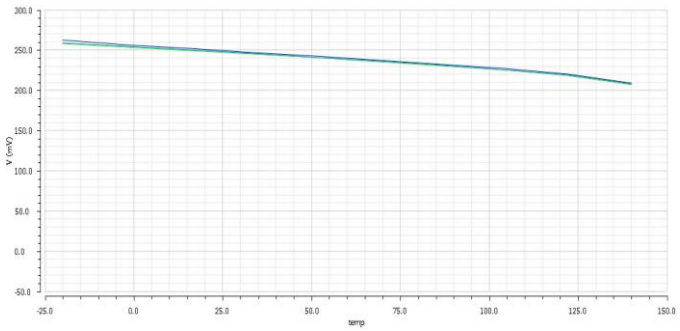

Fig. 4. Practically measured V_{ref} versus temperature .

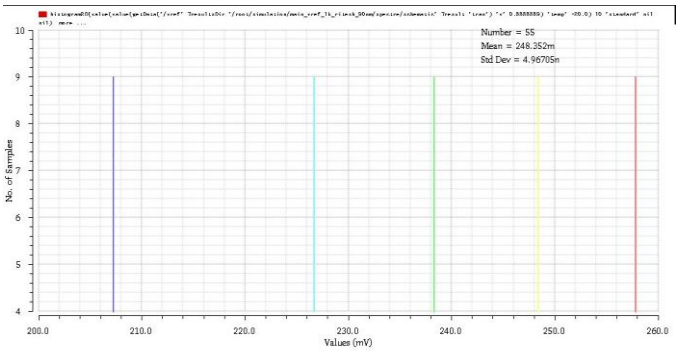

Fig. 5. Histogram simulation result of supply voltage.

III. RESULT

The proposed sub-BGR schematic is developed using cadence virtuoso tool in a standard 90-nm CMOS. Simulated output using Spectre simulator as shown in fifigures. Fig 4. shows the measured output voltage V_{ref} versus temperature variance range. Fig 5. shows the histogram simulation results of V_{ref} and TC. The average V_{ref} and standard deviation are 248.352 mv and 4.967 nV respectively, leading to a variation coefficient i.e minimum. Fig 6 and 7 show The spectral power of the sub-BGR proposed in Fig 6 shows Power versus voltage range from 0v to 2v and Power variation is nearly constant from 0.7v –2v. Fig 7. show the average power consumption and standard deviation are 457pw and 231pw respectively, with range of temperature -20°C–140°C.

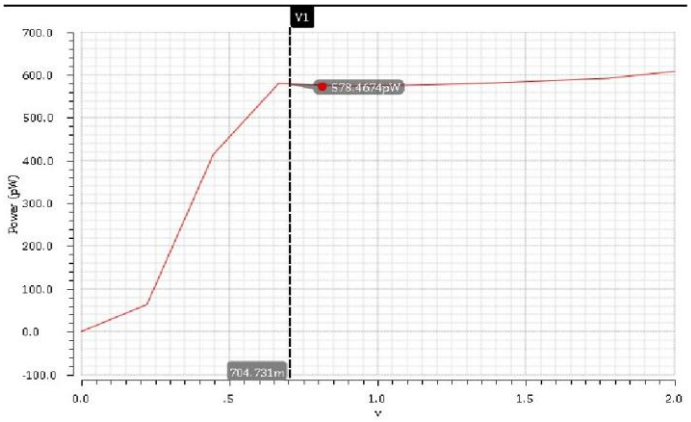

Fig. 6. Practically measured spectral power versus supply voltage.

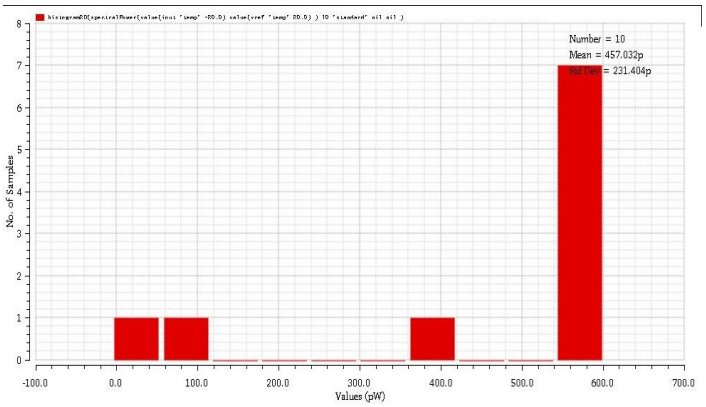

Fig. 7. Histogram simulation result of power.

REFERENCES

[1] D. Albano, F. Crupi, F. Cucchi, and G. Iannaccone, “A sub-T/q voltage reference operating at 150 mV”, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 8, pp. 1547–1551, Aug. 2015.

[2] Jinghui An , Chenjian Wu , Dacheng Xu, “A Wide Temperature Range 4.6 ppm/C Piecewise Curvature-Compensated Bandgap Reference With No Amplifiifiers” ,International Conference on IC Design and Technology (ICICDT), Aug. 2019.

[3] H. Banba et al., “A CMOS bandgap reference circuit with sub-1-V operation,” IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 670-674, May 1999.

[4] M. Kim and S. Cho, “A 0.8 V, 37 nW, 42 ppm/C sub-bandgap voltage reference with PSRR of 81 dB and line sensitivity of 51 ppm/V in

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 07, July-2020

0.18μm CMOS," in Proc. Symp. VLSI Circuits, Kyoto, Japan, pp. 144-145, Jun. 2017.

[5] J. M. Lee et al., "A 29 nW bandgap reference circuit," in IEEE Int. Solid State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 1-3 ,Feb. 2015.

[6] A. Shrivastava, K. Craig, N. E. Roberts, D. D. Wentzloff, and B. H. Calhoun, "A 32 nW bandgap reference voltage operational from 0.5 V supply for ultra-low power systems," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 13 , Feb. 2015.

[7] Y. Liu, C. Zhan, and L. Wang, "An ultralow power subthreshold CMOS voltage reference without requiring resistors or BJTs," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 26, no. 1, pp. 201-205, Jan. 2018.

[8] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V temperature-compensated subthreshold CMOS voltage reference," IEEE J. Solid-State Circuits, vol. 46, no. 2, pp. 465-474, Feb. 2011

[9] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V," IEEE J. Solid-State Circuits, vol. 47, no. 10, pp. 25342545, Oct. 2012.

[10] D. Wang, X. L. Tan, and P. K. Chan, "A 65-nm CMOS constant current source with reduced PVT variation," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 4, pp. 13731385, Apr. 2017.

[11] M.-E. Hwang and K. Roy, "A 135 mV 0.13 W process tolerant 6T subthreshold DTMOS SRAM in 90 nm technology," in Proc. IEEE Custom Integr. Circuits Conf. (CICC), pp. 419422 Sep. 2008.

[12] B. Razavi, Design of Analog CMOS Integrated Circuits. New York, NY, USA: McGraw-Hill, 2001.