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Implementation of Low Power Wallace Tree Multiplier using Carry Select Adder with BEC

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Abstract: **Multipliers are major blocks in the most of the digital and high performance systems such as Microprocessors, Signal processing Circuits, FIR filters etc. In the present scenario, Fast multipliers with less power consumption are leading with their performance. Wallace tree multiplier with carry select adder (CSLA) is one of the fastest multiplier but utilizes more area. To improve the performance of the multiplier, CSLA is replaced by binary excess-1 counter (BEC) which not only reduces the area at gate level but also reduces power consumption. Wallace tree multiplier using CSLA with BEC is occupying less area, memory and consuming less power when compared to Wallace tree multiplier using CSLA and Wallace tree multiplier. Area and power calculations for the Wallace tree multiplier using CSLA with BEC are giving good results compared to regular Wallace tree multiplier.**

Keywords*: *Wallace tree multiplier, carry select adder, BEC.

I . INTRODUCTION

Now-days the back end users are very interested in portability, durability, flexibility and remote control. To meet these requirements Integrated Chip (IC) technology has improved a lot. As there are many technologies, the present trend is Very Large Scale Integration (VLSI) technology, as in this technology many millions of transistors in the form of logic circuits can be integrated on a single chip. As the physical existing signals are analog signals, these are harder to process hence Digital Signal Processors (DSP) are introduced, in which the analog signal is converted into digital form processed according to the program inside it, again converted in to analog signal if required. As there are many modules in the DSP processor to implement the each function we have to program it, in this programming there are many operators used here. The mainly used and complicated block is multiply and Accumulate (MAC) unit, multiply and Add (MAD) units, these are large in area and more processing time required to execute this process.

Our main concept is to reduce these complications with this unit, so we use fusion techniques to have optimized design and many more optimized circuits with circuit minimization techniques are used have an optimized Sparse Parallel Prefix Adders operator design.

II.DESIGN OF PROPOSED ARCHITECTURE

2.1 Wallace tree multiplier for 4-bit

Step by step procedure for multiplying two four bit integers according to Wallace multiplier. Wallace multiplier consists of three steps.

1. Multiply each bit of one arguments with each bit of another argument, which results in n^2 products.
2. Consider the first three rows of the multiplied products and reduce them into two rows by using full adders and half adders as per the requirements. Repeat this process until two rows of multiplied products are obtained.
3. Normally in the case of four bit additions of two integers a sum of four bits and carry one bit is formed. So, in the last step of layer we first have two rows of products half adder to add last two bits and the carry of the half adder is connected to the next layer. By following the same procedure add all the bits of two rows. At last the sum of four bits can be obtained Coming to the solution of 4*4 Wallace tree multiplier; In first stage we obtain four rows of the multiplied products as shown in the Fig. 2.1.

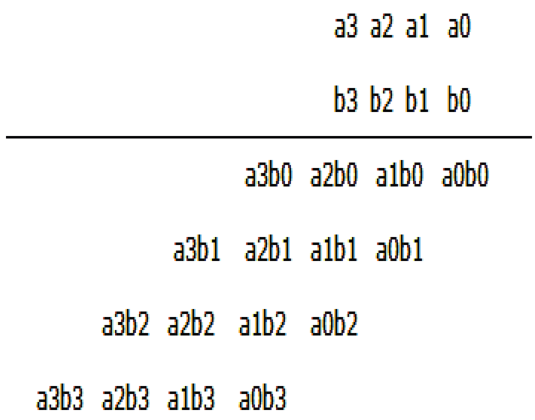

Fig: 2.1.Partial Products Generation

Now in the second stage choose the first three rows and reduce them into two rows by using half adders and full adders. As per the requirement it is needed two half adders and two full adders, sum and carry are generated as a0b0, s(0)c(0), s(1)c(1), s(2)c(2), s(3)c(3), a3b2 as in the Fig.2.2.

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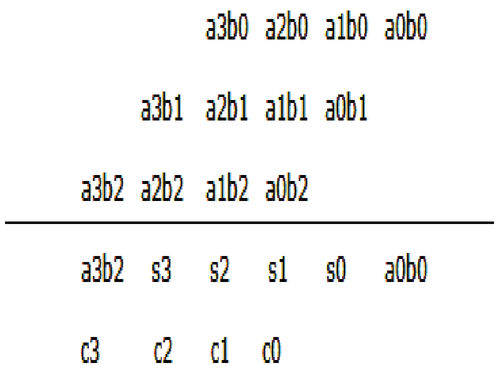

Fig: 2.2.Partioning and Addition of the Partial Products for Group1

These obtained products are added to the fourth row of the multiplied products in the third stage by this operation the results of sum and carry as a0b0, s(0), s(4)c(4), s(5)c(5), s(6)c(6), s(7)c(7), a3b3 are obtained here one half adder and three full adders are used, It is shown fig 2.3.

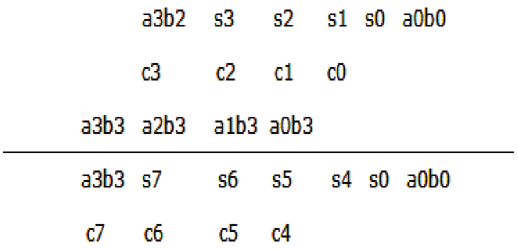

Fig: 2.3. Portioning and Addition of the Partial Products for Group2

Finally in the fourth stage again add this sum and carry to obtain the last stage products as a0b0, s(0), s(4), s(8), s(9), s(10), s(11)c(11),two half adders and three full adders are used in this stage as shown in the below Fig.2.4.

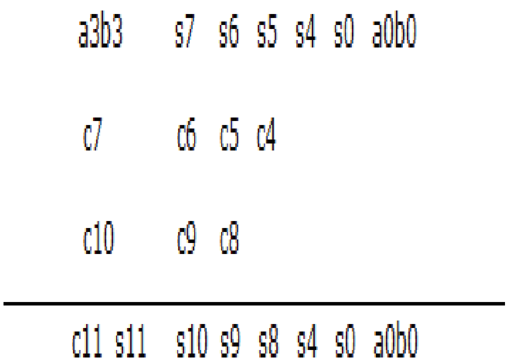

Fig: 2.4. Portioning and Addition of the Partial Products for Group3

2.1.1 Wallace Tree Multiplier Design

A method for fast multiplication was originally proposed by Wallace. Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. Using this method, a three step process is employed to multiply two integer numbers. The first step is to multiply each bit of one of the arguments, by each bit of the other, yielding *n2* results. Based on the position of the multiplied bits, the wires carry different weights. The second step is to reduce the number of partial products to two by layers of full and half adders. The third step is to group the wires in two and then add them using conventional adder. In this paper, two different architectures of Wallace tree multiplier are presented. First one is designed using only half adder and full adder, while the second one uses a more sophisticated carry skip adder (CSA).

2.1.2 Wallace Tree Multiplier using Full and Half Adders

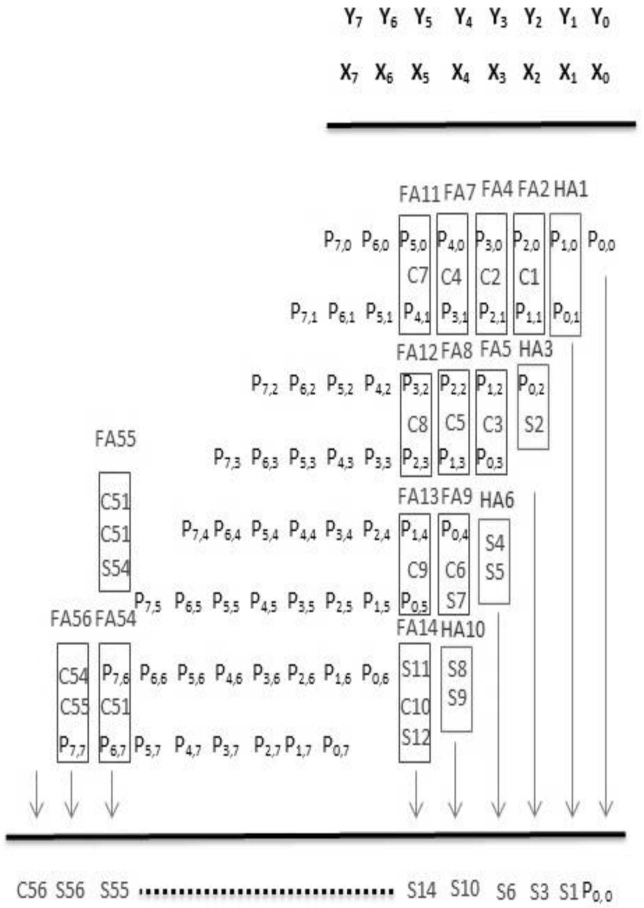

Fig: 2.5. Wallace Tree partial product addition using half and full adders.

The Wallace tree method reduces the number of adders by minimizing the number of half adders in any multiplier. In 8×8 multiplier, the first partial product is the least significant bit in the output of the multiplier result. After that, moving to the next column of the partial product if there are any adders from the previous product, the full adder is used otherwise a half adder is used and so on. Fig.2.5. shows how the algorithm is implemented.

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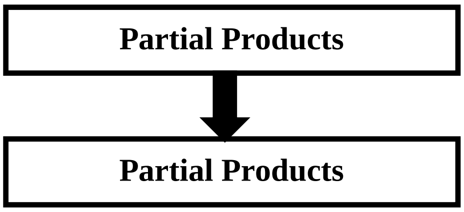
2.2. Wallace Tree Multiplier Using CSLA



Partial products obtained from the group 2 were given to the carry select adder, as this addition process reduces the delay as compared with the normal Wallace tree multiplier to generate the final multiplication products

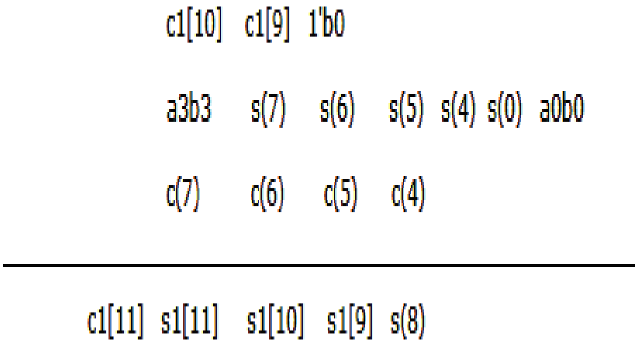


Fig: 2.6. Partitioning and Addition of the Partial Products when input carry is zero

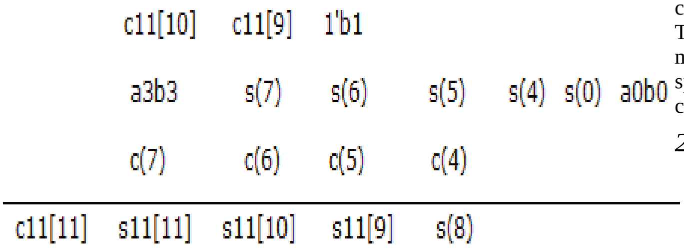


Fig: 2.7. Partitioning and Addition of the Partial Products when input carry is one

The CSLA operation takes place by assuming one of the carry bit as 1'b0 and 1'b1. here in this case we assume 1'b0 as c(8) and 1'b1.In the case of 1'b0 we get the results as c1(11) , s1(11) , s1(10) , s1(9) , s(0) , s(4) , s(8) , a0b0. In the next case c(8) as 1'b1 is assumed to get the result as a0b0 , s(0) , s(8) , s11(9) , s11(10) , s11(11) , c11(11).

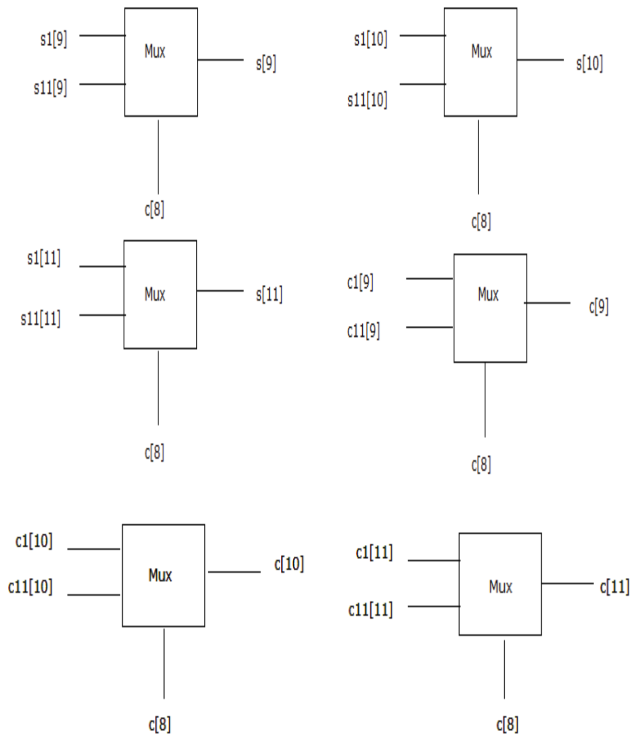


Fig: 2.8. Selection of final results by using Multiplexers

Depending on the value of carry bit c(8) the selection of the bits either from the case of 1'b0 or from the case of 1'b1 takes places and it is the required output. The selection of outputs using carry bit c(8) is clearly mentioned below using multiplexers. CSLA uses multiple ripple carry adders in order to increase speed but the area is very high .In order to reduce area, ripple carry adder with cin =1 is replaced by means of BEC.

2.3. Wallace Tree Multiplier Using CSLA With BEC:

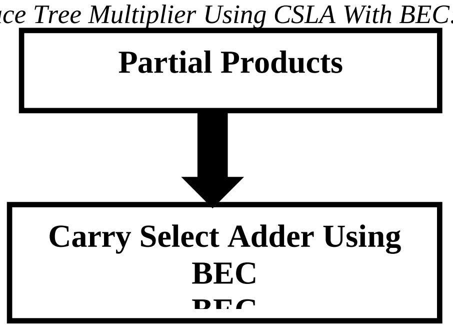


Fig: 2.9. Block diagram for Wallace Tree Multiplier using BEC

While using the carry select adder with BEC method , Partial products obtained from the group 2 were given to the carry select adder using BEC in order to reduce the delay and it uses less number of gates when compared to the Wallace tree multiplier using CSLA, and obtain the final products of the multiplication.

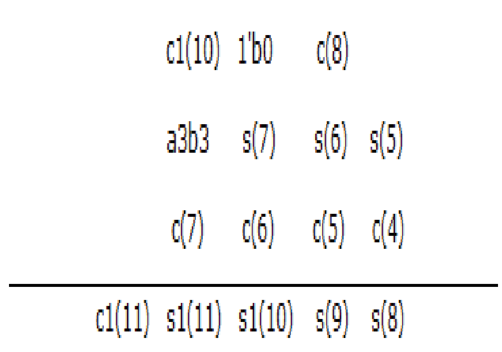


Fig.2.10.Partitioning and Addition of the Partial Products when input carry is zero

The main reason for using the carry select adder with BEC is to reduce the no. of gates when compared to normal Wallace multiplier. The 1'b1 case in normal CSA is replaced by BEC. The result from 1'b0 case is given as inputs to the BEC adder. Binary to excess-1 converter (BEC) to improve speed of addition. This logic can be implemented with any type of adders to further improve the speed. Using BEC instead of RCA in regular CSLA we can achieve low area and power consumption.

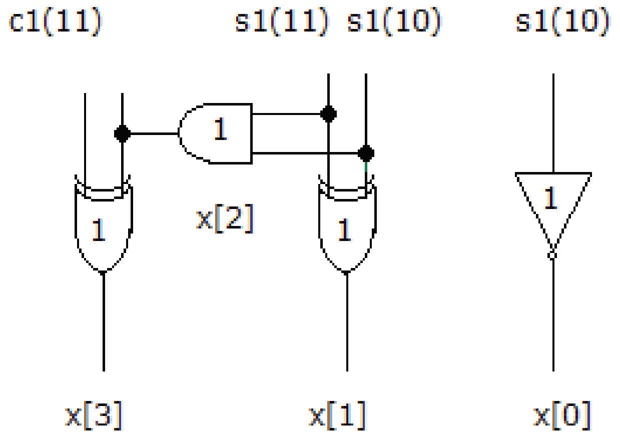


Fig.2.11. BEC with partial products as inputs

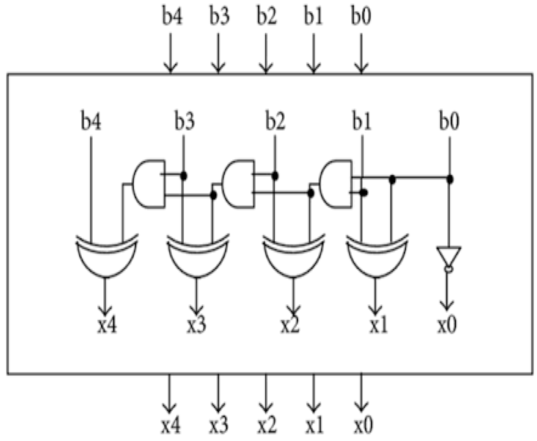


Fig.2.12. Block diagram of 4-bit Binary to Excess-1 converter

III. SIMULATION RESULTS

*3.1 4*4 Bit Wallace Tree Multiplier*

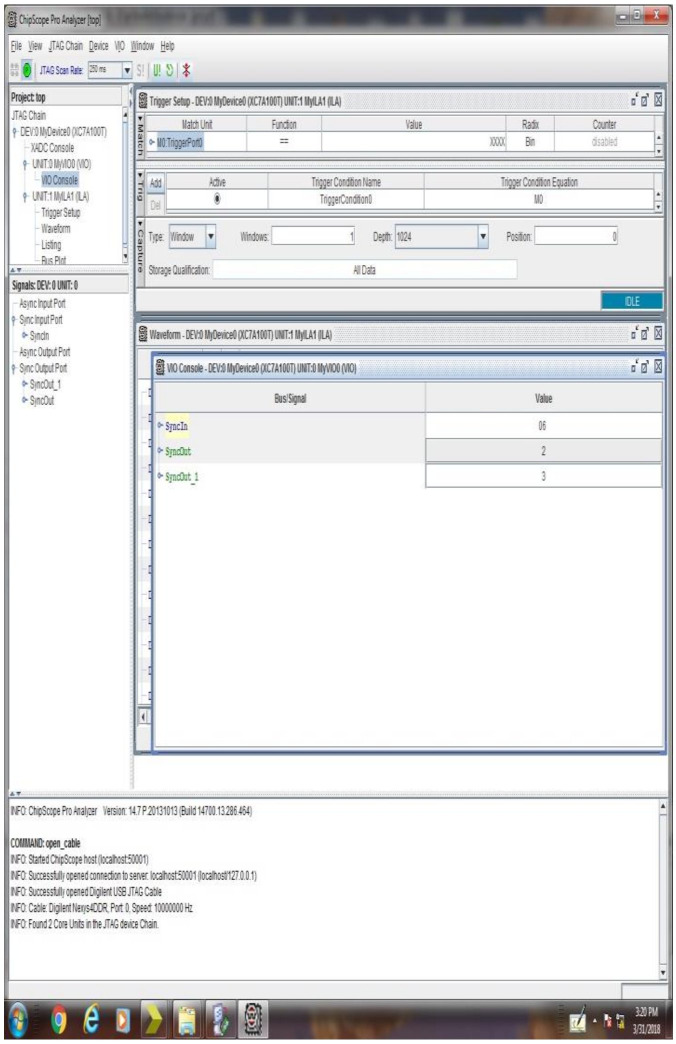


Fig.3.1 Simulation result for 4-bit Wallace tree multiplier

3.2 4-Bit Wallace Tree Multiplier Using Carry Select Adder

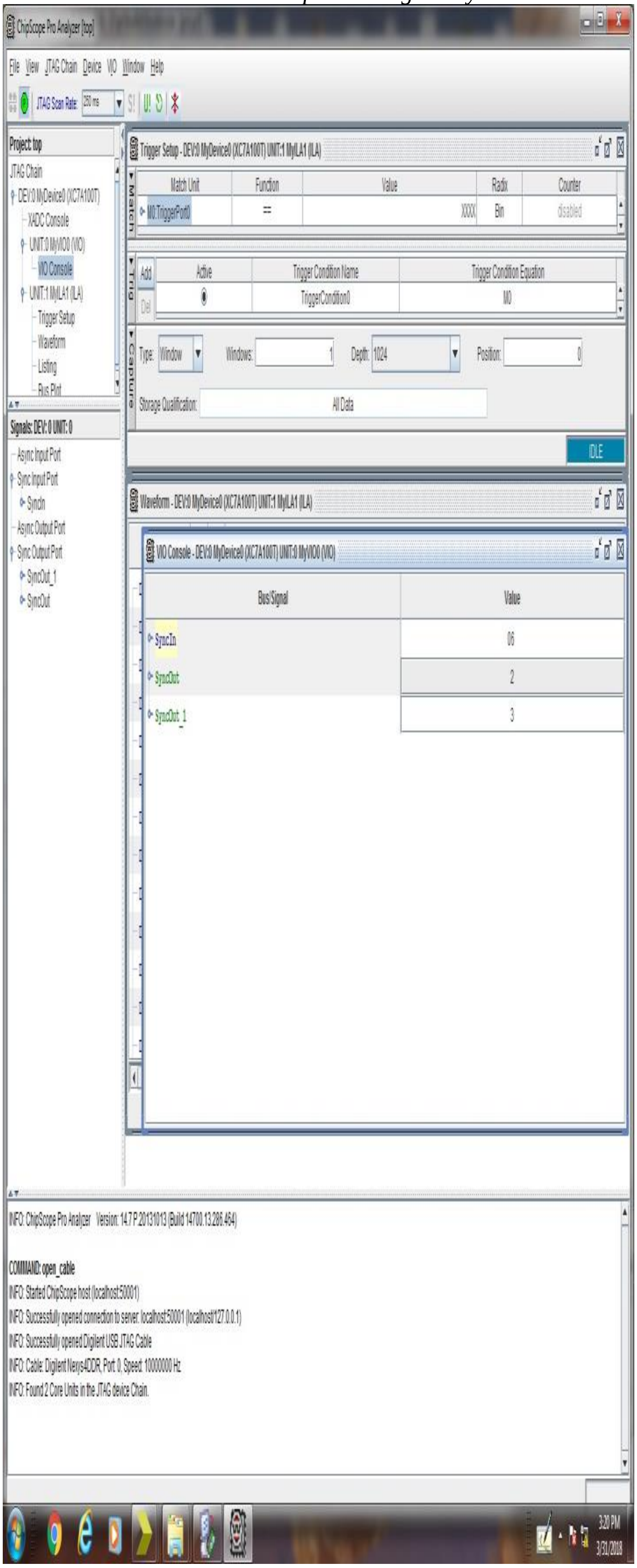


Fig.3.2 Simulation result for 4-Bit Wallace Tree Multiplier Using Carry Select Adder

3.3 4-Bit Wallace Tree Multiplier Using Carry Select Adder CSLA With BEC

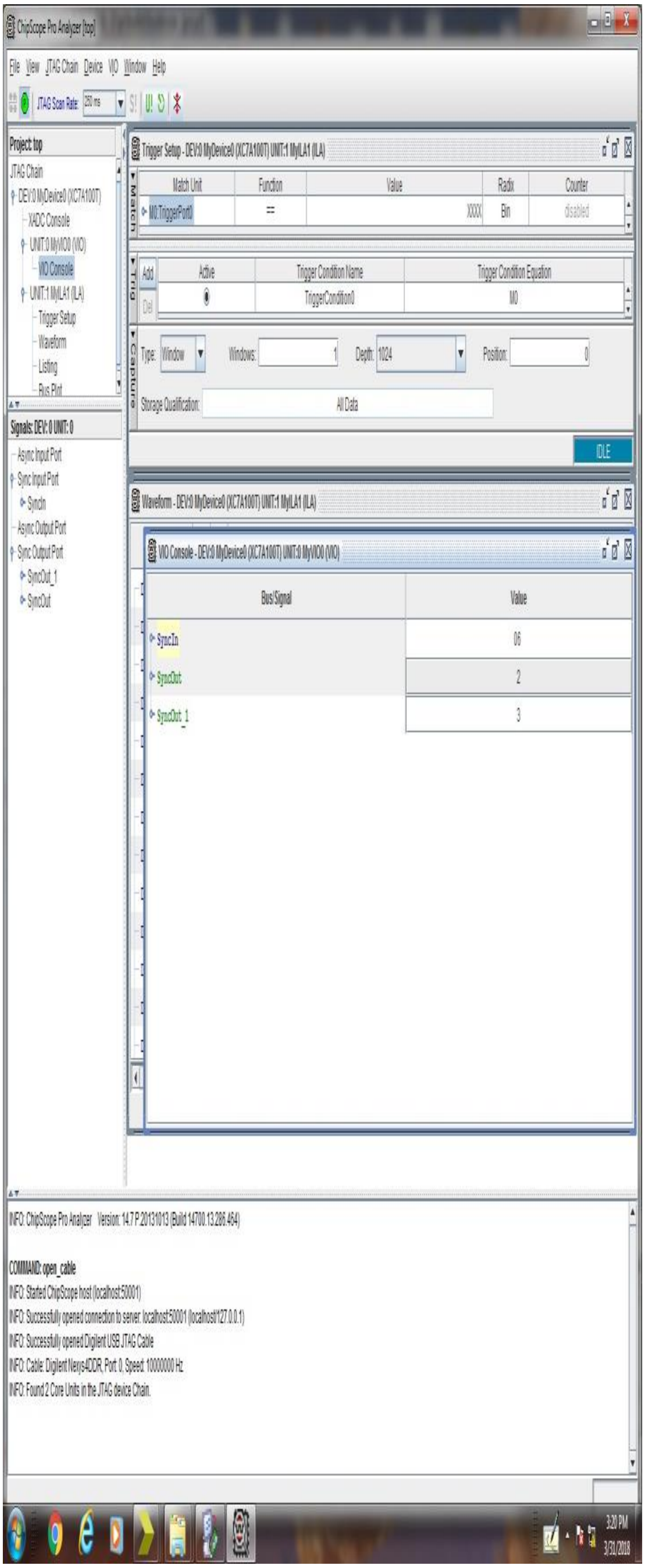


Fig.3.3 Simulation result for 4-Bit Wallace Tree Multiplier Using Carry Select Adder CSLA With BEC

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Table 3.1 : COMPARISON

Parameters	Wallace Tree Multiplier	Wallace tree Multiplier using CSLA	Wallace tree multiplier using CSLA with BEC
Memory (KB)	3,17,900	3,17,77	3,17,708
Delay (ns)	6.4944	6.380	1.855
Power (mW)	0.082	0.082	0.080

IV. CONCLUSION

A Simple approach is proposed in this project to reduce the area of Wallace tree multiplier using CSLA. From the above results it is observed that the Wallace tree multiplier using CSLA with BEC is occupying less area, memory and consuming less power when compared to Wallace tree multiplier using CSLA and Wallace tree multiplier. This approach is showing slightly higher delay when compared to the other two approaches. This design is synthesized using Xilinx ISE design suite 14.7 and is implemented on FPGA design of Artix 7 family.

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