International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 05, May-2015

Implementation of Interleaver Address Generator for Multimode Communication in WLAN

Kiran Koli
IV Semester M.Tech, Dept. of ECE
B.N.M Institute of Technology
Bengaluru, India

N. Sheshaprasad
Associate Professor, Dept. of ECE
B.N.M Institute of Technology
Bengaluru, India

***Abstract*—Interleaver address generator for multimode communication in WLAN satisfies all the modulation schemes used in 802.16e. The proposed model is finite state machine (FSM) based address generation with efficient use of FPGA memory block for storing the write and read address. In terms of maximum operating frequency, FSM based address generation performs better compared to the existing technique. Proposed design supports dynamic computation of interleaver address.**

Keywords—Interleaver, Address generator, Finite state machine, FPGA

I. INTRODUCTION

The unpredictable increase of internet usage in the last decade has dragged the quest of Broadband Wireless Access. BWA has emerged as last mile access solution and challenging competitor to the third generation technology (3G). It is gaining popularity at alarming rate as an alternative solution to Digital Subscriber Line (DSL). The basic requirements of broad band wireless access are turnaround time (TAT), high processing speed and flexibility. These necessities make the designers to choose reconfigurable hardware platform like field programmable gate array (FPGA). So system implemented on FPGA can be upgraded easily with the help of hardware description language (HDL). WiMAX is based on IEEE 802.16 standard for broadband wireless access system. IEEE 802.16d, now known as IEEE 802.16e adds mobility supports to IEEE 802.16 and defines standard for mobile broadband wireless access (BWA) in frequency band 2 to 6 GHz.

Interleaving contribute an important role in improving the performance of forward error correction (FEC) mechanism in terms of bit error rate. Basically interleaving can be defined as the process of rearranging code symbols so as to spread burst of errors into random like errors. To correct these errors, FEC algorithm can be used. Mainly two types of interleavers are being used in BWA such as Block interleaver and Convolution interleaver. Wimax uses special type of block interleaver in which the interleaver depth (ID) and pattern vary depending upon the code rate and modulation type. By observing various modulation schemes in Orthogonal Frequency Division Multiplexing (OFDM) based wireless local area network, it can be inferred that multimode interleaver is the best solution from implementation point of view.

The rest of the paper is organized as follows. The section II explains about the literature survey. Section III illustrates the System description. Section IV states results and discussion followed by conclusion and future work.

II. LITERATURE SURVEY

In the paper [1], author has compared the bit error rate of message signal with and without interleaver and has implemented the interleaver using different muxes and modulation schemes to improve the bit error performance.

In the paper [2], bursts of errors are distinguished from random errors. Then the philosophy of interleaving is illustrated by means of an example, i.e. interleaving process can convert a bursty channel into a random like one. Consequently, interleaving, together with a wide spectrum of readily available random error correction codes, can combat effectively the bursts of errors. Mainly this paper focuses on 2-D/3-D interleaving techniques.

In the paper [3], capability of designing and implementing an OFDM system was presented. This paper intends to show the capability of a straight forward translation of a wireless communication standard into a pure VHDL implementation in order to implement it on a reconfigurable platform. The divide and conquer approach was utilized to design and test each entity alone and then combine the complete system. The work has achieved the task of designing the digital baseband part of an OFDM transmitter that confirms to the standard of IEEE802.11a. However, the implemented design supports only the fixed data rates in the standard that is 6, 12 and 24 Mbps.

In the paper [4], the authors have implemented and evaluated a novel design for the hardware of the multi-mode interleaver block used in the OFDMA mode of the IEEE 802.16e standard. A new architecture with area and delay efficiency is introduced and the same is verified using quantitative comparisons between classical interleaver designs and FPGA implementations of this architecture.

III. SYSTEM DESCRIPTION

IEEE 802.16e based WiMAX system is as shown in Fig 1. In this system, the input binary data flow obtained from source is randomized in order to prevent a long run of ones and zeros, which causes timing recovery problem at the receiver end. Pseudorandom binary sequence is being used in which randomizations done by modulo 2 additions of the data with the output of the PBRS itself. Thereafter the randomized data bits are encoded using Reed Solomon encoder followed by convolution encoder. In conventional block interleaver bits received from the encoder are stored row wise in the interleaver's memory.

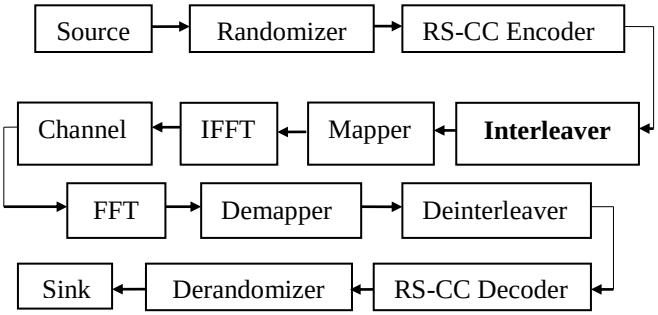

Fig 1: Overview of WiMAX PHY layer System

The instant the memory is entirely filled, the bits are read in column by column manner, and then the interleaving data comes to map per block where the modulation takes place. The data symbols resulting are used to construct OFDM symbols by Inverse Fourier Transform (IFFT). Cyclic prefix is used to reduce ISI. In the receiver side inverse blocks are applied by performing FFT, de-mapping, de-interleaving, decoding and de-randomization operations respectively to get the original data sequence.

A. Contribution of this paper

Design of interleaver address generator for WiMAX for BPSK,QPSK,16-QAM,64QAM with different code rates with various interleaving depth using FPGA internal memory.FSM based address generator is used which uses multiplexers, low power carry adder, flip –flop and counter. In the address generation part a low power carry select Adder is used, which increases address generator efficiency by reducing overall area and power parameters.

There are basically 2 types of interleavers being used in broadband wireless access, Block interleaver and Convolution interleaver. In WiMAX system the block interleaver used has different interleaving pattern for different modulation schemes and code rates [1]. In this case various interleaver depths are essential to incorporate various code rates and modulation scheme. The first step is to ensure that the adjacent coded bits are mapped onto nonadjacent sub carriers, which improves the performance of the decoder and provides frequency diversity. Then adjacent bits are alternately mapped to less and more significant bits of the modulation constellation to avoid long run of lowly reliable bits. The interleaving is a technique of reordering the encoded data such that the adjacent bits now become nonadjacent. The data stream received from the RS-CC encoder is permuted by using the two-step processes described by equation (1) and (2). These steps ensure mapping of coded bits onto nonadjacent subcarriers and alternate less/more significant bits of the modulation constellation, respectively.

$$m_k = \left(\frac{N_{cbps}}{d}\right)(k \,\%\, d) + \left\lfloor \frac{k}{d} \right\rfloor \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$j_k = sx\left\lfloor \frac{m_k}{s} \right\rfloor + \left(m_k + N_{cbps} - \left\lfloor \frac{dx\, m_k}{N_{cbps}} \right\rfloor\right) \% s \ldots\ldots (2)$$

Where: k= 0, 1……Ncbps-1.
Ncbps = Number of coded bits per sub channel.
s = Ncpc/2,
Where Ncpc is the number of coded bits per subcarrier.

Top level view of interleaver consists of 2 sections. They are interleaver memory and address generator as shown in Fig.2.Here address generator is a circuit which generates interleaver addresses according to the pre-determined permutation scheme; it generates both write and read addresses depending on the select (SEL) line.

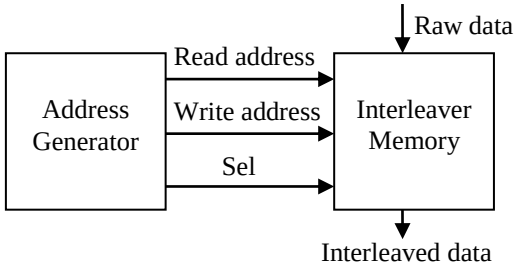

Fig 2: Top level view of WiMAX Interleaver

The encoded data is stored in bit addressable interleaver memory and according to the read addresses generated; data is read out to get the interleaved data. Similarly the data can be written into the interleaver memory according to the write addresses and data read out continuously.

Table I: Modulation schemes of various code rates and interleaving depth of IEEE 802.16e.

SI.No	Modulation Type	Code rate	Interleaver depth
1	BPSK	1/2	48
2	QPSK	1/2 3/4	96,288,384,432,480,576 144,192
3	16 QAM	1/2 3/4	192,384,576 288
4	64 QAM	1/2 2/3 3/4	288,576 384 432

The Table I consists of different modulation types, code rate and interleaver depth which shows up to what extent address generation process works with respect to given ieee 802.16e predefined values of WLAN.

To design the Interleaver address generator model many muxes are used. Each and every mux can be expressed as 2:1 mux while writing design code. In the Fig 3, first stage consists of 8 muxes to implement unequal increment of addresses used in 16-QAM (Quadrature amplitude modulation) and 64-QAM modulations. The selection is controlled by T-flip flop and MOD-3 counter for four muxes of 16-QAM and last four MUXs of 64-QAM respectively. In second stage the top most MUX contains 8 input lines with equal increment of address of different interleaver depth. The input to the second and third MUXs in second level is from the first level muxes outputs of 16 QAM and 64-QAM respectively.

Table II: Increment values of addresses with various Interleaving depth of different modulation schemes.

Modulati -on	**Mod -type**	**Code -rate**	**Inter -leaver depth**	**ID**	**Increm -ent values**	**Spac- ed equ- ally**
BPSK	00	1/2	48		3	Y
QPSK	01	1/2	96	000	6	Y
		3/4	144	001	9	Y
		1/2	192	010	12	Y
		1/2	288	011	18	Y
		1/2	384	100	24	Y
		3/4	432	101	27	Y
		1/2	480	110	30	Y
		1/2	576	111	36	Y
16-QAM	10	1/2	192	000	13,11	N
		3/4	288	001	19,17	N
		1/2	384	010	25,23	N
		1/2	576	011	37,35	N
64-QAM	11	1/2	288	X00	20,17,17	N
		2/3	384	X01	26,23,23	N
		3/4	432	X10	29,26,26	N
		1/2	576	X11	38,35,35	N

Table III: Address generation of different modulation schemes and interleaver Depths

BPSK Ncbps=48 Code rate=1/2	0	3	6	9	12	15	18	21
	24	27	30	33	36	39	42	45
	1	4	7	10	13	16	19	22
	25	28	31	34	37	40	43	46
QPSK Ncbps=96 Code rate=1/2	0	6	12	18	24	30	36	42
	48	54	60	66	72	78	84	90
	1	7	13	19	25	31	37	43
	49	55	61	67	73	79	85	91
16-QAM Ncbps=192 Code rate=1/2	0	13	24	37	48	61	72	85
	96	109	120	133	144	157	168	181
	1	12	25	36	49	60	73	84
	97	108	121	132	145	156	169	180
64-QAM Ncbps=288 Code rate =1/2	0	20	37	54	74	91	108	128
	145	162	182	199	216	236	253	270
	1	18	38	55	72	92	109	126
	146	163	180	200	217	234	254	271

The third stage contains one of the increment values from each MUX of the second stage and increment address of BPSK signal. Second stage consists of totally 3 muxes controlled by 3 bit selection line. Output from the third stage MUX acts as one of the inputs to the adder after required '0' padding. Another input of the adder is from Accumulator (ACC) output which is fed back to adder input which holds previous address. Once the addition is done a new address is written into the accumulator. The read addresses are generated by ten-bit up counter. When counter reaches its terminal count for the preferred modulation method, the counter resets to its initial state.

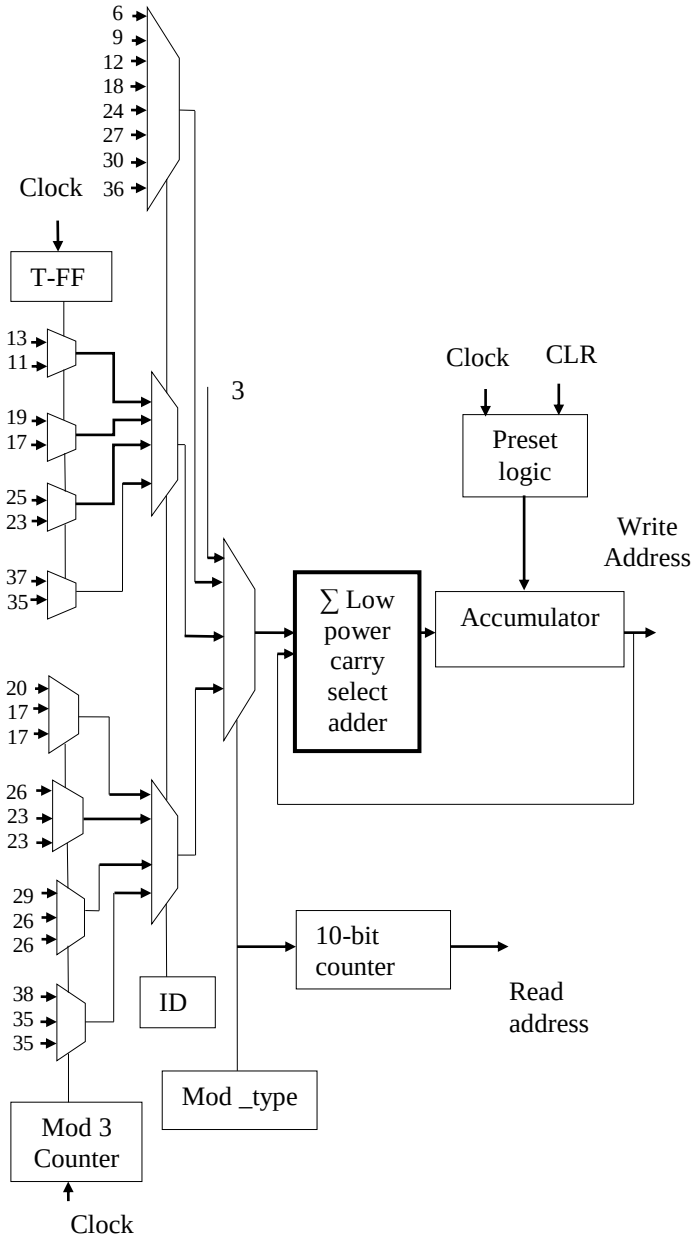

Fig 3: Interleaver Address Generator.

B. FSM for address generator

This finite state machine contains a 4-bit binary counter and it keeps the track of end of states during each iteration. When CLR=1, FSM enters into the first state. Depending upon the value of modulation scheme it makes transition to one of the next level state. The different states indicate one of the interleaver depths.

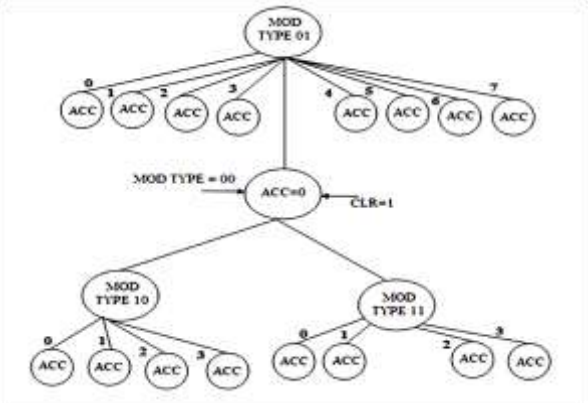

Fig 4: FSM for address generation

Based on the value of interleaver depth, one of state switches to next level of states. When FSM finishes the terminal value of first iteration, accumulator is loaded with the initial value of one for next iteration. After completing first iteration of 16 addresses, it keeps on repeating until the next modulation scheme of different interleaver depth is encountered. Preset Logic is controlled by clear and preset.

C. Interleaver Memory

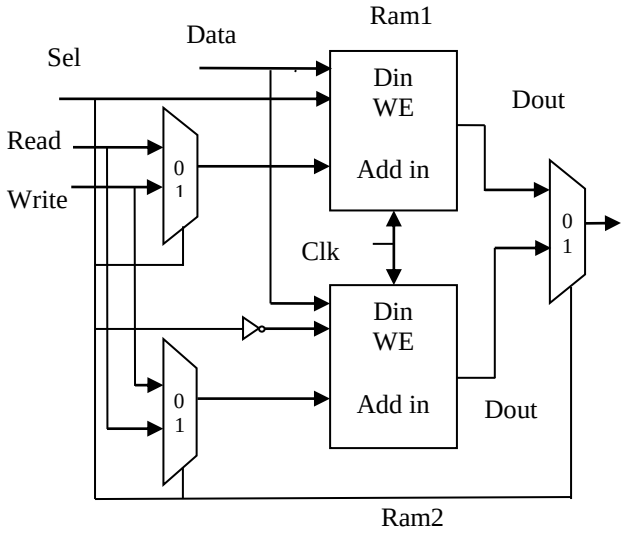

Fig 5: Schematic view of interleaver memory

The interleaver memory block consists of two memory blocks Ram 1 and Ram 2, one inverter and three MUXs as shown in Fig 5.In this case depending upon the selection line memory access operation takes place. So depending upon the read and write addresses, memory can be utilized with respect to clock signal, and in the above block interleaving when one memory block is being read, the other one is written and vice-versa. Each memory block receives either read address or write address with the help of the MUX connected to their address inputs and select line. Ram1 at the beginning receives the read address and Ram 2 gets the write address with write enable signal of Ram 2 active. After a particular memory block is written / read up to the desired location, the status of select line changes and the operation is reversed. The MUX at the memory output routes the interleaved data flow from the read memory block to the output.

IV. RESULTS AND DISCUSSION

The Fig 6, 7, 8 and 9 shows different address generation of different modulation schemes, with respect to MOD_TYPE and chosen ID values.

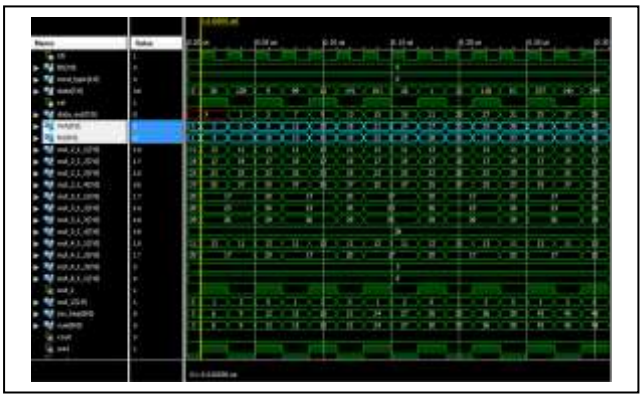

Fig 6: Generation of write and read address of BPSK with MOD_TYPE=00, ID=00

As the MOD_TYPE and ID values change it generates different addresses, and hence depending upon these modulation scheme is decided.

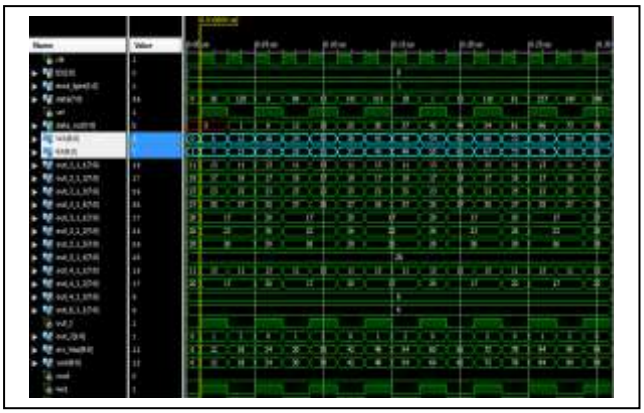

Fig 7: Generation of write and read address of QPSK with MOD_TYPE=01, ID=00

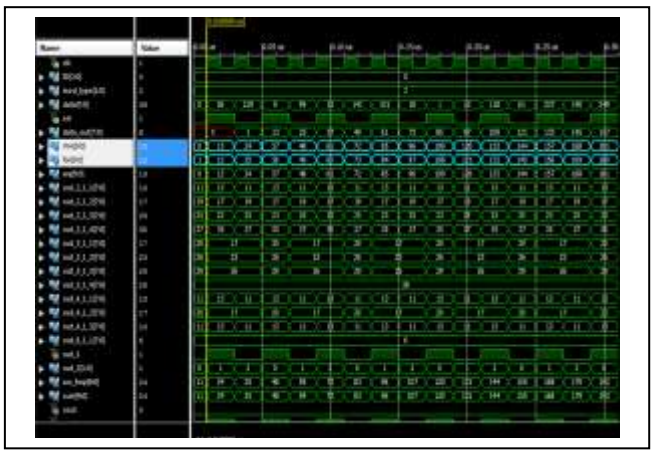

Fig 8: Generation of write and read address of 16-QAM with MOD_TYPE=10,ID=00

Fig 9: Generation of write and read address of 64-QAM with MOD_TYPE=11, ID=00

Table IV: Device utilization summary of proposed method

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	63	11440	0%
Number of Slice LUTs	108	5720	1%
Number of fully used LUT-FF pairs	59	112	52%
Number of bonded IOBs	27	102	26%
Number of Block RAM/FIFO	1	32	3%
Number of BUFG/BUFGCTRLs	2	16	12%

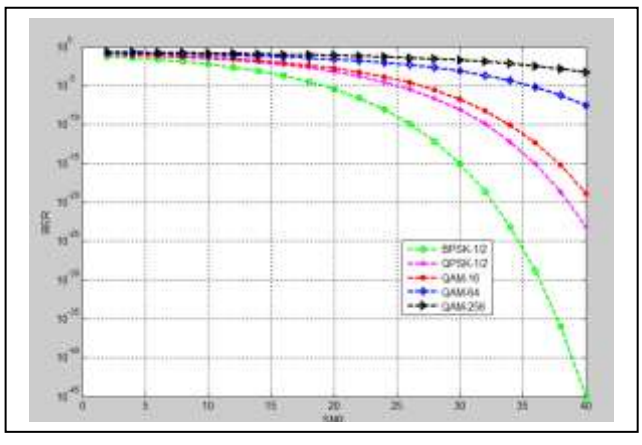

Fig 10: SNR vs. BER graph for different modulation scheme

Number of slice registers used in proposed method is 63 and its utilization percentage in a summary table is 0% as shown in Table IV. So it signifies less area is acquired by logic circuits and the power consumed is 0.015W. The Fig 10 shows bit error rate of different modulation techniques with signal to noise ratio and this MATLAB plot signifies that with the help of interleaver the bit error rate performance is improved for different modulation types with different code rate in presence of noisy channel.

V. Conclusion and Future Work

In this paper, FSM based address generator is used for generation of write and read address for interleaver memory. The Proposed model is implemented using low power carry select adder in Verilog. Different modulation schemes were used to generate the address depending upon variation of MOD_TYPE and ID with respect to clock. Different timing analysis report was obtained for the proposed method to know the area efficiency and other logic utilization summary. MATLAB is used to extract SNR vs. BER of BPSK, QPSK and QAM.

Future work: In this Paper, the main focus was to design the INTERLEAVER address generator. The future work may include design of the DEINTERLEAVER at the receiver circuit that will evaluate a more efficient design of address generator which will give required parameters like area, power consumption. Further reduction of the system delay may be designed which will improve the communication by avoiding the bit error and loss of information.

References

[1] Sagarika Mohanty,Dr. Noor Mahammad Sk, A novel interleaver design for multimode communication in WLAN,Internatioal conference on signal processing and integrated networks(SPIN),IEEE,pp. 286-290,2014.
[2] Y. Q. Shi, X. M. Zhang, Z. C. Ni, and N. Ansari, Interleaving for Combating Bursts of Errors, IEEE Circuits and System magazine, first quarter, pp. 29-42, 2004.
[3] A. Sghaier, S. Ariebi, and B. Dony, A pipelined implementation of OFDM transmission on reconfigurable platforms, CCECE08 Conference, pp. 801-804, December 2007.
[4] A.A.Khater, M. M. Khairy and S. E. D. Habib, Efficient FPGA Implementation for the IEEE 802.16e Interleaver, International Conference on Microelectronics, Morocco, pp. 181-184, 2009.
[5] J. B. Kim,Y. J.Lim, and M. H.Lee, A low complexity FEC Design for DAB, IEEEISCAS, pp.522-525, 2001.
[6] IEEE std. 802.11g-2003, Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications, Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band, July 2003.
[7] Design and implementation of a configurable Interleaver/Deinterleaver for Turbo Codes in 3GPP Standard, International Conference on Reconfigurable Computing and FPGAs, 2009.
[8] Multiband ofdm physical layer specification, 2005.Available at http://www.wimedia.org/
[9] M. Shukla, R.C.S. Chauhan, Ruchir Gupta,V.K. Srivastava, S.Tiwari, Performance Analysis of Tree Based Interleaver with Iterative IDMA Receivers using Optimum Power Allocation Algorithm,IEEE ,2011.
[10] B. Ramkumar and Harish M Kittur, Low Power and Area Efficient Carry Select Adder, IEEE transactions on very large scale integration (vlsi) systems, vol. 20, no. 2, february 2012.
[11] .A.Mary Juliet, Dr.S Jayashri, design analysis of deterministic interleaver for OFDM -IDMA system, International Conference on Signal Processing, Image Processing and Pattern Recognition [ICSIPR], 2013.