

# Implementation of Image Segmentation Using FPGA

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**Abstract-** The proposed work presents FPGA based architecture for image segmentation. It has found application in forensic science and also in digital multimedia for creating image dazzling effect. Currently the image processing algorithms are limited to software implementation which is slower due to the limited processor speed. So a dedicated processor for segmentation was required which was not possible until advancement in VLSI technology. Now more complex system can be integrated on a single chip providing a platform to process real time algorithms on hardware. Image Segmentation is an important technique in the area of image processing with wide applications in Medicine, Remote sensing to mention a few. A lot of research work is in progress in various areas resulting in many computationally efficient algorithms. There are conventional as well as improvised segmentation algorithms depending on the application. The choice of the technique in most cases depends on the application and image in question rather than a generalized method. The proposed work uses histogram method for segmentation. The conventional histogram method is modified to adopt for automatically determining the threshold for different regions in the image. The objective of this project is to realize the segmentation algorithm on FPGA. FPGA implementation renders it more useful for real time applications.

**Keywords:** FPGA, VLSI, segmentation, histogram.

## 1. INTRODUCTION:

Field Programmable Gate Array (FPGA) technology has become an alternative for the implementation of software algorithms. The unique structure of the FPGA has allowed the technology to be used in many applications from video surveillance to medical imaging applications. FPGA is a large-scale integrated circuit that can be re-programmed. The term "field programmable" refers to ability of changing the operation of the device. Gate array refers to the basic internal architecture that makes re-programming possible. Implementations of real-time image processing algorithms can be done on general purpose microprocessors. In certain instances, image processing algorithms are also implemented using digital signal processors and application specific integrated circuits. The application of FPGA in image processing has a large impact on image or video processing. This is due to the potential of the FPGA to have parallel and high computational density as compared to a general purpose microprocessor. This is coupled together with the ability of FPGA of being re-programmable that adds flexibility in the development of image processing algorithms on FPGA. During the recent years FPGAs have become the dominant

form of programmable logic. In comparison to previous programmable devices like PAL and CPLDs, FPGAs can implement far larger logic functions. FPGAs support sufficient logic to implement complete systems and sub-systems. FPGA exploit the increasing capacity of integrated circuits to provide designers with reconfigurable logic that can be programmed on application-specific basis. This drastically increases flexibility in both the design process and the final artifact by permitting one board-level design to perform many functions or to be upgraded in the field.

## 2. IMPLEMENTATION OF IMAGE SEGMENTATION USING FPGA

The Image segmentation is a very important application in the field of image processing. Image segmentation is the process of extracting features or regions of interest from an acquired image for further intelligent computer analysis. The image is sliced into multiple regions based on some property of the pixels. These properties are intensity, texture, position or some local or global statistical parameters. Segmentation using computer vision finds multiple applications especially in the area of biomedicine. The tissues or organs of interest need to be extracted from the images acquired using medical imaging techniques. The clear view of only the interested regions/organs will help the radiologist in earlier diagnosis and treatment [14]. Segmentation is also used intensively in areas such as pattern recognition, remote sensing, metallurgy etc. There are number of literatures on image segmentation both semiautomatic and automatic. Many segmentation algorithms have proved to be successful. But not much of work is done in the area of realizing hardware for any branch of image processing. [22] uses Seed growing method for segmentation. Here cell (i.e. pixel) network is used as the core of the architecture to implement segmentation with some degree of parallelism. An effort is made to integrate all the blocks used in the segmentation using histogram method.

### 5.2 Automatic Segmentation Algorithm Based On Dynamic Threshold:

Segmentation based on threshold is one of the primitive segmentation techniques. The proposed work has implemented a simple but efficient thresholding technique for segmentation on FPGA. Threshold values are chosen from the histogram. Histogram is a counter arranged as a vector

indexed from 0 to 255 (In a gray image pixels will vary from 0 to 255). Each counter will hold the number of pixels with the intensity value corresponding to the counter index. Conventional histogram fails when the peaks are not clearly defined or overlapping. We have overcome this problem by identifying peaks within a defined neighbourhood. Peaks are determined in each region. This ensures that every distinct region within the image is extracted separately.

5.2.1 The segmentation algorithm is described in the following steps:

Step 1. Determine the histogram of the image.

Step 2. Set a width for the neighbourhood within the histogram.

Step 3. Set the first counter in the histogram as the initial value.

Step 4. Get the maximum value within the specified width ranging from the initial value.

Step 5. Retain the maximum count value.

Step 6. Increment the initial value and repeat the previous two steps until the last count. This gives almost a smoothed histogram from the original histogram as shown in Fig.5.1

Step 7. Determine the largest Peak value and set this as the threshold.

Step 8. Segment the image based on this threshold. One region gets extracted. Set certain offset to the threshold value as there is always variations among the pixels representing the same information or region. This limitation is due to the scanning hardware.

Step 9. Look for the next largest value from the remaining peaks. Carry out the segmentation as mentioned in the previous step.

Step 10. Repeat step 9 till all the peaks are set for thresholding and segmenting.

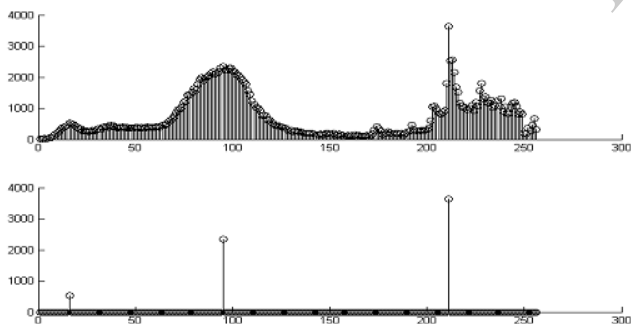


Fig 5.1 Histogram Showing Three Distinct Regions And The Second Figures Shows Three Peaks Extracted.

In the proposed algorithm threshold values are accurately and automatically determined for every region. Depending on the image the width of the region can be set. Fig. 5.1 shows the original histogram and the smoothed histogram to identify the different threshold values for the different regions present in the image. The threshold values are dynamically assigned from the histogram. This also enables the algorithm to segment image with any number of distinct regions. This makes the entire process of segmentation totally automatic.

### 5.3 FPGA Implementation:

The flow chart for FPGA implementation of image segmentation is shown in Fig. 5.2, gives the overview of the sequence of operations and different signals involved. The processor is provided with two pins for external interface viz: data/instruction and output/busy to indicate the nature of data available and the status of the processor. The data bus is eight bit wide and the data is read while the data/instruction is high. Every pixel is read in a single clock pulse. While the data/instruction pin is set low externally the available information correspond to the instruction which is decoded in the control unit and processed in the operator. Output/busy pin is set low by the processor while the processor is executing the instruction. Once the execution is over output/busy line is set high indicating that the processed data is available.

### 5.4 Segmentation Processor Architecture:

The proposed segmentation processor has the architecture shown in Fig. 5.3. It consists of five functional blocks: 1. Interface, 2. Interlacer, 3. Memory, 4. Operator and 5.

Control unit. The interface unit literally acts as the interface between the processor and the external data/instructions source. Interlacer unit is a register which converts the data from serial to parallel, parallel to serial and also provides serial in serial out, parallel in parallel out. Interlacer unit implements the parallelism in transferring the data too and fro between the memory and the external interface. The memory stores the pixels of the image. Operator performs the histogram calculation and thresholding part of the segmentation algorithm. And the control unit masters the interaction and timing of the different functional units.

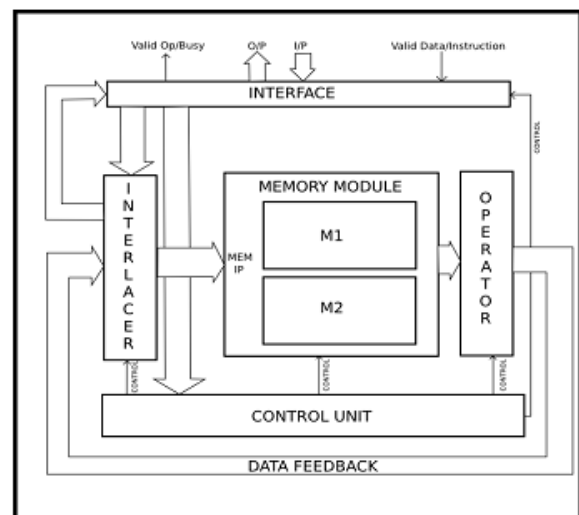


Fig 5.3 Architecture Of Segmentation Processor.

Fig 9.8 Original Image For Segmentation.

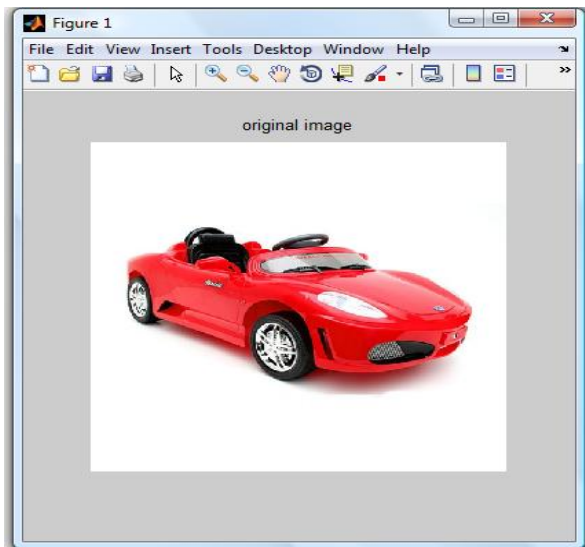


Fig 9.9 Gray Scale Image.

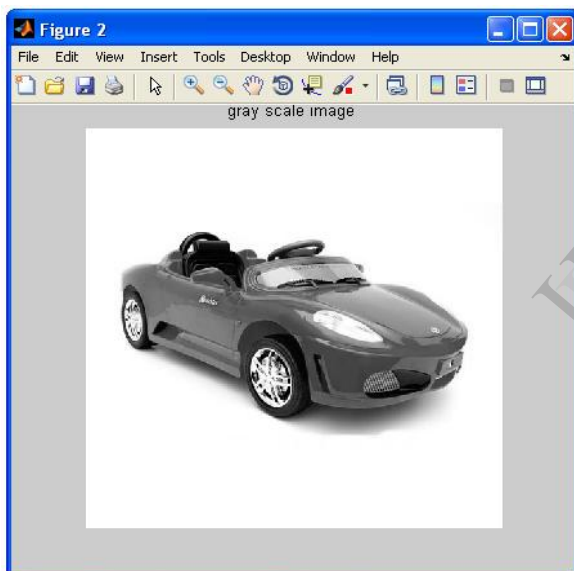


Fig 9.10 Segmentation Using Matlab.

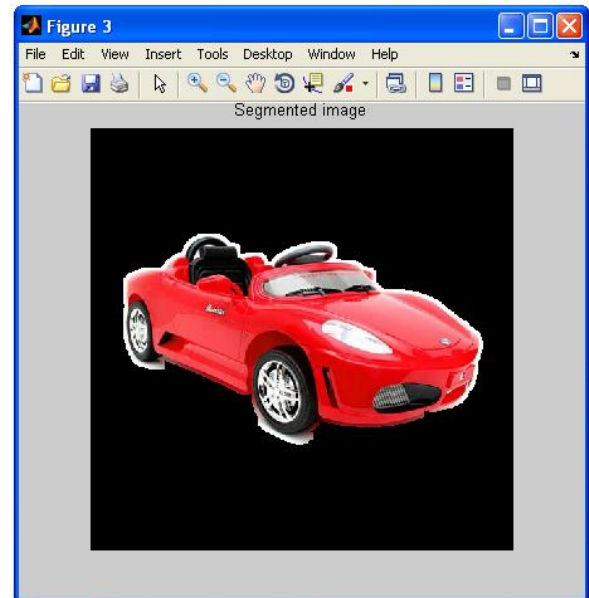
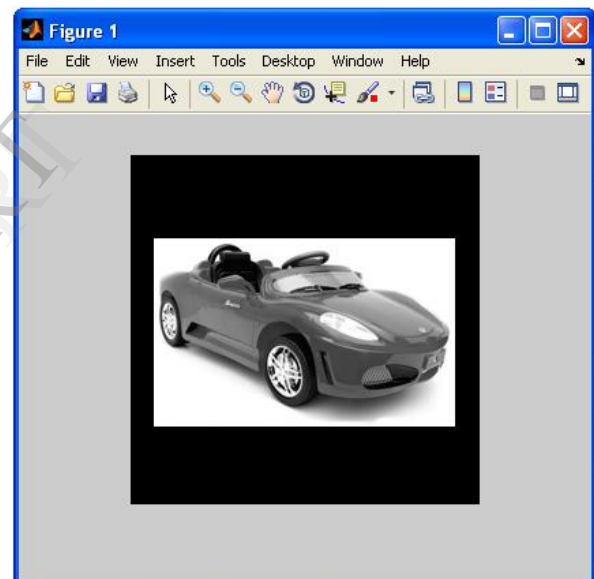


Fig 9.11 Output Of Vhdl Coding Using Segmentation Module.



More parallelism in the segmentation process can be introduced at the cost of increased hardware. The processor is can be designed such that more image processing techniques could be incorporated by putting additional functional blocks in the operator unit. The processor can then mimic an image processor at low cost hardware. In segmentation the other techniques like edge detection, region growing, model based fuzzy classification, neural network etc. can also be implemented and dumped on board for real time applications.

Applications:

- Fingerprint recognition.
- Face recognition.
- Vehicle number plate detection.
- Analysis of DNA sequences.

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