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Implementation of High-Speed Low Power32-Bit Dadda Multiplier using CLA

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***Abstract*: Multipliers and Adders are the basic hardware units in arithmetic operations. This project is implemented a 32-Bit Dadda multiplier using Carry Lookahead Adder (CLA) to reduce the delay, power consumption and increase speed while adding partial products in multipliers to get final sum quickly / Fastly. This project can be implemented/evaluated using Verilog HDL on Xilinx Vivado tool.**

***Keywords*: Dadda Multiplier, Carry LookAhead Adder, Verilog HDL.**

I. INTRODUCTION

Multiplication is the second most used arithmetic operation after addition, which has resulted in a large research interest in developing ways to improve the performance of multipliers. Multipliers have complex designs as a result of the large number of partial products that are formed during a multiplication; however, the general process can be broken down into three steps. The first step is to generate the partial product matrix. Each partial product is generated with an AND gate. As a result, N^2 AND gates are required in an N-by-N multiplier. The second step (referred to as the "reduction" step) is to reduce the N rows of partial products to 2 rows that have an equivalent value. This step has the most delay in a multiplier and is where most of the research effort, this report included, focuses on improving. The third step is to use a carry LookAhead adder (CLA) to add the 2 rows and obtain their sum which is the product of the two input operands.

There is a widely used approach, Dadda which are currently used in high-speed multipliers to perform the reduction step. This multiplier is constructed with half adders and full adders. By using these arithmetic components in parallel, a result can be obtained quickly. Moreover, by using carry lookahead adder the delay of the second step (the reduction) can be improved by up to 30%. The drawback is that the complexity of the design increases by up to 25%. The approach offers different benefits with regards to complexity and performance. This report analyzes the differences between the two adders RCA, CSLA with CLA.

II. LITERATURE SURVEY

Madhav Venkata, Srinivas Nandan, Sudhakar Alluri (2020) proposed an "HIGH PERFORMANCE 32-BIT
DADDA MULTIPLIER USING EDA". They design a 32-bit Dadda multiplier using SQRT CLSA with CBL which consumes less power but it comes with low speed & delay is high. In Dadda multiplier delay can be occurred, due to number of partial products during multiplication. The proposed project will be implemented with Dadda multiplier using CLA and simulated in Verilog language through Xilinx ISE tool. The proposed project aims in reducing the numbers of reducing partial products to get better power efficiency less delay and high speed [1].

s. manju, v. sornagopal, "An efficient of SQRT architecture of Carry Select Adder design by common Boolean logic" Carry Select adder (CSLA) is known to be the fastest adder among the Conventional adder structures. This work uses an efficient Carry select adder by sharing the Common Boolean logic (CLB) term. In this the logic simplification, we only need one OR gate and one inverter gate for carry and summation operation. Through the multiplexer, we can select the

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correct output according to the logic states of the carry in signal. Based on this modification square root CSLA (SQRT CSLA) architecture have been developed and compared with the regular and Modified SQRT CSLA architecture. The Modified CSLA architecture has been developed using Binary to Excess -I converter (BEC). This paper proposes an efficient method which replaces a BEC using common Boolean logic [2].

I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng we proposed an area-efficient carry select adder by sharing the common Boolean logic term. In this the logic simplification and sharing partial circuit, we only need one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal. In this way, the transistor counts in a 32-bit carry select adder can be greatly reduced from 1947 to 960. Moreover, the power consumption can be reduced from 1.26mw to 0.37mw as well as power delay product reduced from 2.14mw*ns to 1.28mw*ns [3].

III. IMPLEMENTATION

3.1 Dadda Multiplier using CLA Approach

The Dadda CLA multiplier differs from the Other Tree CLA multiplier by doing the minimum reduction required at each stage. Predetermined stage heights are used similar to how the original Dadda reduction uses predetermined stage heights. To find these predetermined stage heights, each stage can be no higher than 1.8 times the subsequent stage height. Since all multipliers must reduce eventually to two, the Dadda CLA stage heights were calculated to be: 2, 3, 5, 9, 16, 28, 50, etc.

A dot diagram for a Dadda CLA 32-bit by 32-bit multiplier is shown in Figure 1. Like the 32- bit by 32-bit Dadda CLA reduction achieves the performance by completing the reduction in 4 stages. The total complexity of this 32-bit by 32-bit Dadda CLA reduction is 1031 gates which is approximately 5% lower than the other tree multipliers.

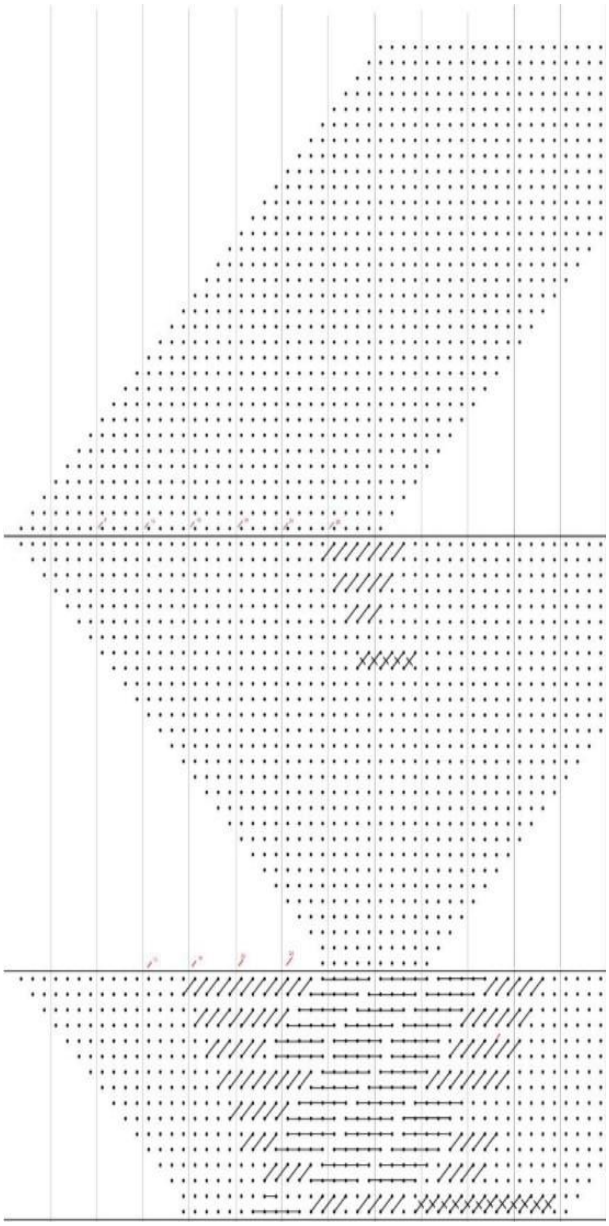

Figure 1: Dadda CLA 32-Bit by 32-Bit Reduction

Compared to the Other Tree CLA multiplier, the Dadda CLA approach does most of its reduction in the middle of its reduction stages; this makes it less attractive for pipelined multiplication.

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IV. SIMULATION RESULTS

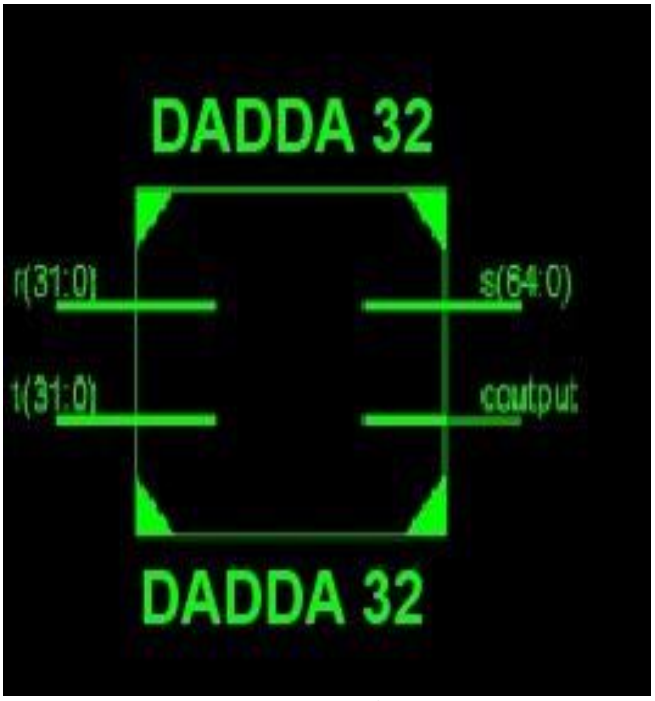

Figure 2: RTL Schematic Diagram of 32-Bit DaddaMultiplier

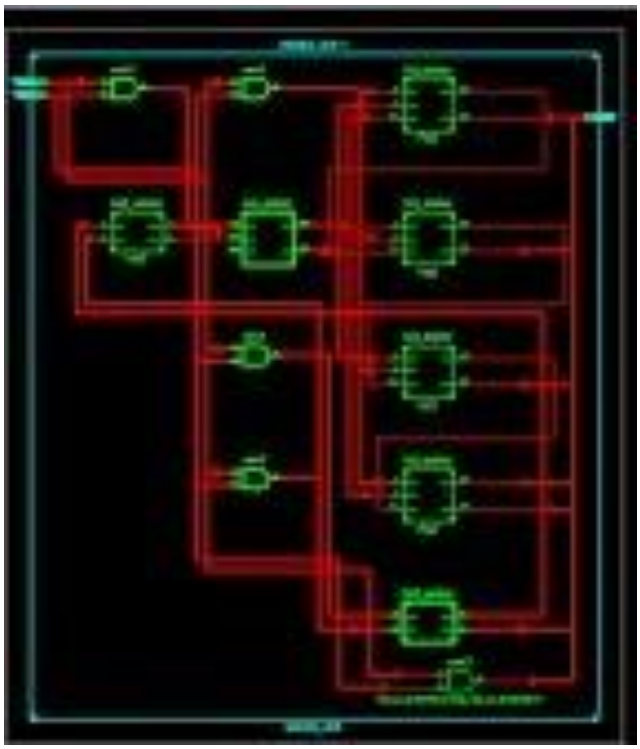

Figure 3: RTL Schematic Diagram of 32-Bit DaddaMultiplier

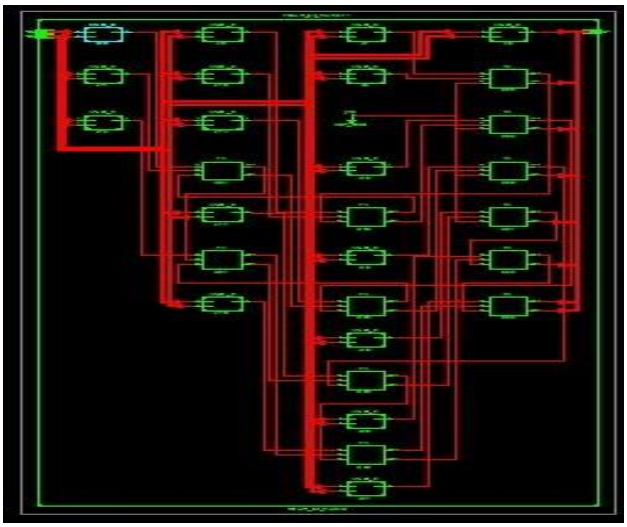

Figure 4: Technology Schematic Diagram of 32-BitDadda Multiplier

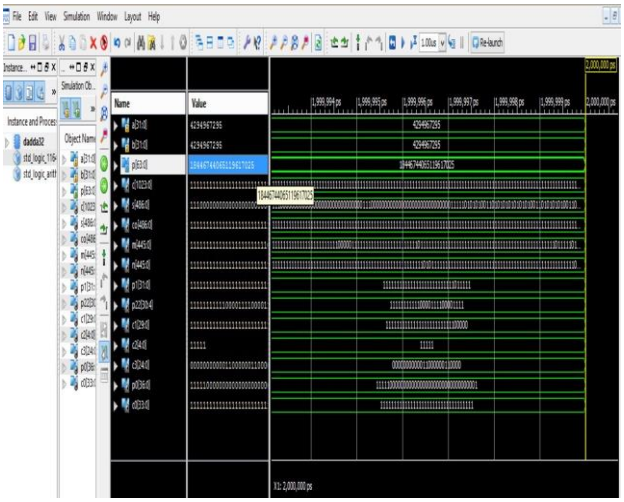

Figure 5: Output Waveform of 32-Bit Dadda Multiplier

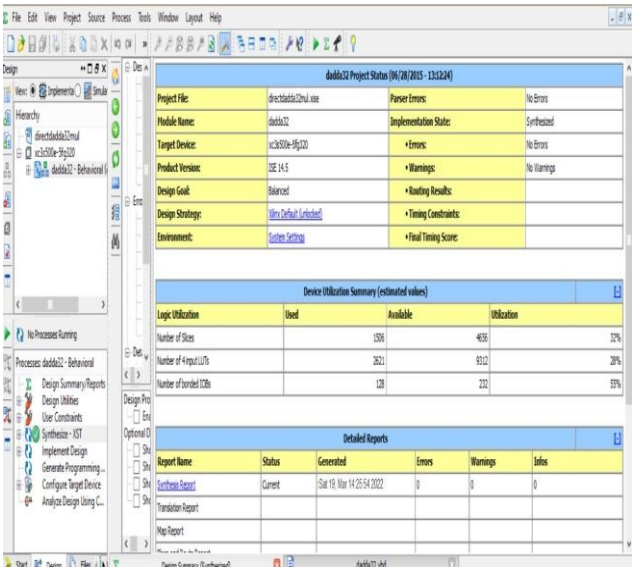

Figure 6: Summary Report of 32-Bit Dadda Multiplier

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Table 1: Comparison of 32-Bit Dadda Multiplier

Wordsize	Adder	No.ofLut's	Delay inns	Power inmW
32_bit	RCA	2957	42.329	339
32_bit	CSLA	2957	36.415	206
32_bit	CLA	1453	32.218	112.689

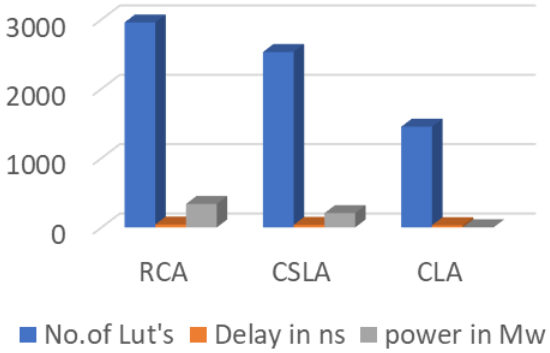

Figure 7: Comparison of Multiplier of Area, Delay andPower

V. CONCLUSION

The implemented design in this work has been synthesized using Xilinx ISE 14.7. The simulated files are imported into the synthesized tool and corresponding values of delay and power are noted. The synthesized report contains area, delay power value for Dadda multiplier. From these results, it is clear that the delay calculation of our project method is reduced by 60%. Multiplier power consumption is also reduced. In future, the project can be extended to produce accurate result.

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