Implementation Of Distance Protection Scheme Using Advanced DSP Techniques

Vidyarani K. R, Satheesh K R and Subhash R Srivatsa

***Abstract*—This paper presents the impact of changes in distance protection algorithm when performing simplifications in certain calculations. Advancements in digital technology have allowed relay manufacturers to include more and more relay functions within a single hardware platform. This paper presents digital power system protection implementation using dsPIC33F microcontroller using Fast Fourier Transform technique. The analog input signal is converted to its digital equivalent through a suitable 16-bit ADC and is further processed using complex Fast Fourier Transform algorithm to extract the fundamental frequency magnitude. Once this magnitude is obtained, it is fed to the internal relay algorithm to initiate appropriate actions. In this paper, implementation of distance relay using mho characteristic is explained.**

***Index Terms*—Analog to Digital Converter (ADC), Digital Signal Processing (DSP), Discrete Fourier transform (DFT), Distance Protection, Fast Fourier Transform (FFT), Power System Protection.**

I. INTRODUCTION

The development in the area of power system protection has taken a view in the technological advancements in electronics especially with the introduction of new designs in microprocessor technology such as microcontrollers and DSPs [1]. Also the availability of commercial software packages such as MATLAB [2] and Mipower [3] software which support educationally oriented power system block sets enable simulation studies to be carried out for power system protection application.

Power systems are designed so that protective relays are used to sense and isolate faults quickly. The main objective of this paper is to increase the speed of operation of protection relays. Protective relays are essential components in power systems because they can minimize huge losses of production due to unnecessary equipment damage as a result of fault or overload. Other considerations are safety, property losses, and replacements [4].

A numerical protection relay is an intelligent electronic device used for power system protection. Due to the rapid

growth of power system infrastructure, need for fast, reliable relays with advanced functionality to protect the major

components of power system and to maintain the system stability is inevitable [4]. The conventional protective relays are either electromechanical or solid state type. The electromechanical relays have several drawbacks such as high burden on instrument transformers, high operating time, mechanical wear and tear etc. The solid state relays have been increasingly used in recent years because of the inherent advantages of compactness, low burden, less maintenance and high speed. Though successfully used, the solid state relays suffer from number of disadvantages, e.g. lack of flexibility, inadaptability to changing system conditions and complexity.

The concept of numerical protection using computers show that improved performance has evolved during past two decades. Numerical relay uses state-of-art digital signal processing techniques to measure the relay parameters there by eliminating the complex analog circuitry. With the development of Very Large Scale Integration (VLSI) technology, fast and sophisticated microprocessors are now available at low cost. This has created a tremendous interest in developing microprocessor based protective relays. Their application to power system protection results faster, more accurate and reliable relays than existing ones. The addition of microprocessors increases the flexibility of relays due to its programmable approach.

II. METHODOLOGY

Most of the numerical relays currently in operation are implemented using complex DFT algorithm to extract the magnitude from the incoming signal. DFT plays an important role in analysis and design of signal processing systems. The basic properties of the DFT

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make it particularly convenient to analyze and design systems. It is important to have efficient algorithms to compute the DFT as it is an important component in many practical applications. DFT requires 2048 complex multiplications [5] for N=32, and hence it takes maximum processor time for extracting the magnitude. Due to this, computation time increases. Implementing FFT algorithm optimizes the DFT by eliminating redundant calculations. The FFT is a class of efficient DFT implementations that produces results identical to the DFT in much fewer instruction cycles to calculate the magnitude of incoming signal [5].

III. Modeling and Generation of Data

The Electromagnetic Transient analysis moduleis the simulation tool that is used to simulate theelectromagnetic transient phenomenon, power system fault analysis, and it is one of the most widely used programs in the electric utility [6]. To generate the transient fault data, Electromagnetic Transient Analysis module-MiPower has been used [3]. Based on MiPower software tool, a large number of data files have been generated by simulating various types of faults on a sample power system model. The power system model selected for this purpose is shown in Fig.1.

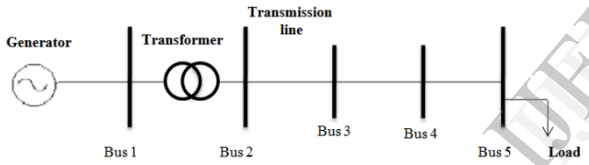

Fig.1. Power system model for generation of Data

The sample power system has a 11kV generator of 500MVA capacity, a 11kV/400kV, 500MVA step up transformer, 400kV, 300 kms long transmission line and a load of 400MW at 0.95 p.f. The fault is created at Bus 4 (fault bus). The faults are created at 0.03 seconds after the start of simulation. To store the data, a sampling rate of 60 samples/cycle (3000Hz sampling frequency) is chosen, so that the waveforms can be recorded accurately.

IV. Matlab Based Simulation of the Digital Fir Filters

The typical simulated waveforms of current and voltage for L-G fault (A-G) created at Bus 4 are shown in Fig.2 and Fig.3. The simulation is conducted using MiPower Eelectromagnetic Transient analysis module. It can be observed that there is considerable decaying Direct Current (DC) component present in current signal, whereas not much disturbance can be seen in voltage signal [7]. As a result, input signals to the relay are contaminated with noise, which must be rejected to retain signal quantities of interest. Distance relays need fundamental frequency components for estimation of resistance and reactance parameters.

This section explains a digital band-pass filter, which passes the fundamental component of the fault signals and attenuates other frequency components including the decaying DC offset and the harmonics of the fundamental frequency. The output of the digital band-pass filter is fed to the algorithm for impedance calculations.

Simulation studies with Finite Impulse Response (FIR) filters have been carried out. FIR filter has the advantage of having a linear frequency-phase response i.e. it delays all frequencies by same amount. Also, it does not contain feedback terms [5]. Specifically, the FIR filter is designed using a Kaiser window of type band pass and the sampling frequency chosen is 3000Hz; the pass band and stop band frequency is 40Hz and 60Hz respectively. Fig.4 shows the frequency response of Kaiser Window output. However, frequencies beyond the pass-band being attenuated, this error may be marginal. Also it will be used to maintain the symmetry of the signal by removing the DC component present in a signal. Filter coefficients are multiplied with incoming voltage sample to remove the DC component [6]. Fig.5 and Fig.6 show the output of the 60th order band pass FIR filter for fault at 60% of the transmission line and 90% of the transmission line respectively.

For the power system model shown in Fig.1, the twin moose conductor is chosen whose resistance and reactance values are 0.0328Ω/km and 0.332Ω/km respectively. The base voltage is 400KV, base current is 144.33A and base impedance is 1600Ω. The mho characteristic is set for 80% of the line length i.e. 240km.

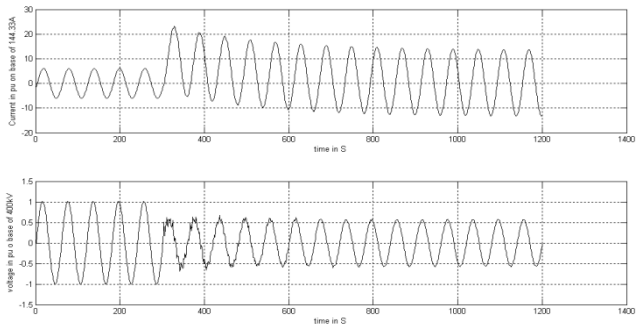

Fig.2. Sample Fault signals at 60% of the transmission line

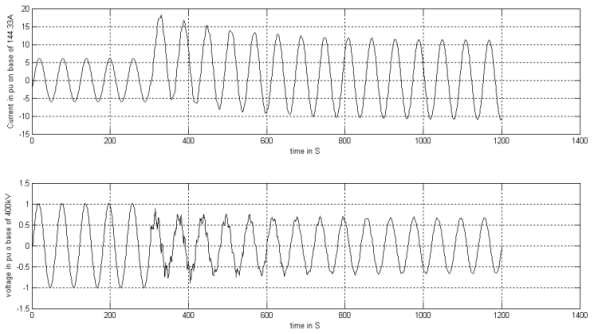

Fig.3. Sample Fault signals at 90% of the transmission line

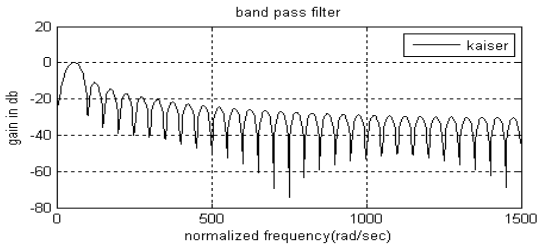

Fig.4. Frequency response of Kaiser Window

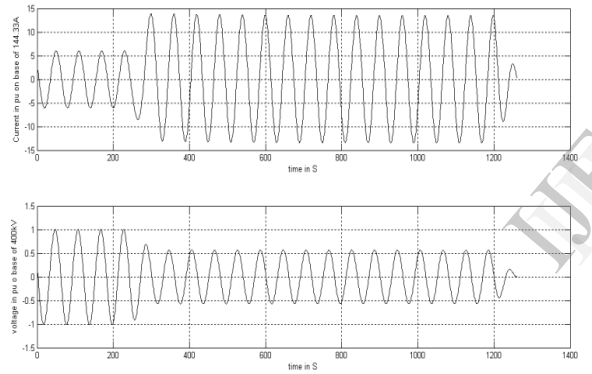

Fig.5. Output of the 60th order band pass FIR filter for fault at 60% transmission line

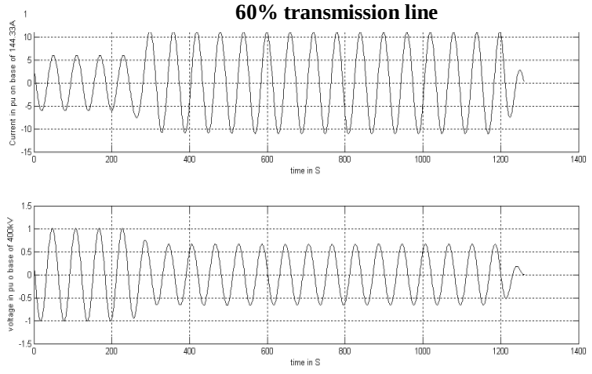

Fig.6. Output of the 60th order band pass FIR filter for fault at 90% transmission line

V. Implementation of Digital Power System Protection

Fig.7 shows the block diagram of numerical power system protection. The incoming input signal is given to Potential Transformer (PT) and Current Transformer (CT) to step down the voltage and current separately depending on the settings. The signal conditioning circuit is used to manipulate the analog signal in such a way that it meets the requirement of next stage. Refining of signal is done by using Low Pass Filter (LPF). LPF is a filter that passes low frequency signals with frequencies lower than the cut-off frequency. This ssures removal of DC components. This output is iven to Analog to Digital Converter (ADC) for further processing.

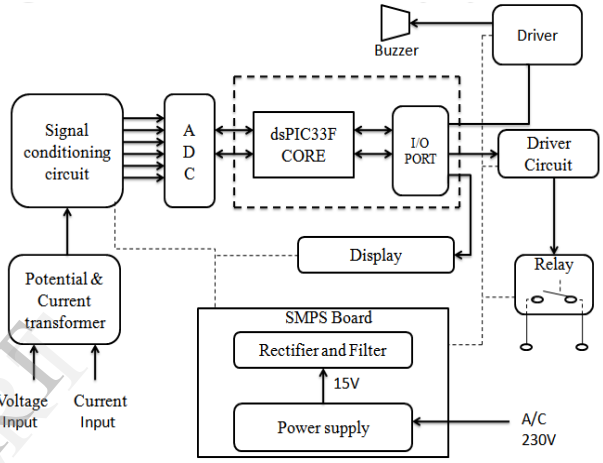

Fig.7. Block diagram of Digital Power system protection

A. *Analog to Digital Converter-AD73360*

Most of the practical signals are analog signals. If DSP has to deal with these analog signals then there is ecessary to convert the analog signal to digital form. ig. 8 shows the process of converting the analog signal to digital signal by sampling and quantization. Sampling is a process of converting the continuous time signal to a discrete time signal at defined sampling interval T. The amplitudes of discrete time signal are then quantized into digital values based on the given word length N [5].

The sampling period, T, is determined by the frequency contents of the input signal according to Nyquist Shannon sampling theorem. It states that the sampling frequency fs should be at least 2 times greater than maximum frequency f_{Max} of the incoming signal].

i.e., $f_s \geq 2f_{Max}$

If the sampling theorem is violated, then aliasing phenomena may occur.

The AD73360 is having six channel 16-bit analog to digital conversion channels. The AD73360 is

particularly suitable for industrial power metering as each channel samples synchronously, ensuring that there is no (phase) delay between the conversions. An on-chip reference voltage is included and is programmable to accommodate either 3.3 V or 5 V operations [8]. A serial port (SPORT) allows easy interfacing of single or cascaded devices to industry standard DSP engines. The SPORT transfer rate is programmable to allow interfacing to both fast and slow DSP engines. The minimum sample rate of AD73360 is 64 k Samples/second [8]. It is having more flexible sample rate using programmable approach.

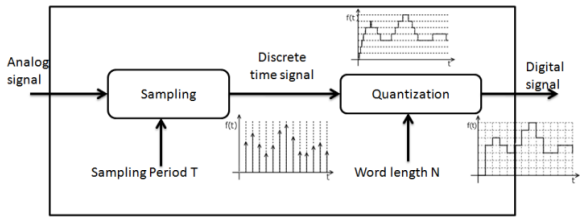

Fig.8. The process of analog-to-digital conversion [4]

B. DSPIC33FJ256GP710 Microcontroller

The dsPIC33FJ256GP710 is having modified Harvard architecture and this is General Purpose Family of device with a 100 pin counts, program memory size of 256 Kbytes and RAM sizes of 30 Kbytes. This family of devices is suitable for a wide variety of high-performance digital signal control applications. This device family employs a powerful 16-bit architecture that seamlessly integrates the control features of a Microcontroller Unit (MCU) with the computational capabilities of a Digital Signal Processor. The resulting functionality is ideal for applications that rely on high-speed, repetitive computations, as well as control [9]. It is having special features like optimized C compiler instruction set, 16-bit wide data path, 24-bit wide instructions and 85 digital I/O pins. It is manufactured using CMOS flash technology so that there is increase in speed of operation and power consumption also reduced [9].

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit Arithmetic Logic Unit (ALU), two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value, up to 16 bits right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The Multiply and Accumulate Control (MAC) instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM memory data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space [9].

C. Algorithm

This section presents the method for computing the magnitude [3]. Basically, the computational problem for DFT is to compute the sequence {X(k)} of N complex valued numbers given of input data sequence {x(n)} of length N, according to the formula

$$X(k) = \sum_{k=0}^{N-1} x(n) e^{-j\frac{2\pi nk}{N}} \quad \ldots\ldots. (1)$$

i. *Direct Computation of the DFT*

For a complex-valued sequence x(n) of N points, the DFT may be expressed as

$$X_R(k) = \frac{2}{N}\sum_{n=0}^{N-1}\left[x(n)cos\left(\frac{2\pi kn}{N}\right)\right] \quad \ldots\ldots (2)$$

$$X_I(k) = \frac{2}{N}\sum_{n=0}^{N-1}\left[x(n)sin\left(\frac{2\pi kn}{N}\right)\right] \quad \ldots\ldots (3)$$

The direct computation of $X_R(k)$and $X_I(k)$ requires:

- $2N^2$ evaluations of the trigonometric functions.
- $4N^2$ real multiplications.
- 4N (N-1) real additions.
- A number of indexing and addressing operations [5].

To calculate resistance and reactance, full cycle direct computation of DFT algorithm has been used. Even though it is very widely accepted algorithm, to extract the magnitude of the incoming signal the processor takes more time because it takes more number of multiplications. Due to this the computation time increases.

ii. Radix-2 FFT Algorithm

One of the most appealing aspects of the DFT is the existence of an efficient procedure for calculating it. The algorithm for fast DFT is known as the FFT. The FFT is a highly elegant and efficient algorithm, which is still one of the most used.

FFT takes advantage of symmetry properties of the complex roots of unity (the W_N, Twiddle factor) and uses repeated clever partitioning of the input sequence into two equally long subsequences, each of which can be separately (and quickly) processed. In order to take full advantage of the repetitive partitioning into equal two parts, the original sequence needs to be of length or periodicity which is a power of 2. If it is not originally so, it is padded with 0s.

The FFT works by taking an N-point input data array and dividing it into halves recursively until the 2-point data pairs are left. These 2-point pairs are then combined to create the 4-point results, and the 4-point pairs are combined to create the 8-point results, and so forth. As a result, N must be a power of 2 (2, 4, 8, 16, 32, 64, etc.) [10].

The 2-point combination is the basic building block of the FFT. This algorithm is repeated for each proceeding stage. The 2-point "butterfly" is calculated as shown in Fig.9 [5].

The W shown in the diagram is "twiddle factor". The twiddle factor is a sine/cosine factor calculated based on the number of points in the current stage [10]. The equation for the twiddle factor is as follows:

$$W_N^m = e^{-j\frac{2\pi m}{N}} = cos\left(\frac{2\pi m}{N}\right) - sin\left(\frac{2\pi m}{N}\right) \quad \ldots\ldots\ldots (4)$$

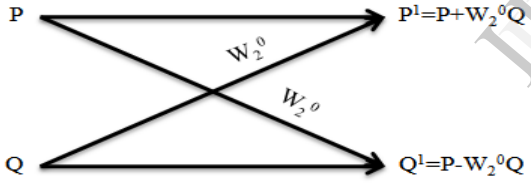

Fig.9.2-Points FFT Butterfly Structure

Fig.10 shows the algorithm for FFT implementation in dsPIC33F microcontroller. ADC output is passed through digital filter to remove the decaying DC component present in the signal. Finding X[32] DFT is sufficient to extract the magnitude so that FFT uses the minimum number of instruction cycle.

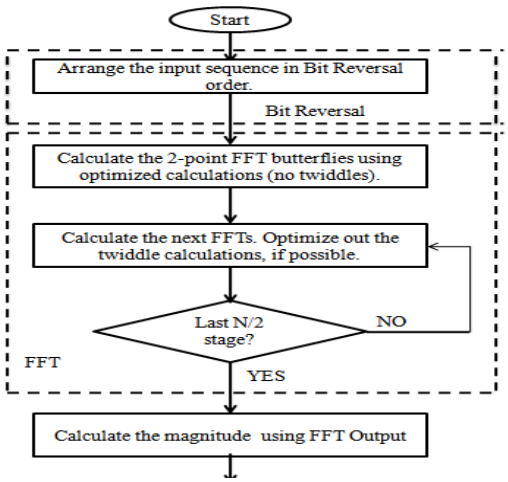

Fig.10. FFT algorithm Flowchart

D. Comparison of DFT and FFT Technique

The main drawback of DFT algorithm is that the extraction of real and imaginary components involves more number of multiplication operations, which makes its implementation on microprocessor a time consuming algorithm. It takes 2048 complex multiplication to find the 32-point full cycle DFT. i.e. each point takes 64 complex multiplications to find the single point DFT in 32 samples of data. It needs to calculate the 32-point full cycle DFT to extract the magnitude of the incoming signal and also it won't eliminate decaying DC present in a signal. The decaying dc causes the large variations in resistance and reactance measurements. Hence there can be a possibility for maloperation of conventional relays at boundaries, as some points lay inside the relay characteristic and some points lay outside the relay characteristic. So before giving signal to DFT computation we need to pass the signal through digital filters.

TABLE I
COMPARISON OF DFT AND FFT TECHNIQUE

Algorithm for extracting Magnitude	N	Number of complex multiplication
DFT	*32*	*2048 ($2N^2$)*
FFT (radix-2)	*32*	*80 ($(N/2)*log_2N$)*

Implementation of FFT approach gives a good solution to overcome the computation speed using less number of multiplication operations to extract real and imaginary components of the signal. Radix-2 FFT is efficient to eliminate the constant dc without passing through digital filter.

This FFT technique is having advantage of finding single point DFT of 32 point DIT-FFT is sufficient to find magnitude of the incoming signal in a more efficient way. 38 real multiplications are sufficient to

find the magnitude instead of 2048 multiplications taken by full cycle DFT so computation speed of algorithm has been increased.

The DSPIC33FJ256GP710 digital signal controller operates at 40MHz frequency and it takes 51.2µS of time to calculate 32-point DFT by using the direct computation of the DFT but FFT takes only 2µS of time to calculate 32-point FFT.

E. Distance Relay Implementation using mho Characteristic

Distance relay is an important unit in the transmission line protection. These relays are widely used for primary and backup protection of transmission lines where high-speed relaying is required. Distance relay use voltage and current input to provide an output signal if a fault is within a predetermined distance from the relay location. Distance to the fault is calculated from the voltage-to-current ratio as a measure of impedance [11]. The major advantage of a distance relay is that it responds to system impedance instead of the magnitude of current or voltage separately.

Fig. 11 shows the ideal Distance relay with mho characteristic which can be graphically represented in terms of three variables R, X (or Z) and RCA, where R is the resistance, X is the reactance, Z is the impedance and RCA is relay characteristic angle [11].

The resistance and reactance are from equations (6) and (7) respectively. These values are used to check whether the impedance point lies inside or outside the circle using equation (8). If impedance point lies inside the circle then relay trips. Impedance is calculated using:

$$Z = R+jX \quad \ldots\ldots (5)$$

where,

$$R = \frac{(V_r \times I_r) + (V_i \times I_i)}{I_r{}^2 + I_i{}^2} \quad \ldots\ldots (6)$$

$$X = \frac{(V_i \times I_r) - (V_r \times I_i)}{I_r{}^2 + I_i{}^2} \quad \ldots\ldots (7)$$

Where V_r, V_i, I_r and I_i are real and imaginary components of voltage and current respectively.

$$\sqrt{(R-a)^2 + (X-b)^2} \leq Z_{set} \quad \ldots\ldots (8)$$

where,

(a , b) = center of the circle in Ω
Z_{set} = set impedance value in Ω (radius of the circle)

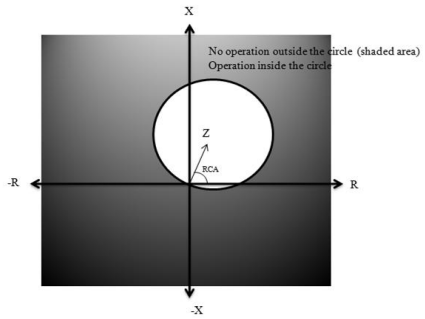

Fig.11. R-X diagram for the generic impedance relay

VI. Results of Distance Relay

For twin moose conductor resistance and reactance per km are mentioned in section III. To set the mho characteristic for 80% of line length, the parameters required are center of the circle: (R , X) = (0.008644pu , 0.02375pu), radius of the circle = 0.025pu and RCA = 70^0. The center of the circle on impedance line is chosen such that circle passes through the origin of R-X plane. The impedance for 80% of the line is 0.05pu.

Typical results for the case of A-G fault are presented in the form of impedance plots. Fig. 12 and Fig. 13 show the impedance plot for a fault at 60% and 90% of the line. To demonstrate, reach setting is set for 80% of the line length. From the results obtained, it has been found that for fault at 60% of the transmission line the impedance of the relay enters into the reach settings indicated in Fig.12 and for fault at 90% of the transmission line the impedance out of the reach setting as shown in Fig.13.

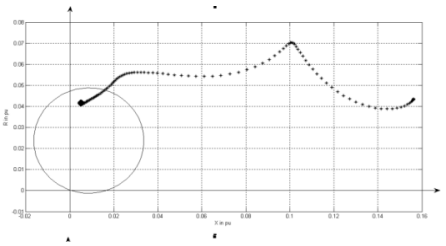

Fig.12. Impedance plot for fault at 60% of line length

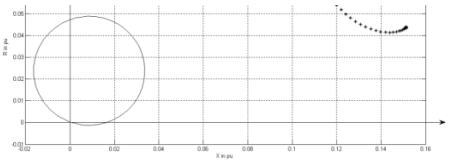

Fig.13. Impedance plot for fault at 90% of line length

The steady state results of relay are observed when the inputs are given to relay through numerical test kit. The setting parameters for 80% of line length are center of the circle: (R , X) = (13.83Ω , 38Ω), radius of the circle = 40.43Ω and RCA = 70^0. Table II shows the implementation results by changing the phase angle

between voltage and current from 0° to 360° in steps of 10° by keeping magnitude of current constant and by reducing voltage. The results observed from the relay are matched with the calculated values.

TABLE II
STEADY STATE IMPEDANCE VALUES
(Phase angle varying from 0^0 to 360^0 in steps of 10^0)

Phase angle	$R_{calculated}$	$R_{observed}$	$X_{calculated}$	$X_{observed}$
0^0	27.5	27.52	0	0
10^0	41	41.01	8	8.01
20^0	49.5	49.52	19	19.01
30^0	53.5	53.51	32.5	32.52
40^0	53	53.01	45.5	45.5
50^0	47.5	47.51	59	59.02
60^0	39	39.01	63.5	63.51
70^0	27.5	27.51	75	75.01
80^0	13	13.01	62.5	62.51
90^0	0	0	75	75.01
100^0	-12.5	-12.52	67.5	67.51
110^0	-21	-21.01	57	57.01
120^0	-25.5	-25.51	43.5	43.52
130^0	-25	-25.01	30	30.02
140^0	-19.5	-19.51	15.5	15.52
150^0	-12.5	-12.51	7.5	7.51
160^0	-2.5	-2.51	1	1.02
170^0 to 340^0	No Trip	-	-	-
350^0	12.5	12.51	-2.5	-2.52

VII. CONCLUSION

The distance relay algorithm using advanced DSP technique is implemented using a dsPIC33F microcontroller. This protection system has encouraged the design and development of microcontroller based protective relays. These relays are compact, reliable, and flexible over conventional relays. The relay algorithm computation speed is increased and also it is not compromised with the accuracy. This relay also provides improved performance, user friendly human interface, self-checking and self-calibration functions.

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