Implementation of Arithmetic Computation using Vedic Algorithm

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***Abstract*— The cubing and squaring computations have very high delay and power consumption in conventional methods. Vedic formula offers the algebraic problem solution techniques analogous to mental calculations to generate fast answer. Vedic maths provides methods with simple strategies that help us achieve low power consumption and less delay. Also in this method, the number of partial products is being reduced thereby reducing the memory. Vedic multiplier is implemented in vedic cubic formula- Yavadunam sutra to reduce the complexities in multiplication. Further, Carry Select Adder is used for vedic multiplier using Urdhva- Tiryakbhyam formula to implement the multiplier in cubing operation. The propose method is implemented using Xilinx ISE 14.7.**

Keywords – Yavadunam sutra, Urdhva Tiryabhyam, Vedic mathematics, Carry Select Adder (CSLA), Vedic multiplier

I. INTRODUCTION

MULTIPLICATION is the major operation in all signal processors, that occupies area and delay.

The operation also requires lots partial products to be stored. Multiplication operation affects delay to greater extent. More particularly, cubing operations affect the performance of the professor. Cubing operation requires large memory space for storage of partial products. E.g., If an n bit number is squared (n*n) then the output of the squaring operation would be of 2n bits. If we need to cube the number (2n*n), then we need a multiplier of 2n size because of varying size [1]. The result is of 3n bits. It becomes a disadvantage if we use same multiplier for cubing operation. So we need a dedicated unit for cubing operation so that area and delay can be minimized [4- 6]. There are various methods so far available for the cubing operation. But, vedic formulae have various techniques that uses fastest algorithms to implement cubing operations [6,8]. One of the formulae for implementing cubic architecture is Yavadunam formula (whatever the extent of its deficiency) [1]. This formula implements cubing operation without performing cubing operation. This formula has multiplication operation. For multiplying, the proposed method uses carry select adder with vedic multiplier using Urdhva-Tiryakbhyam (Vertically and crosswise) technique [2,3]. This is the basic Vedic algorithm for multiplication. Here, we are implementing cubic operations with the Yavadunam sutra and multiplier with Urdhva-Tiryakbhyam and carry select adder (CSLA) [2,9].

II. VEDIC MATHEMATICS

Vedic maths is an ancient form of mathematics. The word “vedic” is derived from the word “veda” which means “store house of knowledge” [7]. Vedic maths has about 16 sutras and various sub-sutras. Vedic maths reduces time delay and increases the efficiency [3]. The various features of Vedic maths are coherency, flexibility, integrity, memory, Efficiency and Speed.

A. Yavadunam (YVDN) Sutra

It is literally defined as “whatever the extent of its deficiency”. Algorithm for calculation of cubes using YVDN formula is described below [1].

Table 1 – Cube calculation steps

Number is close to the BO	**Number is not close to the BO**
Here consider BO=1000. Subtract 993 from 1000,result is 7	Here considered BO=500. Subtract 500 from 521,result is 21
Calculate 1st term, cube of 7 i.e.7^3=343	Calculate 1st term ,cube of 21=9261
Compute the 2nd term, $3*7^2$=147. Since BO =10^3,here power=3,so 147 is left shifted by 3 positions	Calculate the 2nd term,$3*5*21^2$=6615, Since BO = 500($5*10^2$), here power=2,so 6615 is laft shifted by 2 positions
Calculate the 3rd term by subtracting 2*7 from the actual number ,i.e.(993-14)=979 and shifting by power*2=3*2=6 positions left	Calculate the 3rd term by adding 2*21 to actual number, i.e.(521+2*21=563)then multiply it with $5^{power}=5^2$ i.e.$563*5^2$=14075 and shifting by power*2=2*2=4 positions left
Finally result=3rd term+2nd term-1st term (‘-‘since actual number993 was subtracted from BO)i.e. the result is equal to 979146657	Finally result =3rd term +2nd term +1st term (‘+’since BO was subtracted from actual number) i.e., the result is equal to 141420761

The following flow chart expresses the algorithm for implementation of cubic structure using YVDN formula in Vedic maths. [1]

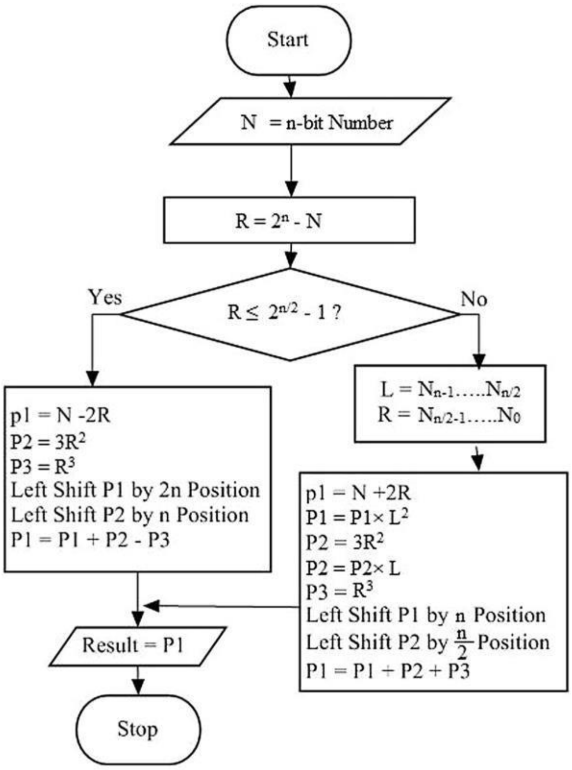


Fig. 1. Flow Chart for YVDN sutra

The following are the examples performed with binary numbers and output is obtained without doing squaring operation.

$993^3=979146657$

$(979146657)_{10}=(111010010111001001011110100001)_2$

$R=2^{10}-993=1024-993=31$

$31<=2^5-1$; True

$P1=993-2*31=(931)_{10}=(1110100011)_2$

$P2=3*31^2=(2883)_{10}=(101101000011)_2$

$P3=31^3=(29791)_{10}=(111010001011111)_2$

P1	1110100011	(+)
P2	101101000011	
	111010010111010000110000000000	(-)
P3	111010001011111	
	111010010111001001011110100001	

(a)

$521^3=141420761$; $(521)_{10}=(1000001001)_2$

$(141420761)_{10}=(1000011011011110100011011001)_2$

$R=2^{10}-521=503$

$503<=31$

$L=(10000)_2=(16)_{10}$; $R=(01001)_2=(9)_{10}$

$P1=521+2*9=137984=(100001101100000000)_2$

$P2=243*16^2=(3888)_{10}=(111100110000)_2$

$P3=9^3=(729)_{10}=(1011011001)_2$

P1	100001101100000000
P2	111100110000
P3	1011011001
	1000011011011110100011011001

(b)

Fig. 2. YVDN sutra (a) Base of Operation (BO) near the number (BO=1000), (b) Base of Operation (BO) far away from the number (BO=500)

B. Urdhva-Tiryakbhyam

It literally means "vertically and crosswise". It is a high speed technique widely used for multiplication. It has less complexity and requires less hardware compared to other multipliers [2].

Example for Vedic multiplication using the numbers 234 and 356 is expressed below.

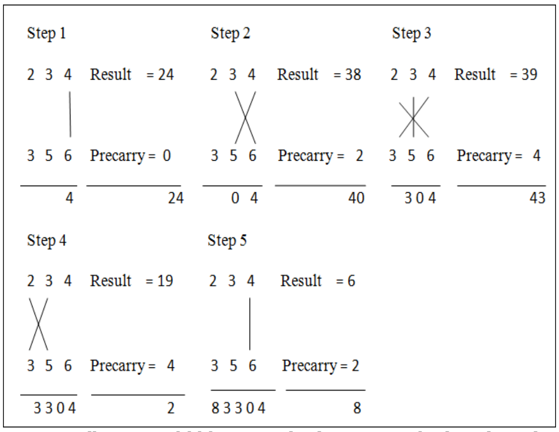


Fig. 3. Urdhva-Tiryakbhyam multiplication method explained with the numbers 234 and 356

III. VEDIC MULTIPLIER

Carry Select Adder (CSLA) is used along with Ripple Carry Adder (RCA) and d_latch in Vedic multiplier in order to achieve less delay. Vedic multiplier with carry select adder is implemented for multiplication processes required in the proposed cubic method. The following block diagram shows the implementation of Vedic multiplier with carry select adder. [2]

IV. ARCHITECTURE

The proposed method implements cubic computation with YVDN sutra. For multipliers, Vedic multiplier with CSLA is used that improves the overall performance of the circuitry.

A. Cubic Architecture

The implementation of the proposed architecture is done with the Vedic multiplier that reduces area, power consumption and propagation delay. It is implemented with YVDN formula and the required simple adders and subtractors whenever required. For computing the values of 2^{n-1} and $2^{n/2-1}$, shifting operation is used which further improves the performance.

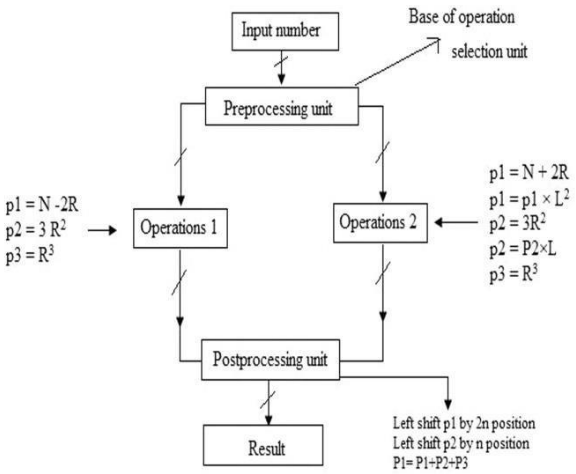


Fig. 4. Architecture for cubic computation with YVDN sutra

B. Vedic multiplier using CSLA Architecture

The Vedic multiplier uses carry select adder with d-latch which is more efficient than the conventional CSLA. It reduces the number of ripple carry adders that are reduced.

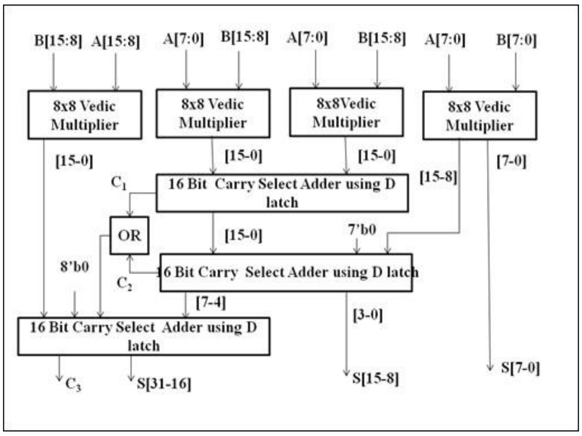
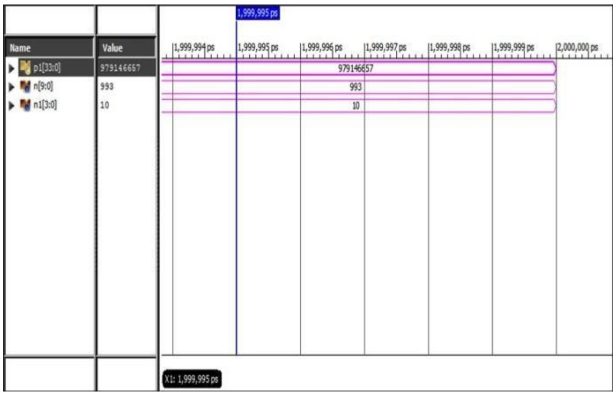


Fig. 5. 16X16 Vedic multiplier with carry select adder and d-latch

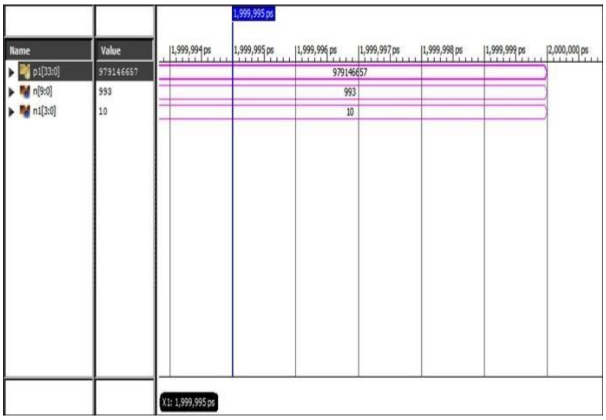
V. SIMULATION RESULTS

The following are the simulation results separately for the numbers 993 and 521 that are discussed as examples. The simulation results are obtained with YVDN formula for obtaining the cube of the number along with Vedic multiplier and Carry Select Adder (CSLA).

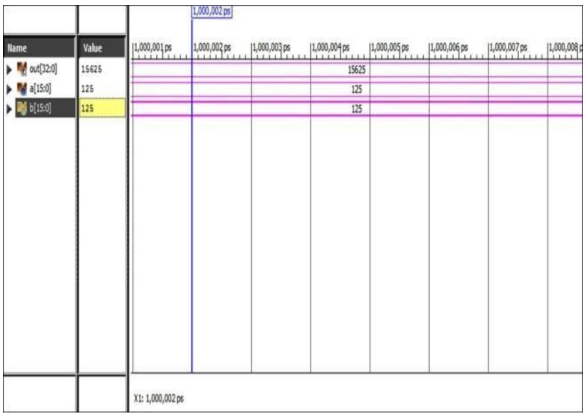
A. Cubic Architecture with number close to the BO



B. Cubic Architecture with number not close to the BO



C. 16X16 Vedic Multiplier with CSLA and d-latch



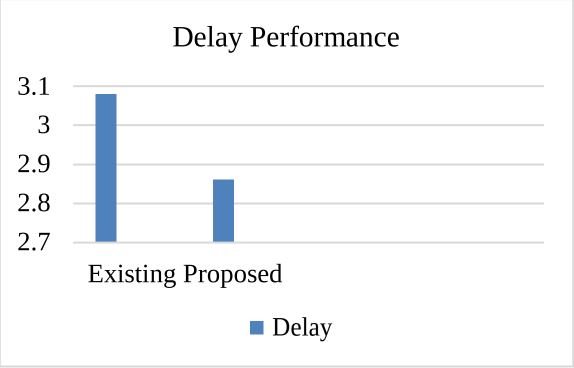
VI. RESULTS AND DISCUSSION

The implementation of the proposed algorithm was done using Xilinx 14.2, 32-bit project navigator. The comparison of performance parameters such as delay and power consumption of the proposed and existing method is tabulated as follows

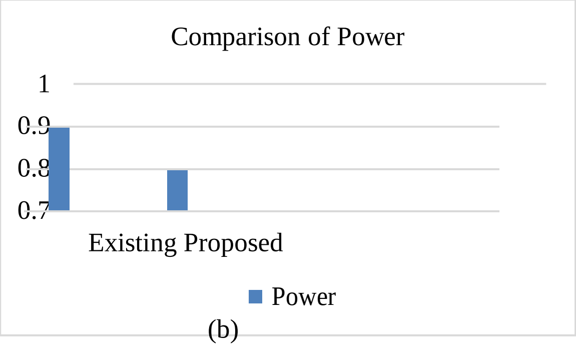
Table. 2 Performance Comparison of existing cubic architecture

S.No	Module	Power(mW)	Delay (ns)
1.	Existing	0.9	3.08
2.	Proposed	0.8	2.86

The comparison of proposed cubic implementation with that of the existing is expressed in terms of bar chart as follows.



(a)



(b)

Fig. 6. Comparison of existing and proposed methods in terms of (a) delay and (b) power consumption

The power consumption has been improved up to 12.5% and the performance in delay has been improved up to 7.41%. This explains the worst case scenario of cubic operation i.e., in case of 8X8X8 n- bit operation. This indicates the decreased delay and reduction in power consumption in the proposed cubic method with vedic multiplier using carry select adder.

VII. CONCLUSION

High speed and less power consumption have been achieved with the proposed method. The generation of partial products, requirement of multipliers with different size and high memory requirement that occur in conventional cubic calculation has been avoided and also vedic multiplier with carry select adder further improves the performance. Thus, the increase in performance of 12.5% and 7.41% in terms of delay and power consumption has been achieved.

REFERENCES

1. Deepak Kumar, PrabirSaha, AnupDandapat, "*Vedic Algorithm for cubic computation and VLSI implementation*", Engineering Science and Technology, an International Journal 20, pp. 1494–1499, 2017
2. C. Durga devi, Renuga Devi M, Sathyasree C and Chitra R, "*Design of High Speed Vedic Multiplier using Carry Select Adder*", National Confernce on Innovations in Electronics, Communication and Computing (NCIECC' 17), pp. 196-202, 2017
3. Anjana.R, Abishna.B, Harshitha. M.S, Abhishek.E, Ravichandra.V, "*Implementation of Vedic multiplier using Kogge-Stone Adder*", International Conference on Embedded Systems (ICES), pp. 28-31, 2014
4. Parepalli Ramanamma, "*Low power Square and Cube Architectures using Vedic Sutra*", International Journal of Engineering Research and General Science Volume 5, Issue 3, pp. 241-248, 2017
5. A. Deshpande, J. Draper,"*Comparing squaring and cubing units with multipliers*", 55th Int. Midwest Symp. on Circuits and Systems (MWSCAS),Boise, ID, pp. 466– 469, 2012
6. Gajji Lavanya, Ch. Venkateswara Rao, Rajaiah Gabbeta, "*Low power Square and Cube Architectures using Vedic Sutras*", International journals of innovative Technologies, IISN 2321-8665 ,Volume 4, issue 14, pp. 2603-2606,2016
7. Chinchu R, Nishi G, Nampooothiri, "*Time Efficient Square and Cube Architecture using Vedic Sutras*", International Journals of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Volume 4,Issue 11, pp.9202-9209,2015
8. C. Suneetha , C. Aruna Bala , "*Low Power Vedic Sutras for an Advanced Square and Cube Architectures*", International Journal and Magazine of Engineering and Technology, Volume 2, Issue 12, pp.1913- 1918,2015
9. Charishma V, Ganeshkumar G, "*Design of High Speed Vedic Multiplier using Vedic Multiplication Techniques*", International Journals of Scientific and Research Publication, Volume 2, Issue 3, pp.1-5
10. Vidhyashakari P, Lokesha B, "Design *and Implementation of Square and Cube Architectures using Vedic Sutras on FPGA*", International Journals of Emerging Technology in Computer Science & Electronics (IJETCSE) , Volume 4, Issue 2, pp.377-381