# Implementation of an Efficient Adaptive Feedback Equalization for Tunable Subthreshold Logic Circuits

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*Abstract*-An Efficient tunable subthreshold logic circuit designed by using adaptive feedback equalization circuit. This circuit used in a sequential digital logic circuit to mitigate the process variation effects and reduce the dominant leakage energy component in the subthreshold region. Feedback equalizer circuit adjusts the switching threshold of its inverter. It is based on the output of the flip-flop in the previous cycle to reduce the charging and discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Also present detailed energy-performance models of the adaptive feedback equalizer circuit. Proposed approach can reduce the normalized variation of the critical path delay while reducing the energy product at minimum energy supply voltage. This design will be implemented in the three tap FIR filter and provide the efficient power reduction. The adaptive equalization circuits are design by Verilog HDL and simulated by Modelsim. Area and power will synthesized by Xilinx tool.

*Index Terms*—Feedback equalizer, leakage energy component, subthreshold, maser-slave positive edge-triggered flip-flop

## I. INTRODUCTION

The use of sub threshold digital CMOS logic circuits is becoming increasingly popular in energy-constrained applications where high performance is not required. The main idea here is that scaling down the supply voltage can significantly reduces the dynamic energy consumed by digital circuits. Scaling the supply voltage also lowers down the leakage current due to reduction in the drain-induced barrier lowering (DIBL) effect. However, as the supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases, which in turn increases the leakage energy of the transistors. These two opposite trends in the leakage and the dynamic energy components lead to a minimum energy supply voltage that occurs below

the threshold voltage of the transistors for digital logic circuits. However, digital logic circuits operating in the sub threshold region suffer from process variations that directly affect the threshold voltage. This in turn has a significant impact on the drive current due to the exponential relationship between the drive current and the threshold voltage of the transistors in the sub threshold regime.

Moreover, sub threshold digital circuits suffer from the degraded $I$ON/$I$OFF ratios resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. These degraded $I$ON/$I$OFF ratios and process-related variations make sub threshold circuits highly susceptible to timing errors that can further lead to complete system failures. Since the standard deviation of $VT$ varies inversely with the square root of the channel area one approach to overcome the process variation is to upsize the transistors alternately, one can increase the logic path depth to leverage the statistical averaging of the delay across gates to overcome process variations. These approaches, however, increase the transistor parasitic, which in turn increases the energy consumption.

In this paper, we first propose the use of a feedback equalizer circuit for lowering the energy consumption of digital logic operating in the sub threshold region while achieving robustness equivalent to that provided Here, the feedback equalizer circuit (placed just before the flip-flop) adjusts the switching threshold of its inverter based on the output of the flip-flop in the previous cycle to reduce the charging/discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic, which makes it more robust to

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timing errors and allows aggressive clocking to reduce the dominant leakage energy. In addition to reducing energy consumption, we also demonstrate how the tuning capability of the equalizer can be used to enable extra charging/discharging paths for the flip-flop input capacitance after fabrication to mitigate timing errors resulting from worse than expected process variations in the sub threshold digital logic.

In general, our approach of using feedback equalizer to lower energy consumption and improve robustness is independent of the methodology used for designing a combinational logic block operating in the sub threshold regime. We propose using an adaptive feedback equalizer circuit in the design of tunable sub threshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve performance of the sub threshold digital logic circuits. At the same time, the tunability of this feedback equalizer circuit enables post fabrication tuning of the digital logic block to overcome worse than expected process variations as well as lower energy and improve performance. expected process variations, we show that the tuning capability of the equalizer circuit can be used post fabrication to reduce the normalized variation ($3\sigma/\mu$) of the critical path delay with minimal increase in energy.

## II.ADAPTIVE EQUALIZER CIRCUIT OF ADAPTIVE EQUALIZATION WITH MULTIPLE FEEDBACK (AEMF)

Several techniques have been used to design robust ultralow power sub threshold circuits. Transistor upsizing and increasing the logic path depth can be used to overcome process variations. The use of gates of different drive strengths has also been proposed to overcome process variations. This method based on the two feedback path used to reduce the power and area of the circuits. In Existing system propose using joint equalization and coding to improve on-chip communication speeds by signaling at rates beyond the rate governed by resistance–capacitance (RC) delay in interconnects.

Operating beyond the RC limit introduces inter-symbol interference (ISI). We mitigate the effects of ISI by employing equalization. The existing equalizer employs a variable threshold inverter whose switching threshold is modified as a function of past output of the bus. In fig.1 the Adaptive feedback equalizer circuit has the two different feedback path in sub threshold regime shows the adaptive feedback equalizer with variable threshold invertors. The use of variable threshold inverter using adaptive feedback equalizer along with the classic master–slave positive edge-triggered flip-flop to design an adaptive E-flip-flop. This adaptive feedback equalizer circuit consists

of two feed forward transistors (M1 and M2)and four control transistors (M3 and M4 for feedback path 1 that is always ON and M5 and M6 for feedback path 2 that can be conditionally switched ON post fabrication that provide extra pull-up/pull-down paths in addition to the pull-up/pull-down path in the static inverter for the Data Flip- Flop input capacitance. The extra pull-up/pull-down paths are enabled whenever the output of the critical path in the combinational logic changes. The control transistors M5 and M6 are enable /disable through transistor switches (M7 and M8) that are controlled by an asynchronous control latch. The value of the static control latch is initially reset to 0 during chip boot up.
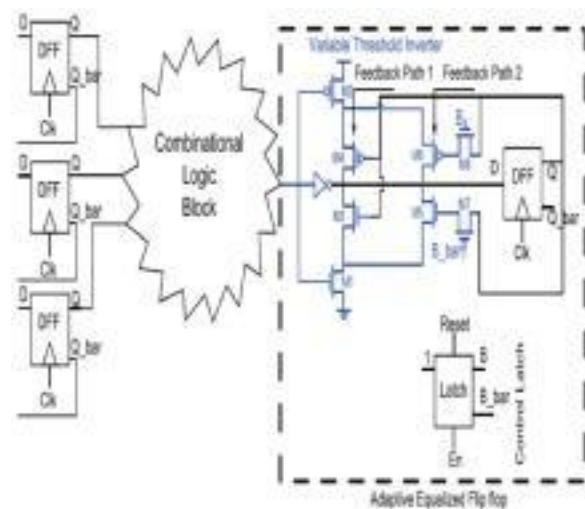


Figure: 1.Adaptive feedback equalizer circuit with multiple feedback paths (designed using variable threshold invertors)

After boot up, if required a square pulse is sent tithe En terminal to set the output of the latch to 1 to switch ONM7 and M8, which enables feedback path 2.The adaptive E-flip-flop effectively modifies the switching threshold of the static inverter in the feedback equalizer based on the output of flip-flop in the previous cycle. The previous output of the flip-flop is a 0; the switching threshold of the static inverter is lowered, which speeds up the transition of the flip-flop input from 0 to 1.

Similarly if the previous output is 1, the switching threshold is increased, which speeds up the transition to 0.Effectively, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions of the flip-flop input. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic. Thad

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response of the adaptive feedback equalizer circuit with two different feedback paths in the sub threshold regime is shown in Fig.2
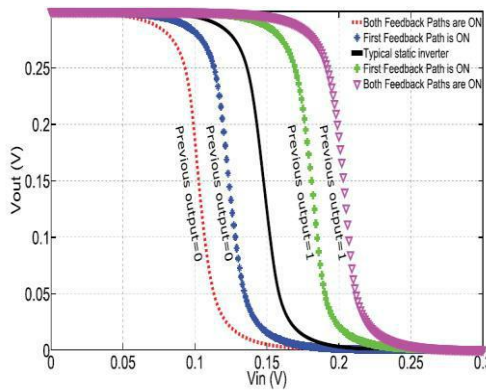


Figure: 2.DC response of the adaptive feedback equalizer circuit with two different feedback paths in the sub threshold regime. The switching threshold of the inverter is modified based on the previous sampled output

### A. CONVENTIONAL MASER-SLAVE POSITIVE EDGE-TRIGGERED FLIP-FLOP

Master Slave flip flop are the cascaded combination of two flip-flops among its inversion i.e. if the master is positive edge-triggered, then the slave is negative-edge triggered and vice-versa. This means that the data enters into the flip-flop at leading/trailing edge of the clock pulse while it is obtained at the output pins during trailing/leading edge of the clock pulse. Hence a master-slave flip-flop completes its operation only after the appearance of one full clock pulse for which they are also known as pulse-triggered flip-flops. Which the first is designated as master flip-flop while the next is called slave flip-flop. Here the master flip-flop is triggered by the external clock pulse.
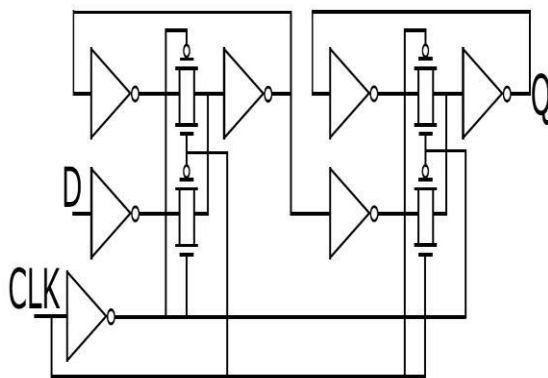


Figure: 3.Circuit diagram of conventional maser-slave positive edge-triggered flip-flop

A positive-edge triggered master–slave D flip-flop, when the clock signal is low (logical 0) the "enable"

seen by the first or "master" D latch (the inverted clock signal) is high (logical 1). This allows the "master" latch to store the input value when the clock signal transitions from low to high. As the clock signal goes high (0 to 1) the inverted "enable" of the first latch goes low (1 to 0) and the value seen at the input to the master latch is "locked". Nearly simultaneously, the twice inverted "enable" of the second or "slave" D latch transitions from low to high (0 to 1) with the clock signal. This allows the signal captured at the rising edge of the clock by the now "locked" master latch to pass through the "slave" latch. When the clock signal returns to low (1 to 0), the output of the "slave" latch is "locked", and the value seen at the last rising edge of the clock is held while the "master" latch begins to accept new values in preparation for the next rising clock edge. This conventional master slave positive edge triggered flip flop which has the more transistor. So that area is increased. Total parasitic capacitance is increased. To avoid this problem adaptive feedback equalizes with multiple feedback paths are used. And also this system has some practical issues such as large power consumption, more area usage. Complex layout.

### III. ADAPTIVE EQUALIZATION WITH SINGE FEEDBACK PATH

Adaptive feedback equalization with single feedback path consists of the whole circuits has data flip flop, variable threshold inverter and combinational logic. This proposed method has designed with original nonqualified design; equalized design with one feed back ON buffer inserted no equalized design. Figure 4 shows the block diagram of three tap FIR filter
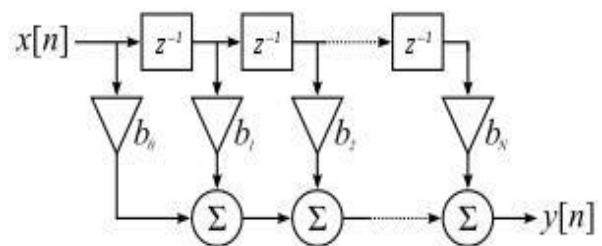


Figure: 4.Block diagram of three tap FIR filter.
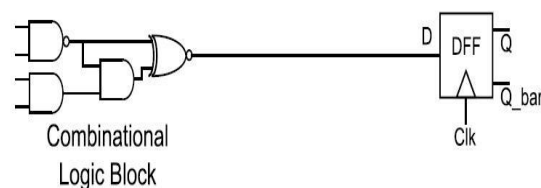
### A. ORIGINAL NON EQUALIZED DESIGN



Figure: 5 Original non equalized designs

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Fig: 5.show the original non equalized design and it has no feedback from output to the input. The combinational logic performed the operations and output will pass through the Flip flop and d flip flop execute the output of And Bar. It provides the some delay in the output.
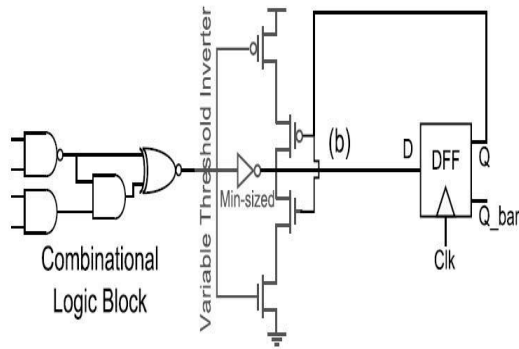
*B. EQUALIZED DESIGN WITH ONE FEEDBACK PATH ON*



Figure: 6 Equalized design with one feedback path on
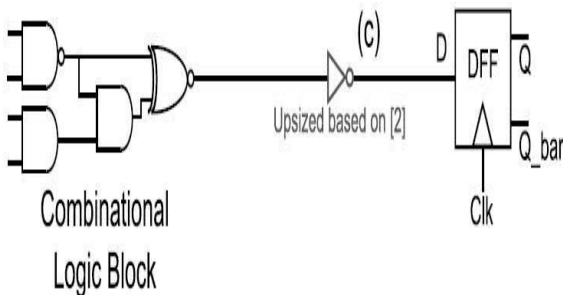
*C.BUFFER-INSERTED NO EQUALIZED DESIGN:*



Figure: 7.Buffer-inserted no equalized design

*D. AESF IMPLEMENTED IN THREE TAP 16 BIT FIR FILTER*

Propose the three tap 16 bit FIR filter which consists of equalized flip flop, 32 bit array multiplier and adder. Here 16 bit inputs are given in to the flip flop. Equalized flip flop is inserted intended with normal d flip flop Registers are designed with 32 bit and 16 bit register. Inputs are feeding to the multiplier. Then it is added with 32 bit adder. Buffer is added between each co efferent. It is used to reduce the harmonics in the output. Finally output will be come with 32 bits. This system has some advantages such as less power consumption, less area usage.
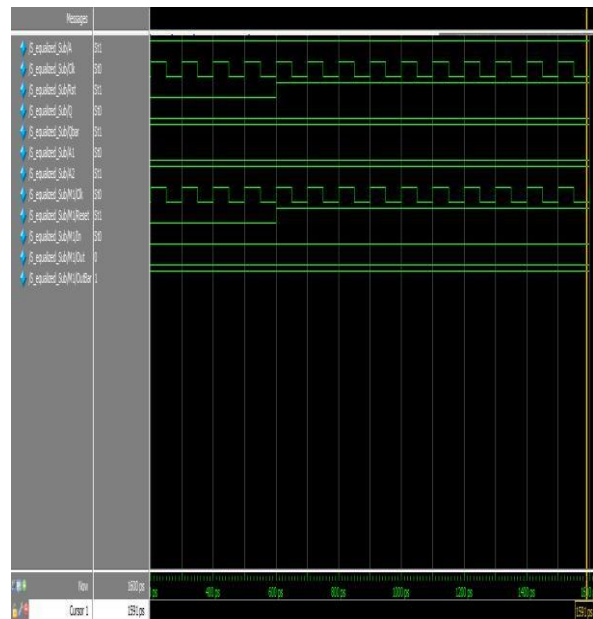
## IV.SIMULATION RESULTS

*A.OUTPUTWAVEFORM OF AESF*



Figure:8 Proposed AESF

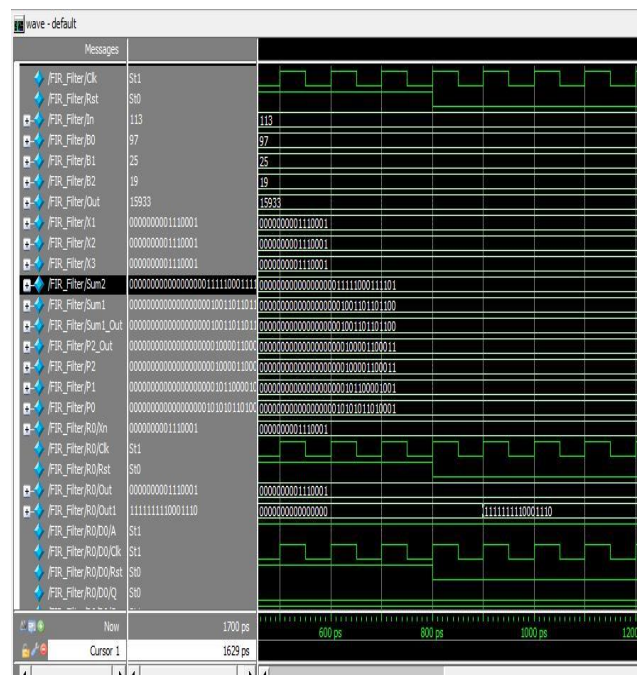*B.OUTPUT WAVEFORM OF AESF IMPLEMENTATION IN FIR FILTER*



Figure: 9. Proposed AESF implemented in three tap 16 bit FIR filter.

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## V. COMPARISION RESULTS

### A. POWER CALCULATION OF AEMF AND AESF

| Method name | Power | | |
|---|---|---|---|
| | *Voltage* | *Current* | *Total Power* |
| Existing method of AEMF | 475mW | 190.00mA | 729mW |
| Proposed method of AESF | 148.44mW | 59.38mA | 391mW |

Table: 1. Power calculations of AEMF and AESF

### B. POWER AND AREA COMPARISIONS OF FIR FILTER

| Method Name | | FIR based on Existing Equalized Flip Flop | FIR based on Proposed Equalized Flip Flop |
|---|---|---|---|
| Area | LUT | 2659 | 2219 |
| | Slices | 2659 | 1237 |
| | Gate | 17350 | 13338 |
| Power | Voltage | 4512.50mW | 3800.00mW |
| | Current | 1805.00mA | 1520.00mA |
| | Total Power | 6269.35mW | 5608.17mW |

Table: 2.Power and Area comparisons of FIR filter

## VI.CONCLUSION

The proposed application of tunable adaptive feedback equalizer circuit used to reduce the normalized variation of total delay along the critical path and the dominant leakage energy of the digital CMOS logic operating in the sub threshold regime. Adjusting the switching thresholds of the gates before the flip-flop based on the gate output in the previous cycle, the adaptive feedback equalizer circuit enables a faster switching of the gate outputs and provides the opportunity to reduce the leakage energy of digital logic in weak inversion region. Tuning capability of the equalizer circuit with single path can be used the power of 560mW and multiple paths used the power of 6269Mw. This design will be Implemented three tap 16 bit FIR filter and power.

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