

Implementation of Adaptive Filter Based on LMS Algorithm

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Abstract: *In Communication channels due to various non-idealities like Inter Symbol Interference (ISI), Additive White Gaussian Noise (AWGN), Non-linear effects etc the input signal suffers from different distortions. In order to neutralize the effect of these distortions introduced by the channel and to be able to recover the original signal as best as possible, we need Channel Equalizer which acts as a Compensator for the Channel distortion, time-varying and can adapt itself to the changes in channel characteristics.*

This paper is VHDL implementation of five tap adaptive filter based on Least mean square (LMS) algorithm with pipelined architecture. So this implementation can work with higher data rates with less clock speed requirements and so with less power consumption. It uses fixed point arithmetic blocks for filtering.

Keywords: *FPGA, Adaptive Filter, Adaptive Algorithm, Least Mean Square Algorithm, FIR Filter, LMS Algorithm.*

I. INTRODUCTION

In digital communication, multi-path distortion channel results in Inter symbol interference (ISI). ISI also brings on higher Bit Error Rate (BER). Accordingly, it is necessary to design a filter to compensate distortion of channel. So to circumvent the channel impairment caused by multi-path fading, more and more receivers resort to adaptive equalizers. An adaptive equalizer is essentially a linear adaptive filter used to model the inverse transfer function of the channel. The algorithm is used to process a speech signal to enhance its signal

to noise ratio (SNR). The adaptive algorithms are classified as stochastic gradient algorithms and exact least Square algorithms. Stochastic gradient algorithms include self orthogonalizing algorithms as a subclass. The conventional least mean square (LMS) algorithm (with sample update), normalized LMS algorithm and block LMS algorithm (with block update) are all stochastic gradient algorithms. Recursive Least Squares (RLS) algorithm is least squares algorithm. Out of these algorithms, LMS and RLS algorithms are popularly used. RLS algorithm has better convergence speed than LMS. But the complexity for hardware implementation is very high LMS algorithm is widely adopted in hardware implementation because of its simplicity and robustness.

Based on this adaptive equalization technique has been widely studied and applied in the field of wireless communication. It is an important means of compensating the distorted channel. Using this technique, an alterable or adjustable system that improves the performance of signal processing via contacting with the outside can be designed and is adaptive. Nowadays, with the ability to operate at high switching frequencies FPGAs (Field Programmable Gate Arrays) have provided an ideal solution for implementing large amounts of high speed signal processing circuitry, allowing the designer to reduce the size and cost of a product. In this project, we describe a pipelined implementation of the LMS adaptive FIR filter.

A. FPGA

FPGAs provide a good combination of high-speed implementation features with the flexibility of a COTS platform. FPGA's have grown over the past

decade to the point where there is now an assortment of adaptive algorithms which can be implemented on a single FPGA device. However, the direct implementation of an adaptive filter on an FPGA often proves to be slow due to the error feedback signal in the recursive structure. Typically, the system throughput rate of many DSP algorithms can be improved by exploiting concurrency in the form of parallelism and pipelining.

II. ADAPTIVE FILTER

In practice, signals of interest often become contaminated by noise or other signals occupying the same band of frequency. When the signal of interest and the noise reside in separate frequency bands, conventional linear filters are able to extract the desired signal. However, when there is spectral overlap between the signal and noise, or the signal or interfering signal's statistics change with time, fixed coefficient filters are in appropriate.

A. ADAPTIVE ALGORITHM

There are numerous methods for the performing weight update of an adaptive filter. There is the Wiener filter, which is the optimum linear filter in the terms of mean squared error, and several algorithms that attempt to approximate it, such as the method of steepest descent. There is also least mean square algorithm, developed by Widrow and Hoff originally for use in artificial neural networks. Finally, there are other techniques such as the recursive least squares algorithm and the Kalman filter. The choice of algorithm is highly dependent on the signals of interest and the operating environment, as well as the convergence time required and computation power available.

III LEAST MEAN SQUARE ALGORITHM

The least-mean-square (LMS) algorithm is similar to the method of Steepest-descent in that it adapts the weights by iteratively approaching the MSE minimum. The LMS algorithm was developed by Widrow and Hoff in 1959. The algorithm uses a gradient descent to estimate a time varying signal. The gradient descent method finds a minimum, if it exists, by taking steps in the direction negative of the gradient. It does so by adjusting the filter coefficients so as to minimize the error. The gradient is the del operator (partial derivative) and is applied to find the divergence of a function, which is the error with respect to the nth coefficient in this case. The LMS algorithm approaches the minimum of a function to

minimize error by taking the negative gradient of the function.

A. FUNCTIONAL IMPLEMENTATION ON A LATTICE FPGA

The LMS reference design has the following two main functional blocks:

- i. FIR Filter
- ii. LMS Algorithm

i. FIR Filter

The FIR filter is implemented serially using a multiplier and an adder with a feedback as shown in the high level schematic in Figure 1. The FIR result is normalized to minimize saturation.

The LMS algorithm iteratively updates the coefficient and feeds it to the FIR filter. The FIR filter then uses this coefficient $c(n)$ along with the input reference signal $x(n)$ to generate the output $y(n)$. The output $y(n)$ is then subtracted from the desired signal $d(n)$ to generate an error, which is used by the LMS algorithm to compute the next set of coefficients.

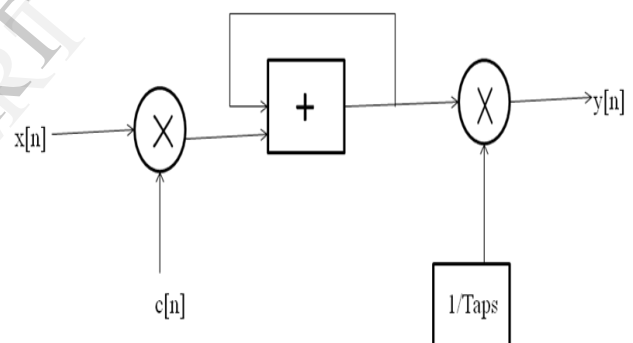


Figure 1 FIR Implementation

ii. LMS Algorithm

The LMS algorithm is implemented as shown in Figure 2. The delay is necessary in the design to separate the current coefficients from the next set of coefficients.

The hardware design of LMS algorithm is implemented via using hardware description language VHDL and FPGA. First, adaptive parameters are obtained via the simulation of LMS-based adaptive equalizer on MATLAB platform. Second, the data processed by FPGA, such as step size, input and output signals, desired signals, and coefficients of equalizer, is strictly expressed into the fixed-point number. Third, according to the function of the module, the system structure of FPGA-based LMS algorithm is divided into data storage module, state control module, output computation module,

error adjustment module, and weight update module, and drawn. Fourth, based on Top-down design idea, pipeline control module with parallel and serial structure, fixed-point operation, the time sequences of the control signals are analyzed. Finally, the performance of FPGA-based system structure of LMS algorithm in time sequence and function is synthesized and simulated on Quartus II 4.1 platform and Stratix II family, and the research results show that it is feasible to implement adaptive filter using FPGA.

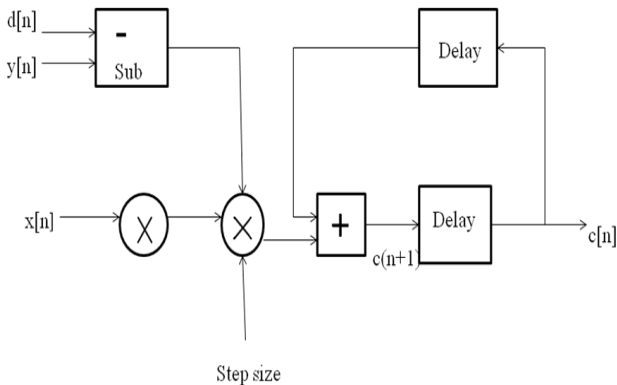


Figure 2 LMS Algorithm Implementation

IV IMPLEMENTATION OF ADAPTIVE LMS EQUALIZER

One of the fundamental components of a Communication System is the Transmission Channel. Ideally, the transmission channel should not introduce distortions in the signal that is transmitted, but this seldom the case. Instead it introduces a distortion and its Frequency Response may be characterized as $H_c(f)$. Thus in order to reverse the effect of this distortion, we introduce an Equalizer in the Receiver section, just after the channel.

Application of “fine-grained” pipelining within the filter processors and careful selection of the filter architecture, results in a high speed, low latency design. In general, a reasonably large step size of the adaptive filter is required to achieve a good adaptive filtering performance. However, a small step size has to be employed for the pipelined adaptive filter in order to prevent divergence of filter caused by the large latency of the pipelined filter. A pipelined adaptive LMS filter with a low-latency design is therefore highly desirable Electronic Support Measures Receivers (ESM).

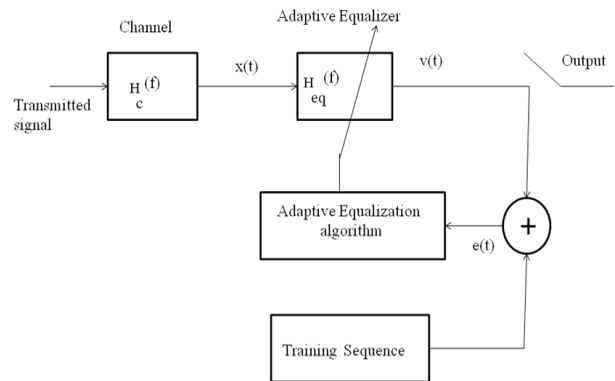


Figure 3 Block Diagram of Adaptive Equalization Process

A. FPGA-BASED FINE-GRAINED PIPELINED LMS FILTER ARCHITECTURE

Two different adaptive LMS predictor architectures based on the fine-grain pipelined DLMS algorithm were selected. The TF fine-grained pipelined DLMS (TF-FPDLMS) is designed for ease of expansion while still maintaining the system sampling rate. The direct-form fine-grained pipelined DLMS (DF-FPDLMS) architecture is well optimized for filtering and speed/cost performance. The advantage of using the direct-form over the TF approach is that the output latency is not linearly dependent on the filter order. In this structure, the pipelining effect on a single tap PM does not carry forward to other taps.

A brief description of the components used to implement the FPDLMS filters is given below:

Reg (1-AoS): A register to store the signal value.

Mult (7-AoS): An 8x 8-b pipelined adder-tree multiplier with a 16-b output format—pipelined at partial product generator and at the first and second adders in the tree.

Adder (1-AoS): An 8-b or 16-b input adder with registered output (As a smaller value of step size u is used for pipelined design, the internal word length is increased to 16-b to accommodate the small coefficient values).

u scaling circuit (0-AoS): A 6-b arithmetic shift right (ASR) operation.

B. VHDL SIMULATION

In this project the input signal $x(n)$ and desired signal $d(n)$ have taken and five tap LMS adaptive equalizer is simulated using VHDL. The three parts of LMS algorithm is designed with the architecture. The following equations are designed with this architecture.

$$Y(n) = W_0(n-1)X(n) + W_1(n-1)X(n-1). \quad (1)$$

$$e(n) = d(n) - Y(n). \quad (2)$$

$$W_0(n) = W_0(n-1) + \mu e(n) \cdot X(n). \quad (3)$$

$$W_1(n) = W_1(n-1) + \mu e(n) \cdot X(n-1) \quad (4)$$

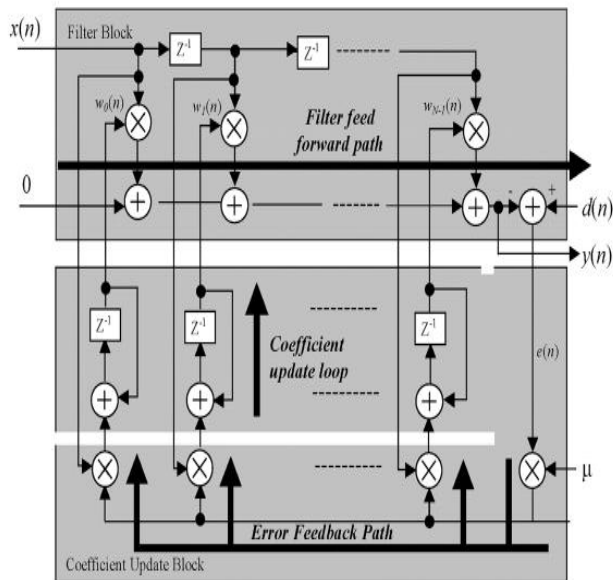


Figure 4 Structure of the FIR-LMS filter—possible pipelining paths

First we started our design with simulating each tap in VHDL and then by cascading all taps to form a 5 tap filter as shown in the above figure where each tap consists of adder, multiplier, truncation and saturation circuit which are implemented using VHDL. Then we implemented adaptive equalizer routine which produces error depending on the output produced by the filter and the desired response. We have then integrated this equalizer with display MSE unit to show the squared error which includes a 4x1 mux and a binary to 7 segment displays.

V CONCLUSION AND FUTURE WORK

We have described a pipelined implementation of the LMS adaptive filter. VHDL simulation of five tap adaptive equalizer is tested for LMS algorithm. The Least Mean-Square algorithm was found to be the most efficient training algorithm for FPGA based adaptive filters. The issue of whether to train in hardware or software is based on bandwidth needed and power specifications, and is dependent on the complete system being designed. The future scope is that to reduce the hardware complexity and feedback latency still more, sign-

sign LMS algorithm can be used for VHDL simulation of adaptive channel equalizer which results in area and power savings.

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