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Implementation of 4*4 Fast Vedic Multiplier using Power Gated GDI Technique

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***Abstract*—Multipliers are used in the building blocks of several processors. Conventional multiplication is a time-consuming and lengthy process; to overcome these drawbacks the circuit designers must develop speedy multipliers. Vedic multipliers can be utilized for the high-speed multiplication process. In Designing CMOS circuits, an issue of the area is always there, to reduce this Gate Diffusion Input (GDI) technique can be used. The GDI concept assists in the reduction of Transistor Count (TC), due to this power dissipation is minimized. Leakage power has become a serious issue in the microelectronic circuit design as the technology scales down to a deep submicron process. The new architecture includes a power gating technique using a sleep transistor. Sleep transistor technique is a simple concept to mitigate the effect of leakage power which uses extra transistors to turn off power supplies in the logic circuit during standby mode.**

Keywords—MultipliersHalf Adder, Full Adder, Vedic Mathematics, GDI, Vedic Multiplier, Power gating.

I. INTRODUCTION

Today most of the processors require a very high-speed operation. Arithmetic operations such as addition, subtraction and multiplication are deployed in various digital circuits to speed up the process of computation. Multiplication is the most important arithmetic operation in signal processing and itsapplications. All the signal and data processing operations like digital signal processing involve multiplication. As speed is always a constraint in the multiplication operation, an increase in speed can be achieved by reducing the number of steps in the computation process. In any digital system design, the three main performance parameters that determine the performance of the system are power, power, and speed. In the work presented, a combination of Vedic multiplier and GDI logic is explored for the design of the 4x4 multiplier. Very little work has been reported in the literature for a combination of GDI and Vedic multiplication at the circuit level. The (DC) direct current analysis of the basic inverter is carried out to calculate the W/L ratios of transistors for different supply voltages.

The Vedic multiplier is designed using Vedic mathematics. It is named as an early mathematics, it was discovered by Shri Bhartiya Krishna Tirtha Maharaja. It is based on an idea where the productions of all partial products are completed by the simultaneous addition of partial product. Vedic mathematics has 16 Sutras which helps in solving mathematical operation, algebra and geometry. For the multiplication, UrdhvaTiryagbhyam method is used. In UrdhvaTiryagbhyam Sutra multiplication is done in vertical and cross wise operation. To reduce the power, Vedic multiplier technique is used.

A 4x4 multiplier is implemented by the amalgamation of Vedic multiplier and GDI logic. Implementation of a multiplier is done by using CMOS technique as well as GDI technique and these are compared with each other, the result of GDI technique leads to less delay. While designing a 4-bit multiplier, the half adders, as well as full adders, are the main basic blocks in a multiplier.

Our proposed system consists of a sleep transistor. The sleep transistor technique can be introduced as the simplest approach to reduce these leakage currents. The sleep transistor technique includes additional transistors in the pull down and pull up circuits. There are two modes of operation; active and standby mode. In the former mode of operation, additional transistors are turned on and the normal operation takes place. The logic circuits will be disconnected in the latter mode because additional transistors are in off state. This technique, thus by detaching the logic networks from the power supply and ground, lowers the standby mode leakage power.

II. VEDIC MULTIPLIER AND GDI

A multiplier is one of the key hardware blocks in most of the processors. Multiplication is a lengthy, time-consuming task. Vedic multiplication in field-programmable gate array implementation has been proven effective in reducing the number of steps and circuit delay. Conventionally at the circuit level, complementary metal-oxide-semiconductor (CMOS) logic is used to design a multiplier. In CMOS circuits, the area is always an issue. Gate diffusion input (GDI)-based logic has been explored in the literature to reduce the number of transistors for various logic functions. Thus, Vedic mathematics, on the one hand, simplifies the multiplication process and reduces the delay; while on the other hand, GDI technique helps in minimizing the transistor count (TC) and reduction in power. Therefore, this study puts forth a GDI logic-based Vedic multiplier.

To study the effectiveness of the GDI logic, the transient response of a 2-bit Vedic multiplier using CMOS and GDI is compared. For the 4-bit Vedic multiplier, two design approaches are taken into consideration. The performance of these circuits is analyzed in terms of average power dissipation, delay, and TC. The effect of supply voltage scaling is also studied. The circuit simulations are carried out at 180 nm for bulk metal oxide semiconductor field effect

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transistor predictive technology model-based device parameters.

A. VEDIC MULTIPLIER FOR 2x2 BIT

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. The 2x2 vedic multiplication flow and architecture is shown in fig.1 and fig.2.

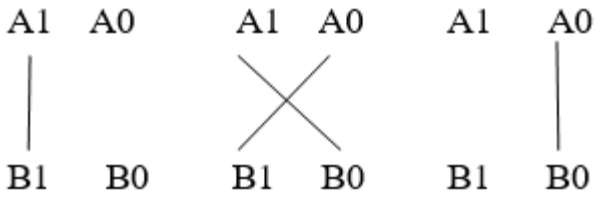

Fig. 12x2 Vedic multiplication

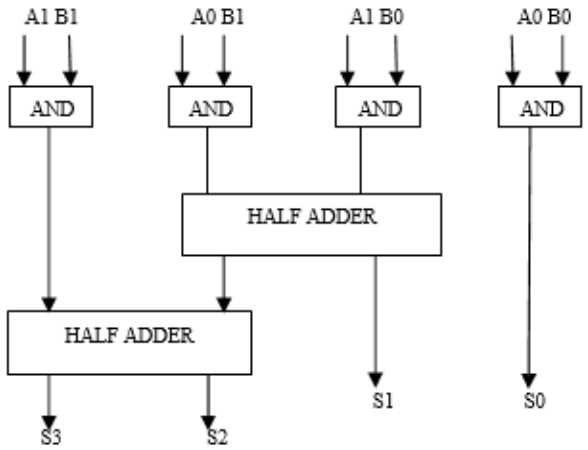

Fig.2 2 Bit Vedic Multiplier

B. GATE DIFFUSION INPUT TECHNIQUE (GDI)

Morgenshtein et al. invented the GDI logic in 2002. To prove the practicability of GDI, an 8-bit carry look-ahead adder (CLA) was fabricated and tested which showed 45% reduction in the power-delay product than CMOS. Moaiyeri et al. demonstrated a GDI-based three-input XOR gate. It was found to be both area and power-efficient. The basic GDI cell is shown in fig.3. The The basic difference in GDI and CMOS is seen in a two-input AND gate . AND gate is 2T in GDI, also, the AND gate followed by an inverter forms a NAND gate. Therefore, the NAND gate is 4T. For delay calculation, the logic effort of the circuit is estimated. The logical effort is the capacitance seen by the input of the NAND gate to that of an inverter. Assuming, the pMOS to nMOS sizing ratio to be 2:1. The capacitance seen by the input A is 3 and it is used to find logical effort. For the two-input CMOS NAND gate, the logical effort is 4, while for GDI it is 1. Therefore, GDI is believed to be an area-efficient technique with reduced logical effort.

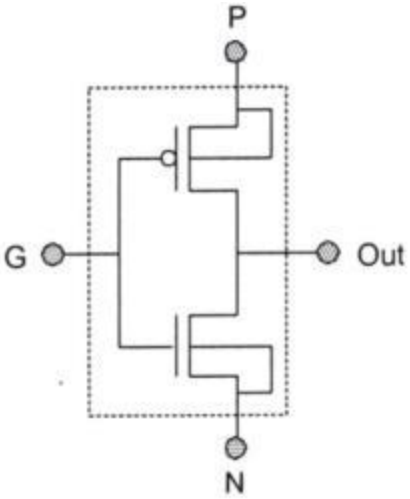

Fig 3. The Basic GDI Cell

III. PROPOSED ARCHITECTURE

Sleep transistor technique is a simple concept to mitigate the effect of leakage power which uses extra transistors to turn off power supplies in the logic circuit during standby mode.

The sleep transistor technique can be introduced as the simplest approach to reduce these leakage currents. The sleep transistor technique includes additional transistors in the pull-down and pull-up circuits. There are two modes of operation; active and standby mode. In the former mode of operation, additional transistors are turned on and the normal operation takes place. The logic circuits will be disconnected in the latter mode because additional transistors are in off state. This technique, thus by detaching the logic networks from the power supply and ground, lowers the standby mode leakage power.

Fig.4 shows the basic block diagram of the proposed 4x4 fast Vedic multiplier with power gating technique. The 4x4 multiplier is designed using four 2x2 vedic design. If any of the input pair is zero, then that particular 2x2 multiplier is turned off.

For example, for first 2x2 vedic multiplier the inputs are A1A0 and B1B0. If both the input of any one of the operand is zero, the entire product of that multiplier is zero. This multiplication process can be avoided using power gating logic.

(A1 | A0) & (B1 | B0) =0------- (1)

When the condition present in equation 1 is satisfied then power gating is applied. If A1=0 and A0=0 or B1=0 and B0=0 then entire multiplier calculation is avoided using power gating logic. The similar logic followed for all four 2x2 vedic multipliers to minimize the unwanted transitions.

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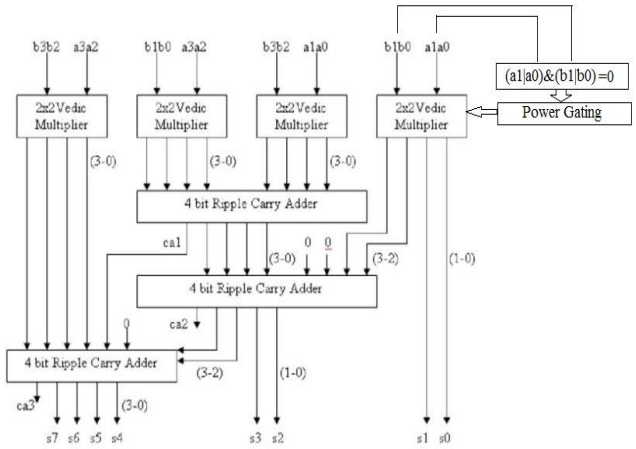

Fig.4 Vedic 4x4 multiplier with power gating

IV. RESULTS AND DISCUSSION

The timing diagram and the power dissipation for the proposed 4x4 Vedic multiplier are discussed in this section. Circuit simulation is made by Microwind DSCH2 tool. The layout and power consumption is calculated in Microwind tool for 90nm technology. Half adder and full adder are implemented using GDI technology, and it is used to design 2x2 vedic multiplier. The result of GDI is having low power dissipation compared to conventional CMOS design. Fig.5 shows the schematic diagram of existing 4x4 vedic multiplier with GDI based full adder and half adder.

Fig.6 shows the schematic of proposed 2x2 vedic multiplier with power gated logic. The operand pair is checked for zero condition based on which sleep transistor performs the gating function. Fig.7 shows the schematic of 4x4 vedic multiplier using four 2x2 design each incorporated with power gating logic. Fig.8 shows the layout of proposed multiplier for 90nm technology.

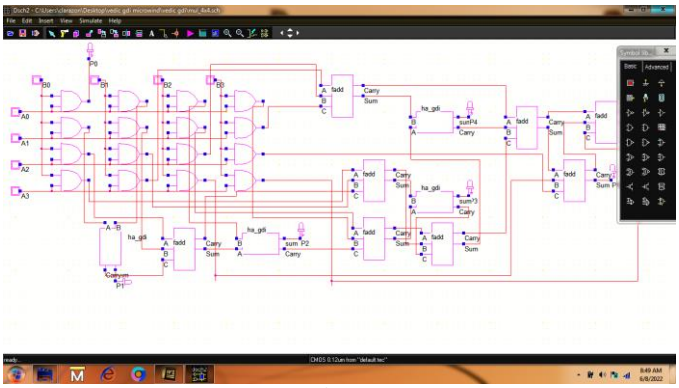

Fig.5 Scematic diagram of existing 4x4 vedic multiplier

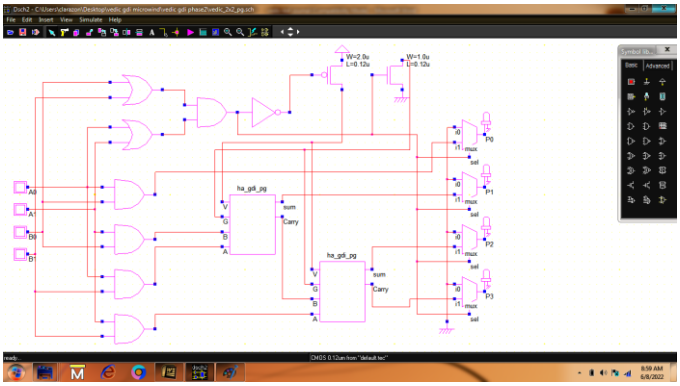

Fig.6 Scematic diagram of 2x2 vedic multiplier with power gating logic

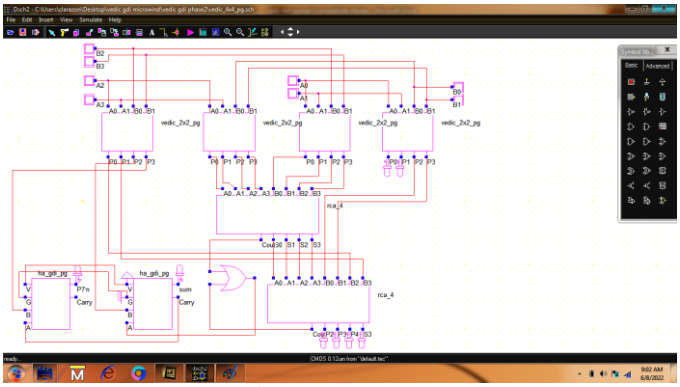

Fig.7 Scematic diagram of 4x4 vedic multiplier with power gating logic

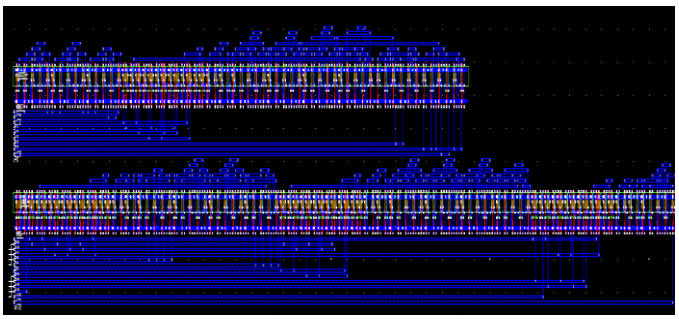

Fig.8 Layout of 4x4 vedic multiplier for 90nm

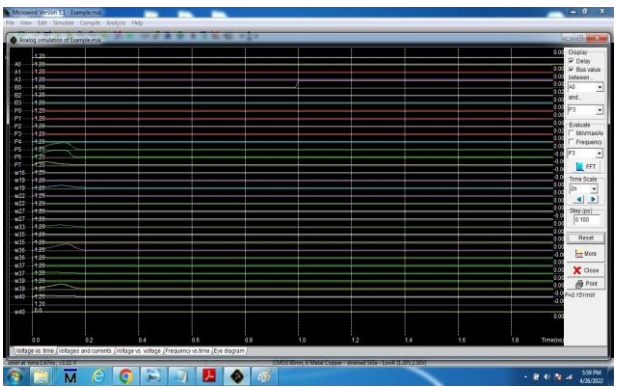

Fig.9 Power result of existing vedic multiplier

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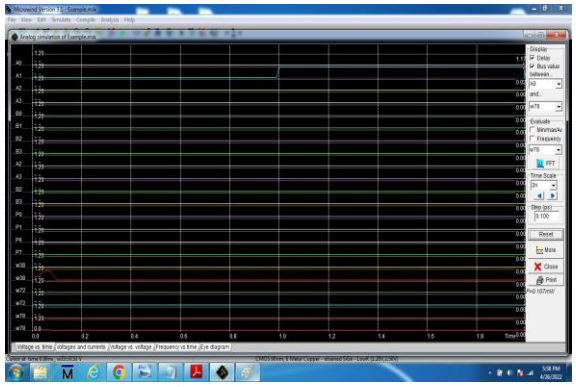

Fig.10 Power result of proposed vedic multiplierbased on power gating

Fig. 9 and 10 shows the power result of existing and proposed multiplier. For 90nm technology existing multiplier consumes 0.151mW and using power gating technique it is reduced to 0.107mW. Fig.11 shows the simulation result obtained using DSCH2 tool for its functional verification.

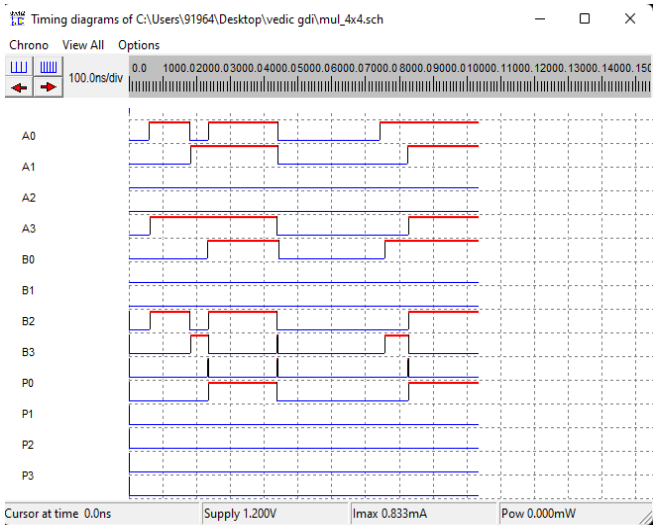

Fig.11 Simulation result of 4x4 Vedic Multiplier

V. CONCLUSION

In this article, a 4 2*2 Vedic multiplier with high speed and reduced complexity can be designed since there is parallelism in the partial product generation. The Vedic multiplier is thus optimized in terms of speed, area and power. While applying leakage power reduction techniques using various sleep transistor approaches, the returns for power and delay can be correlated. The leakage power reduction can be attained more in standby mode than active mode. The presence of additional transistors in the circuit causes anhigh increase in propagation delay. Of all the techniques, power gating achieves more power-saving and increases speed. Drain gating technique has more leakage reduction in active modeCircuit complexity reduces, with the concept of GDI and Vedic mathematics. The high-speed adders are designed using the GDI technique, which are used to reduce power dissipation with increased speed. It is achieved due to decrease in transistor counts. The power gated sleep method is a new remedy for designers. This technique shows the least speed power product among all techniques. The Proposed technique achieves ultra-low leakage power consumption with much less speed, especially it shows nearly 50-60% of power than the existing. So, it can be used for future IC'S for area & power Efficiency

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