Implementation in High Power Factor Application System Using SEPIC Converter on Discontinuous Operation

[1]M.Senbaga,
P.G Scholar,
[1]Pandian SaraswathiYadav Engineering College,
Sivagangai, Tamilnadu.

[2]S.Sathyamoorthi
Assistant Professor
[2]Pandian SaraswathiYadav Engineering College,
Sivagangai, Tamilnadu.

Abstract

My aim is an implementation in high power factor application based on SEPIC converter operating in discontinuous conduction mode for achieving the control of grid connected power system and unity power factor. This approach is found to be attractive for power factor application and reduced total harmonic distortion. Detailed design criteria for the power and control stages of the single-phase and three phase SEPIC converter circuit are presented. The DCM operation gives additional advantages such as zero-current turn-on in the power switches, zero-current turn-off in the output diode and reduces the complexity of the control circuitry. Due to this fact, the pulse width modulation (PWM) technique is studied. The proposed system is confirmed by experimental implementation.

***Index Terms*—single-ended primary-inductor converter (SEPIC), converter, discontinuous conduction mode (DCM), power factor correction (PFC), single-phase rectifier, three phase rectifier, PWM technique.**

1. INTRODUCTION

In the previous sections, Compared to conventional buck or boost converters, this allows a low current ripple at the input for a relatively low level of the DC-bus voltage. In passive topologies 12- and18-pulse rectifiers with or without isolation are used, while others are hybrid structures. In the case of active structures, control could be done in the input current, output voltage In this paper an analysis of the CCM operated input current wave shaping technique using inductor voltage sensing for power factor correction (PFC) rectifier based on isolated SEPIC converters is introduced. The voltage conversion ratio of the SEPIC converter is used to derive the operation of control circuit. The duty ratio is obtained by

Comparing an integral signal of the rectified inductor voltage and a negative ramp carrier waveform.

The Circuit parameters are designed based on operations of SEPIC converter between DCM and CCM. The small signal modelling is determined and used to design output voltage regulator circuit. The proposed analysis is verified by the circuit experimentation of 100 W SEPIC rectifiers.

In this process, it is operating in discontinuous conduction mode. This circuit is more unforgiving than the boost converter, because the MOSFET and diode voltages and currents are higher to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost High-frequency isolation, unidirectional or bidirectional systems, single- or multiple-stage converters, and those related to continuous or discontinuous operational modes. In summary, if only the structures that result in a unity power factor (PF), low input current total harmonic distortion (THD), controlled output voltage and isolation from the mains are considered, three criteria may be highlighted: number of stages, isolation, and control strategy.

In relation to the number of stages, systems with two or more stages are commonly found[1], where the first stage is responsible for the rectification and the power factor correction (PFC) and the second for the isolation and output voltage regulation .Even with the individual efficiency of each block being high, the global efficiency of this kind of structure is generally low. Thus, in the search for better efficiency, the

application of structures that accomplish all the energy processing in a single-stage is an interesting approach. In the case of the three-phase rectifier, structure control, usually applied for PFC, is generally complex and involves the monitoring of input currents and complicated control loops.

2. STRUCTURAL CONSTRUCTION OF MODEL

Moreover, to operate in CCM, the single-phase PFC circuit requires a complex control, as well as a large intermediate bus capacitor to limit the bus voltage ripple and handle the pulsating power in the intermediate.

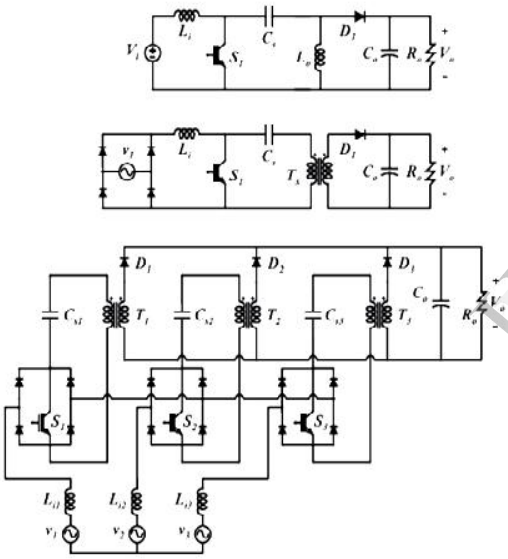

Fig 1: a)Non-isolated sepic, b)Isolated single stage rectifier, c)Proposed three phase isolated rectifier

2.1. Impact of DCM Operation on the Input Current Ripple

Due to the DCM operation of the power stage, the current ripple in the input boost inductors is quite large, as compared to those of CCM rectifiers. A higher input current ripple requires a larger input filter, which increases the rectifier cost. To show the impact of the DCM operation on the amplitude of the high-frequency input current ripple, it compares the high-frequency spectrum of the input currents for three different cases: (1) single-phase CCM boost rectifier; (2) VIENNA rectifier; and (3) single-switch three phase DCM boost rectifier. As can be verified, all cases draw the same power per phase at the same switching frequency. The boost inductances of the CCM rectifiers (single-phase CCM boost and VIENNA) were designed to limit the maximum peak-to-peak input current ripple to below 25% of the fundamental input peak current value. The bus voltage in all cases is chosen accordingly to allow proper operation. The system parameters used for the DCM boost rectifier.

3 .PRINCIPLE OF OPERATION AND ANALYSIS

When the switch is closed, the SEPIC DCM operation is cleared about the discontinuous operation of the current on the output diode. In open condition the output current in zero. When this operation mode is ensured, the converter is capable to follow a resistance, obviously providing a sinusoidal input current in phase with the input voltage. As a end result, only a simple control loop is required to control the system output voltage. In the three-phase system, the DCM is characterized by the same criteria. Thus, to obtain the converter operation in this mode, it is necessary to make sure that the discontinuous currents across the three output diodes. The conventions adopted for voltages and currents are also expressed in ,

$$Vo=Vo_1=Vo_2=Vo_3 \quad (1)$$

$$io=io_1+io_2+io_3 \quad (2)$$

$$L_{i1} \gg L_{01}$$
$$L_{i2} \gg L_{02}$$
$$L_{i3} \gg L_{03}$$

$$Vc_{s1}=|V_1|$$
$$Vc_{s2}=|V_2|$$
$$Vc_{s3}=|V_3|$$

$$L_{i1}=L_{i2}=L_{i3}=L_i \quad (3)$$

The three-phase input voltages are sinusoidal; however, due to the symmetry, the system presents the same behaviour for each sector of 30◦. Therefore, in order to reduce the mathematical complexity, it is possible to analyze the system only for one sector and expand it to a whole main grid period.

In the case of the input voltages are featured in the relations expressed by (2). In this situation, dc-dc Voltage source, respecting the relations in (2), may be adopted to represent the system operation

$$|V_3| > |V_1| > |V_2| \quad (4)$$

$$|V_1| > 0 \quad |V_2| > 0 \quad |V_3| < 0 \quad (5)$$

4. SEPIC OPERATION AND DESIGN

This circuit is more unforgiving than the boost converter, because the MOSFET and diode voltages and currents are higher. SEPIC is a DC/DC converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage.

This type of conversion is handy when the designer uses voltages from an unregulated input power supply. Hence this is very much preferred in applications such as battery chargers, power electronic circuits, home appliances, aircraft due to its less electromagnetic interference, inherent inrush current, reduced noise disturbances and less switching losses.

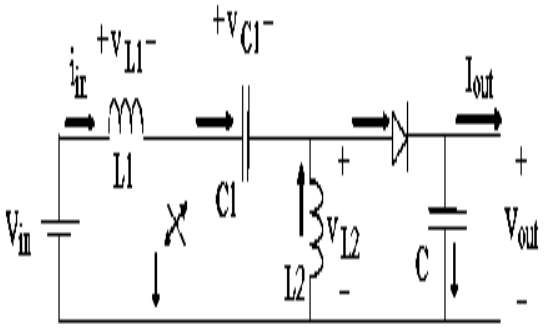

Fig 2:Circuit Diagram of the sepic converter

.

The bridgeless boost rectifier has the same major practical drawbacks as the conventional boost converter, such that the dc output voltage is always higher than the peak input voltage, input–output isolation cannot easily be implemented, the start up inrush current is high, and there is a lack of current limiting during overload conditions. Moreover, it is well known that the boost converter operating in discontinuous current mode (DCM) can offer a number of advantages such as inherent PFC function, very simple control, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the DCM operation requires a high-quality boost inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more robust input filter must be employed of the rectifier. The operation of SEPIC is similar to the bridgeless buck-boost PFC converter which has only three conduction semiconductors at every moment. Comparing with the cascade buck-boost CBB-PFC converter, the efficiency is increased. Power factor is more than 0.98, and total harmonic distortion (THD) is less than one. The main features of the presented converter include high efficiency, low voltage stress on the semiconductor devices, and simplicity of design. These advantages are desirable features for high-power and high-voltage applications. The modelling and simulation result of Bridgeless Discontinuous Conduction Mode SEPIC Power Factor Correction rectifier is presented.

4.1. Mathematical Analysis

From the description of the operation stages [1], it is possible to obtain the equivalent circuits whose analysis results in a linear system that, when solved, provides the system solution.

The interaction of the system phases can be observed from the input current waveform, in which, in contrast to a single-phase converter, there is a behavioural change in the input current, between the active switch turn off and subsequent turn on, evidenced by stages 2 through 5. The three-phase system was mathematically solved considering the complete system, and the important results are those related to the average values reported herein.

$$I_o = \frac{3}{4}\frac{V_p^2 D^2}{V_o f_s L_{eq}} \quad (6)$$

$$L_{eq} = \frac{L_i L_o}{L_i + L_o} \quad (7)$$

$$\overline{I_o} = D^2 \frac{V_p}{V_o n} \quad (8)$$

$$V_o = V_p D \sqrt{\frac{3R_o}{4 f_s L_{eq}}} \quad (9)$$

$$G = \frac{D^2}{\overline{I_o}} \quad (10)$$

$$D_{\lim} < \frac{G}{(1+G)} \quad (11)$$

$$P_o = P_i = P_{3\phi} = \frac{3}{2} V_p I_p = \frac{3}{4} \frac{V_p^2 D^2}{f_s L_{eq}}. \quad (12)$$

The average value for the output current is given by (6). This expression confirms that the three-phase system is equivalent to three single-phase systems connected in parallel. The parameter L_{eq} results from the parallel association of the input and output inductances, (7). The parameterized average output current expression, considering the transformer turns ratio n is given by (8) and the average output voltage is given by (9). The load characteristic is a function of the static gain and the parameterized output current, given by expression (10), and it is shown in Fig. 4, where the duty cycle limit D_{lim} between CCM and DCM is defined by equation (11). Through the application of (6), it is possible to derive an expression for the output power. In addition, considering the system operating with unitary efficiency, the input power is equal to the output power, according to (12). Equation (12) also shows the advantage referred to the three-phase system employment, since the input power is constant

4.2. Influence of the Modulation Type

As previously noted, the classical modulator is considered in all of the previous descriptions. Under this condition, the complete system is characterized by the waveforms, from which it can be noted that the input current and voltage (depicted only for one phase) are sinusoidal and in phase with one other. Additionally, it is observed that the voltage across the SEPIC capacitor follows the input voltage, confirming the supposition. A second alternative is to employ a modulator, from where the switches are commuted with a 120◦ phase shift.

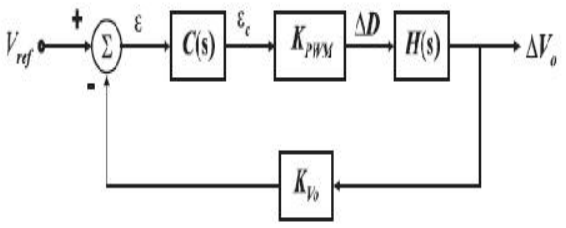

Fig 3:Block diagram of the proposed control strategy

Consequently, the input current ripple, for the same inductance value, is reduced and presents a minor current waveform distortion in the zero crossing. There are no significant changes in the high-frequency operation on comparing the two modulators, but the number of operation stages is increased in the second one, resulting in a more complicated mathematical analysis. The component stresses are similar, but now there is an advantage associated with the output current. Due to the shift of the module operation, the currents of the output diodes are also shifted, implying that their peaks do not appear together, reducing the current stresses on the output capacitor.

5. SIMULATION RESULT PERFORMANCE

Relevant voltage and current waveforms are shown, for rated power and voltages, which are in agreement with the expected results. It can be observed that the maximum voltage across the active power switch is equal to the sum of the line-to-neutral input peak voltage and the load voltage referred to the transformer primary side. The currents on the semiconductors increased and, consequently, the conduction power loss are increased because the converter operates in DCM and this is the major downside of the topology.

Fig.7 shows the output open loop control waveform with the currents through the output diode. The peak currents of the diodes appear simultaneously, as expected. Fig. 12 shows the output waveform for the closed loop control of the PFC Rectifier.

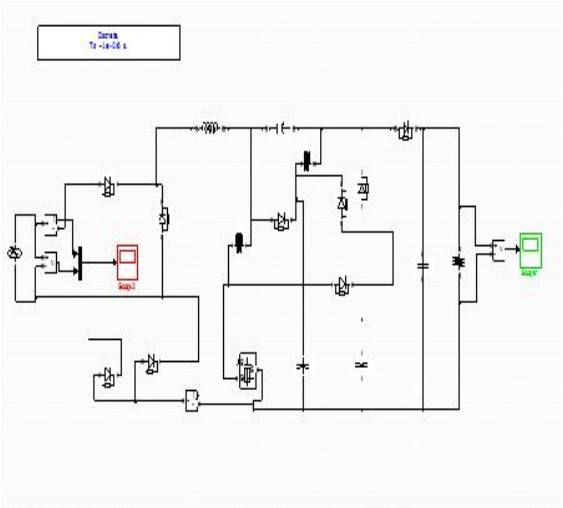

Fig 4: Open Loop control of DCM SEPIC PFC Rectifier

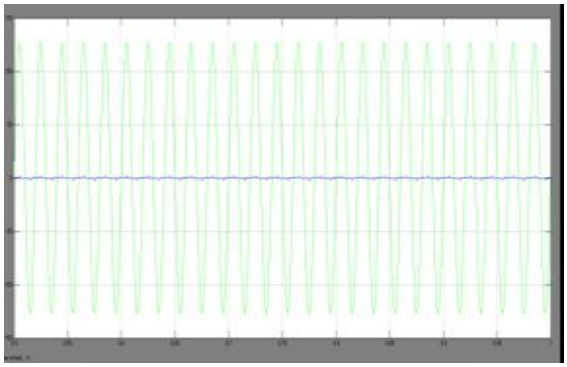

Fig 5 :Input waveform for the Open Loop control of DCM SEPIC PFC Rectifier

The measured efficiency curve of the non optimized laboratory prototype, designed and built only for concept proof purposes is shown.

The efficiency is 90% for the rated power operation. It is possible to improve the converter efficiency by employing better magnetic material, low conduction loss power semiconductors, and regenerative clamping or snubber circuits.

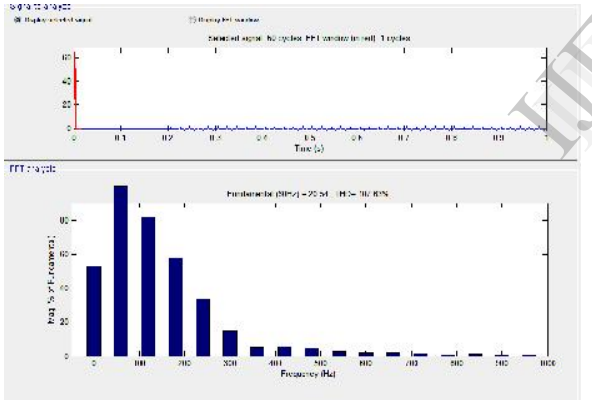

Fig 6: THD Rating for the input

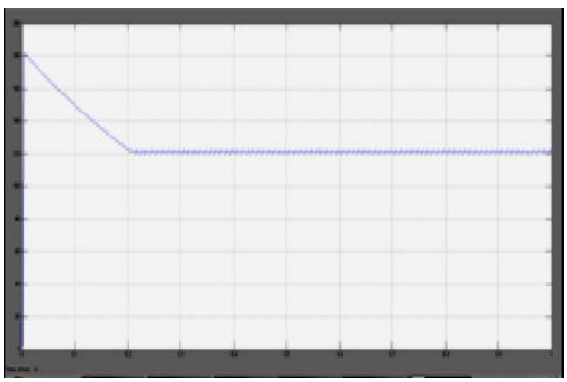

Fig 7: Output waveform for the Open Loop control of DCM SEPIC PFC Rectifier

The main contribution of the phase-shift modulator is the reduction of the output capacitor current stress, without affecting the average current.

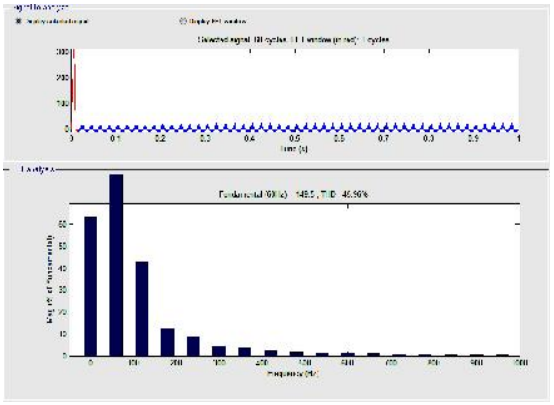

Fig 8: THD Rating for the output waveform

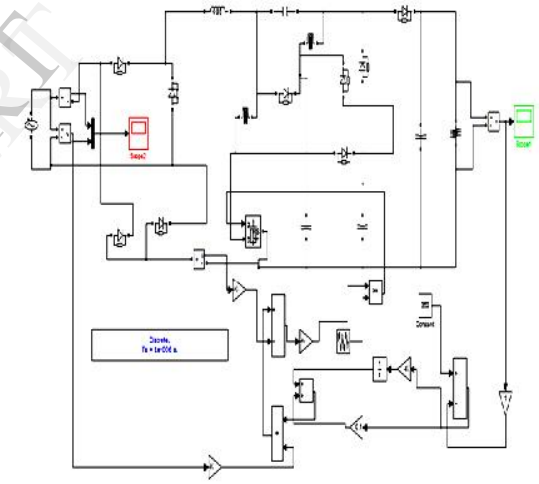

Fig 9: Simulation diagram of the closed loop control of DCM Rectifier

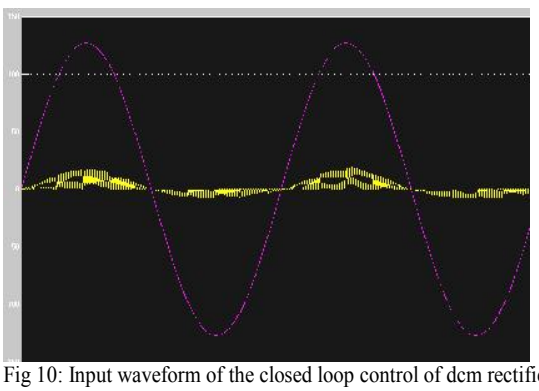

Fig 10: Input waveform of the closed loop control of dcm rectifier

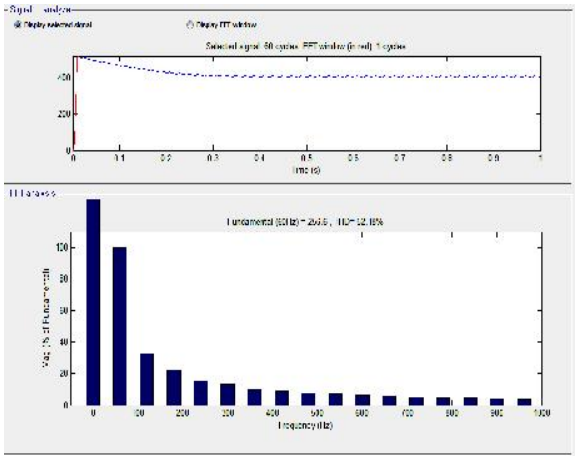

Fig 11: THD rating of the closed loop control

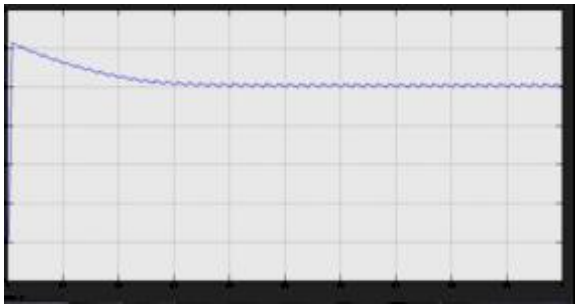

Fig 12: Output waveform for the Closed Loop control of DCM SEPIC PFC Rectifier

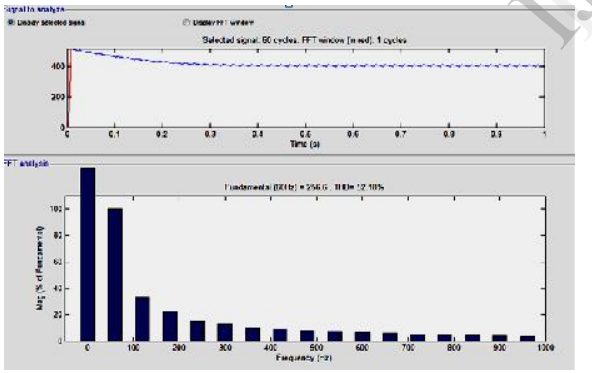

Fig 13:THD Rating of the closed loop control

Table 1: Specifications and Parameters of the proposed System

Characteristics	Sepic Rectifier Modules
Input Inductance	3.631mH
Output Inductance	97.72µH
Sepic Capacitances	1.5µH
Input Voltage	380V
Switching Frequency	40KHz
Output Voltage	400V
Power Rating	4KW

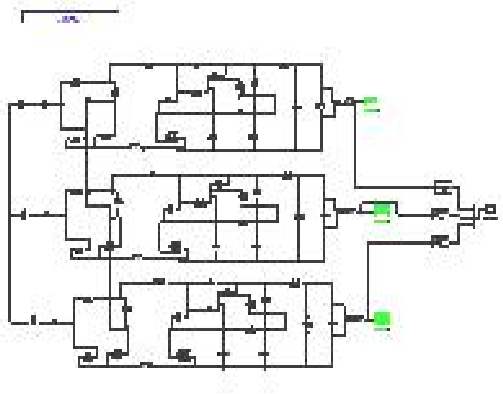

Fig 14: Simulation diagram of 3phase control of DCM Rectifier

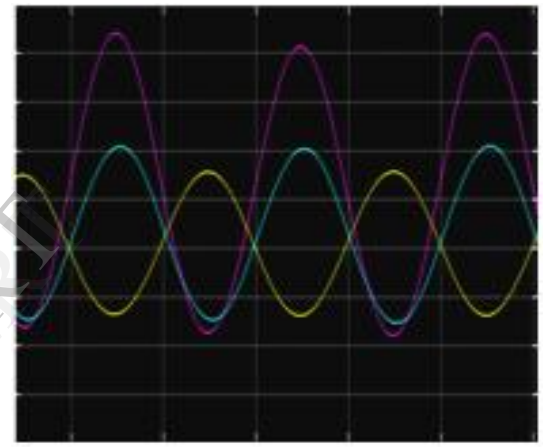

Fig 15: Output waveform for the proposed three phase rectifier

CONCLUSION

The single-phase DCM SEPIC rectifiers with low input current distortion and low total harmonic distortion have been presented and analyzed. Closed loop technique is mainly used for minimizing the THD rating, leading to a cost reduction, simplicity, and robustness. To maintain same efficiency, the improved circuits could operate with higher switching frequency. In addition to the single phase, a three-phase isolated high PF rectifier topology based on the dc–dc SEPIC operating in the DCM was presented. Thus, additional reduction in the size of PFC inductor and EMI filter could be achieved. This circuit would be most suitable to be used as a switch mode power supply application, battery chargers and telecommunications.

REFERENCES

[1] Gabriel Tibola and Ivo Barbi, "Isolated Three-Phase High Power Factor Rectifier Based on the SEPIC Converter Operating in Discontinuous Conduction Mode",IEEE Trans.Power Electron, nov 2013.

[2]H.-Y. Tsai, T.-H.Hsia and D. Chen, "A novel soft-switching bridgeless power factor correction circuit," in Proc. Eur. Conf. Power Electron. Appl., 2007, pp. 1–10. [2]

[3]J. C. Liu, C. K. Tse, N. K. Poon, B. M. Pong, and Y. M. Lai, "A PFC voltage regulator with low input current distortion derived from a rectifierless topology," IEEE Trans. Power Electron., vol. 21, no. 4, pp. 906–911,Jul. 2006.

[4] H. Y. Kanaan, K. Al-Haddad, G. Sauriole, and R. Chaffai, "Practical design of a SEPIC power factor corrector with DC-voltage regulation," in*Proc. IEEE Int. Symp. Ind. Electron.*, 2006, pp. 964–969.

[5] T. Tanitteerapan, "Analysis of power factor correction isolated SEPIC rectifiers using inductor detection technique," in *Proc. 47thMidwest Symp. Circuits Syst.*, 2004.

[6]B. N. Singh, A. Chandra, P. Rast goufard, and K. Al Haddad, "Single phase switch mode boost rectifier: An improved design/control applied tothree phase AC-DC converters to power up telecommunication system," in *Proc. 24th Annu. Int. Telecommun. Energy Conf.*, 2002, pp

[7] Y. K. E. Ho, S. Y. R. Hui, and L. Yim-Shu, "Characterization of single stage three-phase power-factor-correction circuit using modular single phase PWM DC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 15,no. 1, pp. 62–71, Jan. 2000.

[8] J. W. Kolar, H. Sree, U. Drofenik, N. Mohan, and F. C. Zach, "A novel three-phase three-switch three-level high power factor SEPIC-type AC to-DC converter," in *Proc. 12th Annu. Appl. Power Electron. Conf. Expo.*,1997, vol. 2, pp. 657–665.

[9]M. Depenbrock and C. Niermann, "A new 12-pulse rectifier circuit with line-side interphase transformer and nearly sinusoidal line currents," in *Proc. 6th Conf. Power Electron.Motion Control*, 1990.

[10] D.M. Mitchell, "AC-DC Converter having an improved power factor",*U.S. Patent* 4,412,277, Oct. 25, 1983.

[11] K. Georgakas, A. Safacas,"Power Factor Improvement of an AC-DC Converter via Appropriate sPWM Technique" **.**

[12] M. R. Sahid, A. H. M. Yatim, Taufik Taufik, University Technology Malaysia "A New AC-DC Converter Using Bridgeless SEPIC".