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Hysteresis Current Control of Split Capacitor type Elementary Additional Series Positive Output SLC

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Abstract

Super lift converter (SLC) is a new series of DC/DC converter possessing high voltage transfer gain, high efficiency, reduced ripple voltage and current. Super lift technique armed by split capacitors increases the output voltage in higher geometric progression. This paper focuses on splitting the input side capacitor of the additional series positive output super lift converter response controlled with two different control techniques. The first control technique is PI control, while the second control technique is sliding mode control. The sliding mode control shows to be more effective than PI control especially when dynamic tests are applied. Sliding Mode control designed to regulate the converter against audio susceptibility and output impedance variation. Simulation study of the proposed converter along with the controller has been carried out in MATLAB/SIMULINK to investigate the static and dynamic response of the converter.

1. Introduction

Super lift converter for a given input voltage, the output voltage increases stage by stage in geometric progression. Voltage conversion from line side to load side voltage. Positive Output Super Lift Converter (POSLC) is a new series of DC to DC converter possessing high voltage transfer gain, high power density, high efficiency, reduced ripple voltage and current. It effectively increases the voltage transfer gain in higher proportion [1-4]. Split capacitor type positive output super lift converter splits the energy storage element capacitor into α parts, effectively increases the energy storage in each capacitor. The stored energy in the inductor and capacitor is pumped to the load.

Split stage in POSLC converter is defined as α stage, if α = 2 the capacitor in the circuit topology is splitted into two capacitor in the circuit which is charged to the supply voltage when the switch is in the ON condition. Positive output super lift converter is classified into two series namely main series and additional Series, these two series differs from the number of energy storage elements used in their topology.

Proportional Integral (PI) controller has been implemented for the proposed DC-DC converter. For same proposed DC-DC converter with sliding mode control (SMC) was designed. In both models converter was tested in steady state and under different disturbances. Both models showed acceptable results. This paper considers the output voltage and inductor current of the Buck converter controlled with two different control techniques, PI control and SMC. The results of both models are compared in steady state, transient region, and under line and load variations.

In this paper, state-space averaged model for split type elementary additional series positive output super lift Luo converter (SEPOSLLC) has been derived.

2. Converter Operation and Modeling of Split Type Positive Output Super Lift Converter

2.1. Circuit Description and Operation

The circuit diagram of the Split Capacitor type positive output super lift converter is shown in Figure 1. It includes DC supply voltage V_{in}, capacitors C_1 to C_3, C_{11}, C_{12} inductor L, power switch (n-channel MOSFET) S, freewheeling diodes D_1 to D_7, D_{11} and D_{12} and load resistance R.

In the description of the converter operation, it is assumed that all the components are ideal and also split capacitor type elementary additional series

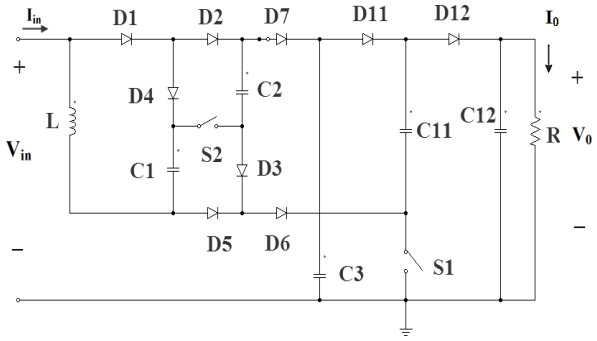


Figure 1. split capacitor type elementary additional series positive output super lift converter

positive output super lift converter operates in a continuous conduction mode. Figure 2 and 3 show the modes of operation of the converter. The voltage across the capacitors C_1 and C_2 are charged to V_{in} during the on state of the switch under the steady state condition.

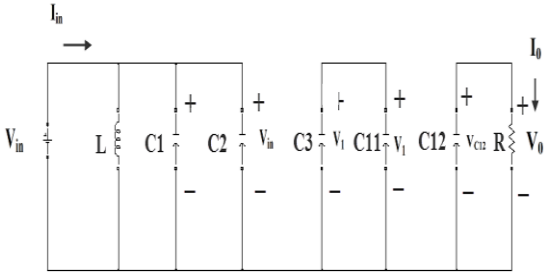


Figure 2. Mode 1 operation

The current i_L flowing through inductor L increases with voltage V_{in} during switching-on period kT

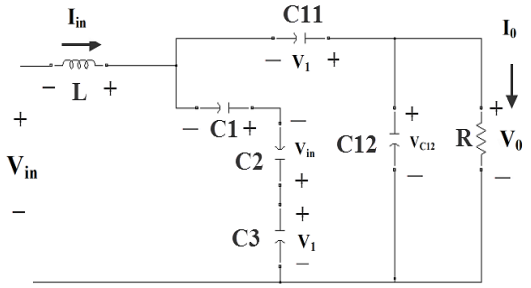


Figure 3. Mode 2 operation

Inductor L decreases with voltage $-[V_O - V_1 - V_{in}]$ during switching-off period $(1 - k)T$. The inductor current increases during switch S on, and decreases during switch S off. The peak to peak current ripple in the inductor is the same during steady state operation and it is given as

$$\Delta_{iL} = \frac{V_{in}}{L} kT = \frac{V_o - V_1 - V_{in}}{L}(1-k)T$$

(1)

$$V_0 = \left(\frac{1}{1-k} + \frac{3-2k}{1-k}\right)V_{in} \qquad (2)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{1}{1-k} + \frac{3-2k}{1-k}\right) \qquad (3)$$

The input current i_{in} is equal to ($i_L + i_{C1} + i_{C2}$) during switching-on and only equal to i_L during switching-off. Capacitor current i_{C1} and i_{C2} is equal to i_{C3} during switching-off. In steady state, the Voltage across the capacitor C_1, C_2 is equal to V_{in}. The following relations are obtained [8].

$$\begin{aligned} i_{in-off} &= i_{L-off} = i_{C1-off} + i_{C11-off} \\ i_{in-on} &= i_{L-on} + i_{C1-on} + i_{C2-on} \\ i_{C1-on} &= \frac{I_O}{k} \end{aligned} \qquad (4)$$

If inductance L_1 is large enough, i_L is nearly equal to its average current I_L. Therefore

$$\begin{aligned} i_{in-off} &= I_L = i_{C1-off} + i_{C11-off} \\ i_{C1-off} &= i_{C2-off} = i_{C3-off} \\ i_{in-off} &= I_L = \frac{2I_O}{(1-k)} \\ i_{C1-off} &= i_{C2-off} = \frac{I_O}{(1-k)} \end{aligned} \qquad (5)$$

And average input current

$$I_{in} = k i_{in-on} + (1-k) i_{in-off} = \frac{4I_o}{(1-k)} \qquad (6)$$

The variation ratio of inductor current i_L is

$$\zeta = \frac{\Delta i_L / 2}{i_L} = \frac{k(1-k)^2 R}{8(4-2k) L_1 f} \qquad (7)$$

The ripple voltage of output Vo is

$$\Delta V_o = \frac{\Delta Q}{C_2} = \frac{(1-k)T I_o}{C_2} = \frac{(1-k)V_o}{fC_2 R} \qquad (8)$$

Therefore, the variation ratio of output voltage V_o is

$$\zeta = \frac{\Delta V_o / 2}{V_o} = \frac{(1-k)}{2RfC_2} \qquad (9)$$

2.2. State space modeling

State variables $x_1, x_2, x_3, x_4, x_5, x_6$ are chosen as the current i_{L1}, the voltage V_{C1}, V_{C2}, V_{C3}, V_{C11},V_{C12} respectively. From Figure 2 When the switch is closed, the state space equation is given as

$$\begin{cases} \dot{X}_1 = \dfrac{U_1}{L} \\ \dot{X}_2 = \dfrac{U_1}{R_{in}(C_1+C_2)} - \dfrac{X_1}{(C_1+C_2)} \\ \dot{X}_3 = \dfrac{U_1}{R_{in}(C_1+C_2)} - \dfrac{X_1}{(C_1+C_2)} \\ \dot{X}_4 = \dfrac{A*U_1}{R_{in}(C_1+C_2)} - \dfrac{X_1}{(C_1+C_2)} \\ \dot{X}_5 = \dfrac{B*U_1}{R_{in}(C_1+C_2)} - \dfrac{X_1}{(C_1+C_2)} \\ \dot{X}_6 = -\dfrac{X_6}{RC_5} \end{cases} \qquad (10)$$

In Figure 3 when the switch is open, the state space equation of split capacitor type elementary additional series positive output super lift converter is given as

$$\begin{cases} \dot{X}_1 = \dfrac{k*U_1}{(1-k)*L} \\ \dot{X}_2 = \dfrac{X_1}{D*(C_1+C_4)} \\ \dot{X}_3 = \dfrac{X_1}{D*(C_1+C_4)} \\ \dot{X}_4 = E*X_1 \\ \dot{X}_5 = F*X_1 \\ \dot{X}_6 = -\dfrac{X_6}{RC_5} \end{cases} \qquad (11)$$

Where the A, B, D, E, F are constants. They are given below

$$\begin{cases} A = B = (3-2k/1-k)*(C_4/C_3) \\ C = (3-2k/1-k) \\ D = 1/(C_1+C_4*(3-2k/1-k)) \end{cases}$$

$$\begin{cases} E = 1/(C_2+C_4*(3-2k/1-k)) \\ F = (C_1*C)/(C_3*C_1+C_4*C_3*C) \end{cases} \qquad (12)$$

By using state space averaging method [7], the state space averaged equation in matrix form of the split capacitor type elementary additional series positive output super lift converter is given as

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \\ \dot{X}_4 \\ \dot{X}_5 \\ \dot{X}_6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ \dfrac{-k}{C_1+C_2}+D(1-k) & 0 & 0 & 0 & 0 & 0 \\ \dfrac{-k}{C_1+C_2}+E(1-k) & 0 & 0 & 0 & 0 & 0 \\ \dfrac{-Bk}{C_1+C_2}+F(1-k) & 0 & 0 & 0 & 0 & 0 \\ \dfrac{-Ck}{C_1+C_2}+C_1(1-k) & 0 & 0 & 0 & 0 & 0 \\ \dfrac{C_1C_4(1-k)}{C_5} & 0 & 0 & 0 & 0 & \dfrac{-1}{RC_5} \end{bmatrix} * \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \\ X_6 \end{bmatrix} + \begin{bmatrix} \dfrac{2k}{L} \\ \dfrac{k}{R_{in}(C_1+C_2)} \\ \dfrac{k}{R_{in}(C_1+C_2)} \\ \dfrac{Bk}{R_{in}(C_1+C_2)} \\ \dfrac{Ck}{R_{in}(C_1+C_2)} \\ 0 \end{bmatrix} * U_1$$

$$V = AV + BU \qquad (13)$$

Its output equation is given as

$$V_0 = V_{C12} \qquad (14)$$

Where R_{in} is internal resistance of source, u is input variable, k is duty cycle or the status of the switches, X_1, X_2, X_3, X_4, X_5 and X_6 are the vectors of the state variables (i_{L1}, V_{C1}, V_{C2}, V_{C3}, V_{C11}, V_{C12}) and their derivatives respectively.

3. Design of PI Control

The PI control is designed to ensure the specified desired nominal operating point, to regulate the voltage for split capacitor type elementary additional series positive output super lift converter. The PI control settings proportional gain (K_P) and integral time (T_i) are designed using Zeigler – Nichols tuning method. Values of L and T obtained from open loop of split capacitor for enhanced positive output super lift luo converter are as follows L = 0.0002s and time constant T = 0.004s. The delay time and time constant are determined by drawing a tangent line at the inflection point of the S-shaped curve and determining the intersections of the tangent line with the time axis and line output [10]. Ziegler and Nichols suggested to set the values of K_P= 1.8 and T_i = 0.0066 s [6].

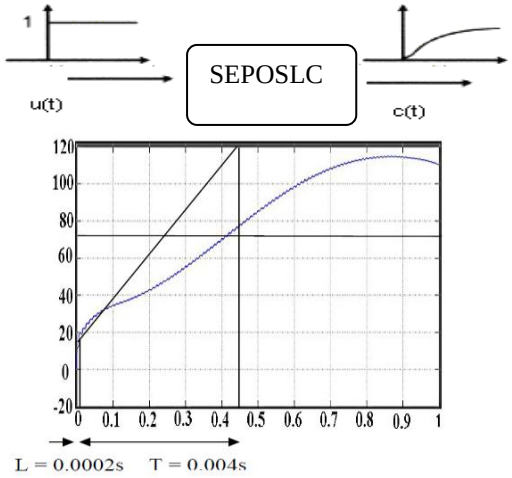


Figure 4. S- Shaped curve of open loop response of SEPOSLC

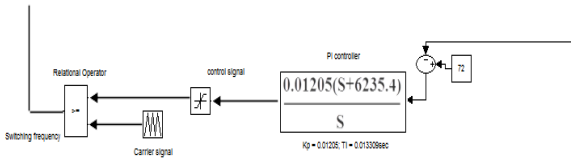


Figure 5. Simulink simulation model of PI control

The PI control optimal setting values (Kp and Ti) are obtained by finding the minimum values of integral of square of error (ISE), integral of time of square of error (ITAE) and integral of absolute of error (IAE), which is listed in Table 1.

Table 1.**Simulated Results Of Minimum Values Of Ise, Iae, Itae And Optimal Setting Values Of Kp And Ti**

ISE	IAE	ITAE	K_p	T_i (s)
0.00154	0.0154	0.3059	0.01205	0.0133

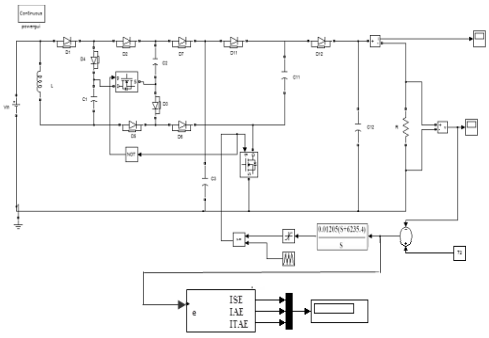


Figure 6. Simulation model of PI control with split capacitor type elementary additional series positive output super lift converter

4. Design of Sliding Mode Control

SMC is a non-linear control which complies with the non-linear structure of switch mode power supply. The control topology consists of a linear and non-linear part. The non-linear parameter can be selected, while it is left to the designer to tune the linear part and get the optimum values depending on the application. Figure 6 shows the control structure of SMC. It consists of two control loops, the output voltage is subtracted from the reference voltage and the difference is passed through an integral action. The output of the integral is amplified through a gain and the result is subtracted from the inductor loop, the difference is passed through a hysteresis. One major drawback of this model is the lack of a standard procedure to select the gain. The hysteresis parameter can be selected by measuring the peak-to-peak inductor current and these are the limits for the hysteresis parameters.

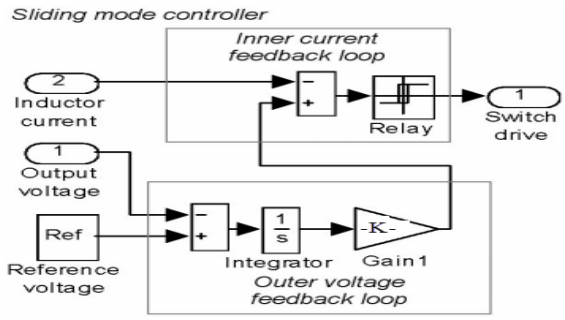


Figure 7. The simulation controller block diagram. Controller includes the current controller (inner loop) and the voltage control loop (PI-control), where together they present SMC

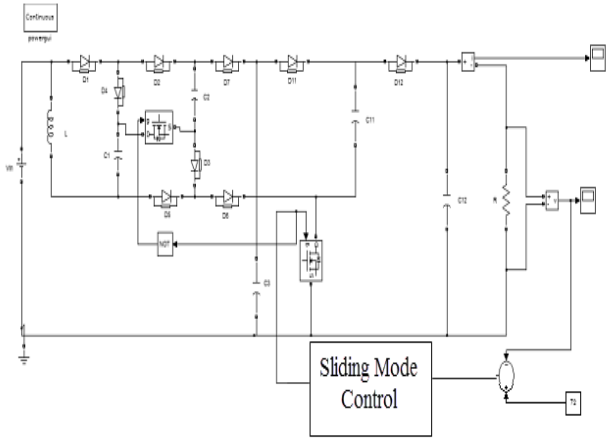


Figure 8. Simulation model of SMC control with split capacitor type elementary additional series positive output super lift converter

5. Simulation Results

The validation of the system performance is done for five regions viz. transient region, line variations, load variations, steady state region and also component variations.

Table 2.Parameters Of Split Capacitor Type Elementary Additional Series Positive Output Super Lift Converter

Parameters Name	Symbol	Value
Input Voltage	V_{in}	12V
Output Voltage	V_o	72V
Inductor	L	100µH
Capacitors	C_1 to C_5	30µF
Nominal switching frequency	fs	100kHz
Load Resistance	R	50Ω
Range of duty cycle	k	0.3 to 0.9
Desired duty cycle	k	0.5

5.1. Transient Region

Figure 9 shows the output voltage and the inductor current of PI with POESLLC in the transient region. It can be found that the converter output voltage and inductor current has a negligible overshoot and settled at time of 0.037 s in this region with designed PI control.

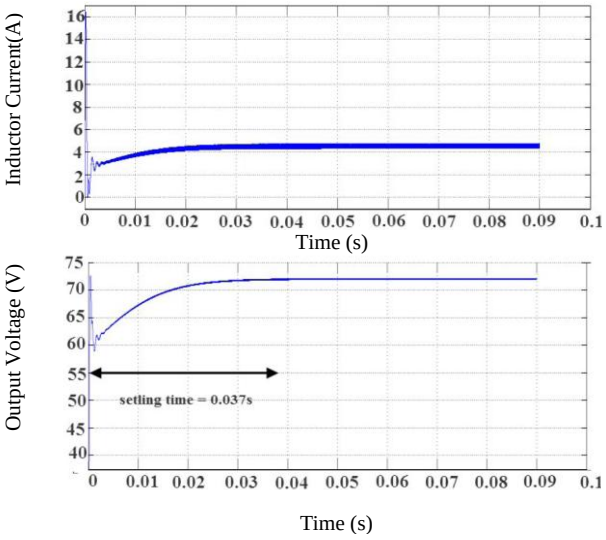


Figure 9. Inductor current and Output voltage in a transient region with PI Control

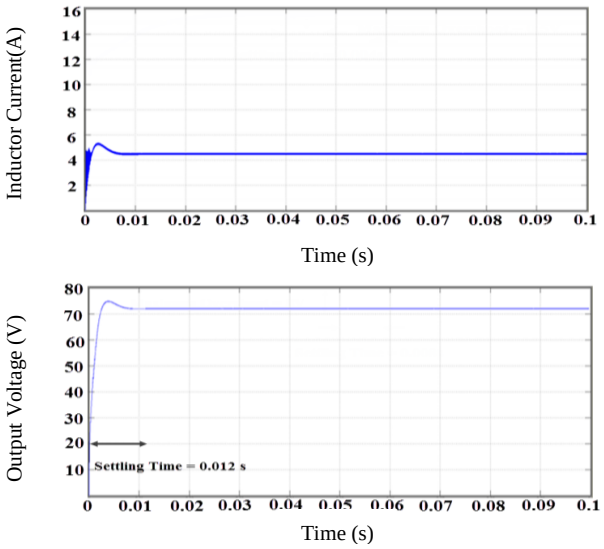


Figure 10. Inductor current and Output voltage in a transient region with SMC Control

Figure 10 shows the output voltage and the inductor current of SMC with POESLLC in the transient region. It can be found that the converter output voltage and inductor current has a negligible overshoot and settled at time of 0.012 s in this region with designed SMC control

Table 3.Output Voltage And Inductor Current Of Poesllc Converter Parameters With Both Pi And Smc In Transient Region

	PI Control		SMC Control	
	Settling time	Maximum overshoot	Settling time	Maximum overshoot
Output voltage	0.037s	No	0.012s	No
Inductor current	0.037s	0.55 A	0.012s	0.15 A

Table 3 shows the comparison between the two models in transient region. The output voltage of POSELLC converter with PI has no overshoot, while the output voltage of the same converter with SMC has no overshoot. The gain of the output voltage with SMC can be reduced by increasing the gain but it will increase the settling time. The graphs show that the settling time with PI is longer. For POSELLC converter with SMC, the settling time is shorter but the inductor current has much less overshoot. SMC has shorter settling time in this region the inductor current has much less overshoot.

5.2. Line Variations

In Figure 11 shows the variation of output voltage of PI control with split capacitor type positive output elementary additional series positive output super lift converter for the input voltage step change from 12 V to 9V (- 30 % line disturbance). It can be found that converter output voltage has a maximum overshoot of 16 V and 0.02 s settling time with designed PI control. In Figure 12 shows the variation of output voltage of PI control with split capacitor type elementary additional series positive output super lift converter for the input voltage step change from 12 V to 15V (+ 30 % line disturbance). It can be found that converter output voltage has a maximum overshoot of 18 V and 0.028 s settling time with designed PI control.

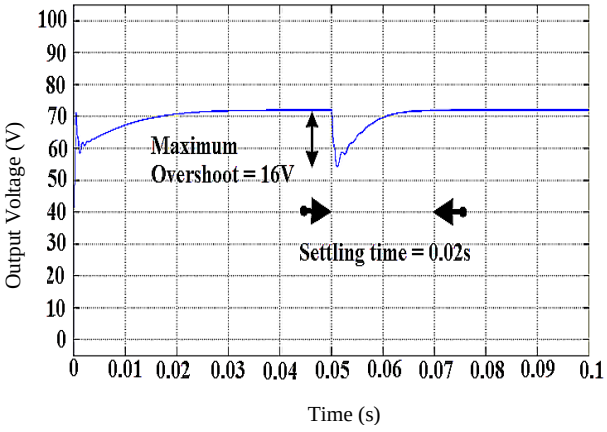


Figure 11. Output voltage when input takes a step change from 12 V to 9 V with PI control

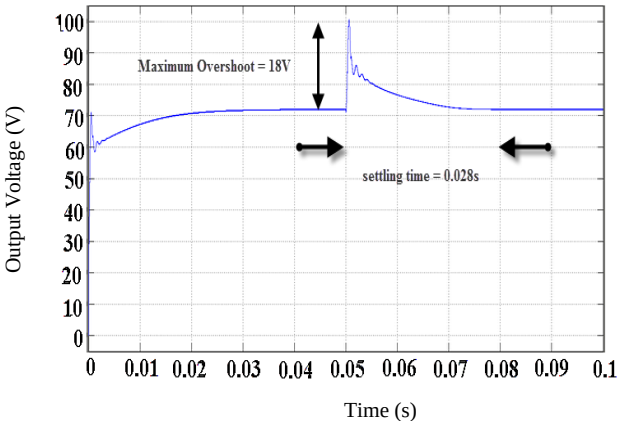


Figure 12. Output voltage when input takes a step change from 12 V to 15 V using PI control

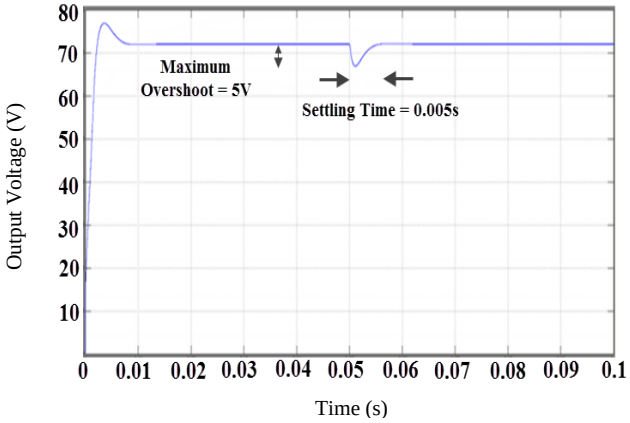


Figure 13. Output voltage when input takes a step change from 12 V to 9 V using SMC control

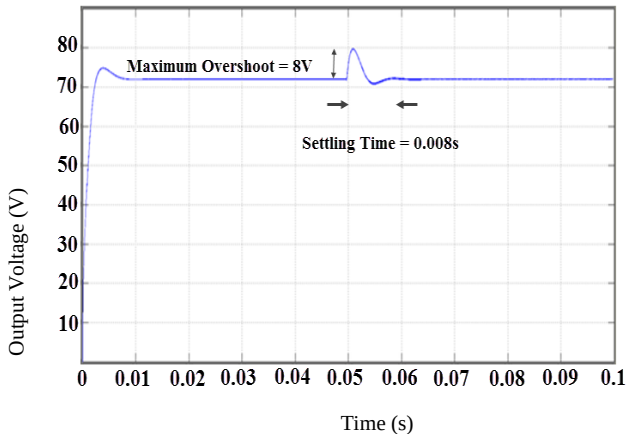


Figure 14. Output voltage when input takes a step change from 12 V to 15 V with SMC control

In Figure 13 shows the variation of output voltage of SMC control with split capacitor type positive output elementary additional series positive output super lift converter for the input voltage step change from 12 V to 9V (- 30 % line disturbance). It can be found that converter output voltage has a maximum overshoot of 5 V and 0.005 s settling time with designed SMC control. In Figure 14 shows the variation of output voltage of SMC control with split capacitor type elementary additional series positive output super lift converter for the input voltage step change from 12 V to 15V (+ 30 % line disturbance). It can be found that converter output voltage has a maximum overshoot of 8 V and 0.008 s settling time with designed SMC control. The POSELLC converter model with SMC has almost negligible effect. It shows that SMC has a strong immunity against line variation disturbances, and has better performance than PI control in this region.

Table 4.Output Voltage Of Poesllc Converter Parameters With Both Pi And Smc In Line Variation

	PI Control		SMC Control	
	Settling time	Maximum overshoot	Settling time	Maximum overshoot
Output Voltage (12 Vto 9 V)	0.02s	16 V	0.005s	5 V
Output Voltage (12 Vto 15 V)	0.028s	18 V	0.008s	8 V

5.3. Load Variations

Figure 15 shows variation of output voltage with step change in load from 50 Ω to 60 Ω (+ 20 % load disturbance) using PI control. It could be seen that there is a small overshoot of 0.5V and steady state reached with a very less time of 0.003 s.

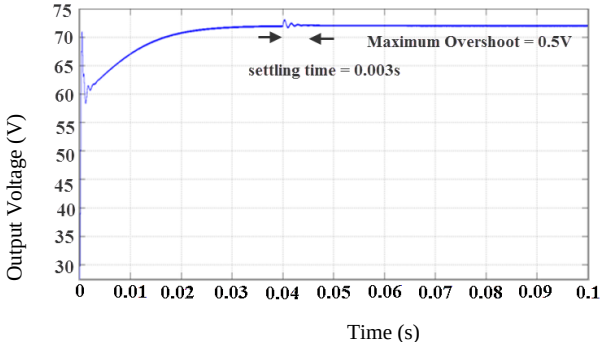


Figure 15. Output voltage when load resistance makes a step changes from 50 Ω to 60 Ω using PI control

In Figure 16 shows another variation of output voltage with step change in load from 50 Ω to 40 Ω (- 20 % load disturbance) using PI control. It could be seen that there is a small overshoot of 0.5 V and steady state reached with very small time of 0.004 s.

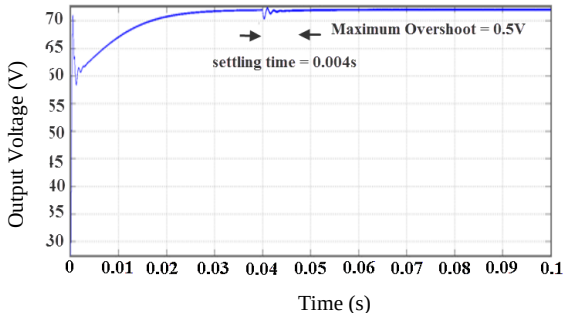
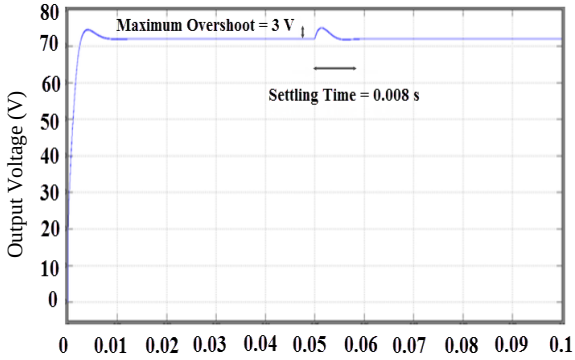


Figure 16. Output voltage when load resistance



makes a step changes from 50 Ω to 40 Ω using PI control.

Figure 17 Output voltage when load resistance makes a step changes from 50 Ω to 60 Ω using SMC control

Figure 17 shows the variation of output voltage with the step change in load from 50 Ω to 60 Ω (+ 20 % load disturbance) using SMC control. It could be seen that there is a overshoot of 3 V and steady state is reached with a very less time of 0.008 s

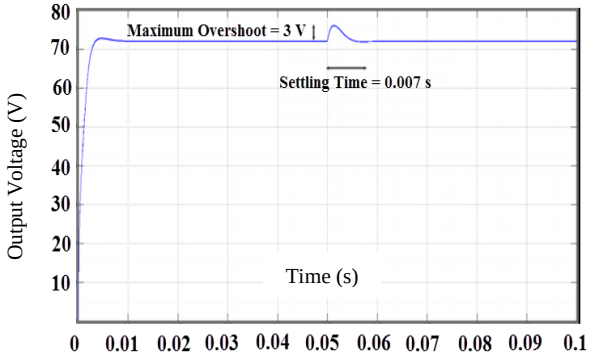


Figure 18. Output voltages when load resistance makes a step changes from 50 Ω to 40 Ω using SMC control

In Figure 18 shows another variation of output voltage with step change in load from 50 Ω to 40 Ω (- 20 % load disturbance) using SMC control. It could be seen that there is a overshoot of 3 V and steady state is reached with a very small time of 0.007 s.

Table 5.Output Voltage Of Poesllc Converter Parameters With Both Pi And Smc In Load Variation

5.4. Steady State Region

Figure 19 shows the instantaneous output voltage and current of the inductor current in the steady state It is evident from the figure that the output voltage ripple is very small about 0.45V and the peak to peak inductor current is 0.55A while the switching frequency is 100 kHz.(using PI control)

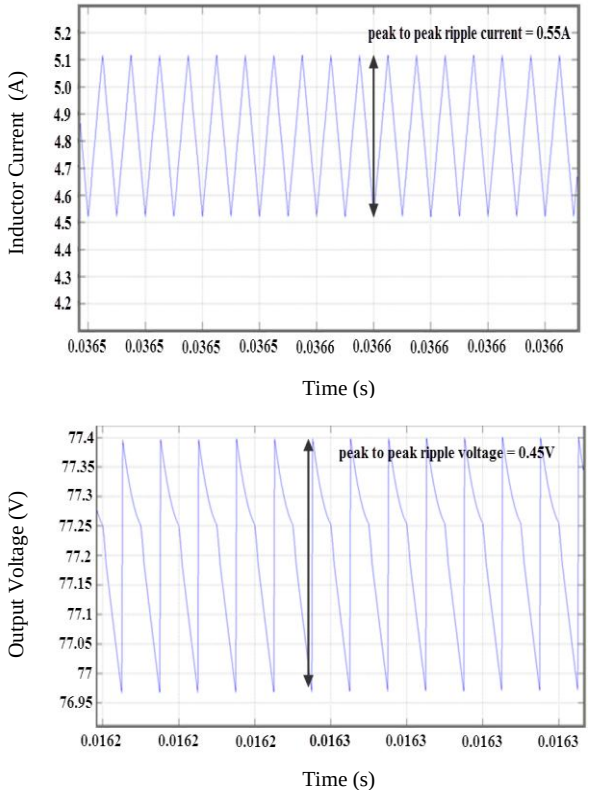


Figure 19. Output voltage and inductor current in steady state region using PI control

Table 6.Output Voltage And Inductor Current Of Poesllc Converter Parameters With Both Pi And Smc In Load Variation

	PI Control		SMC Control	
	Peak to Peak ripple current	Peak to Peak ripple voltage	Peak to Peak ripple current	Peak to Peak ripple voltage
Output voltage		0.45 V		0.11 V
Inductor current	0.55 A		0.15 A	

	PI Control		SMC Control	
	Settling time	Maximum overshoot	Settling time	Maximum overshoot
Output Voltage 50 Ω to 60 Ω	0.003s	0.5 V	0.008s	3 V
Output Voltage 50 Ω to 40 Ω	0.004s	0.5 V	0.007s	3 V

Figure 20 shows the instantaneous output voltage and current of the inductor current in the steady state It is evident from the figure that the output voltage ripple is very small about 0.11V and the peak to peak inductor current is 0.15A while the switching frequency is 100 kHz.(using SMC control)

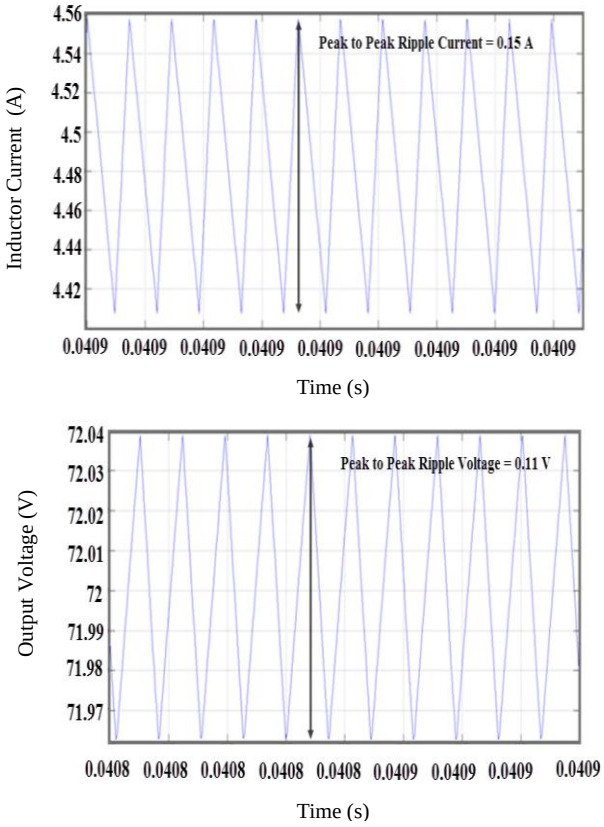


Figure 20. Output voltage and inductor current in steady state region using SMC control

5.5. Circuit Components Variations

An interesting result has been illustrated in Figure 21, which shows response for the variation in capacitor value from 30 µF to 120 µF. There is no wide variation in the output peak overshoot and settling time. The capacitor change has no severe effect on the steady state voltage across the load. In

Figure 22 shows the output voltage for inductor variation from 100 µH to 300 µH and the change has no severe effect on the converter behavior due to the efficient developed PI control.

An interesting result has been illustrated in Figure 23, which shows response for the variation in capacitor value from 30 µF to 120 µF. There is no wide variation in the output peak overshoot and settling time. The capacitor change has no severe effect on the steady state voltage across the load. In Figure 24 shows the output voltage for inductor variation from 100 µH to 300 µH and the change has no severe effect on the converter behavior due to the efficient developed SMC control.

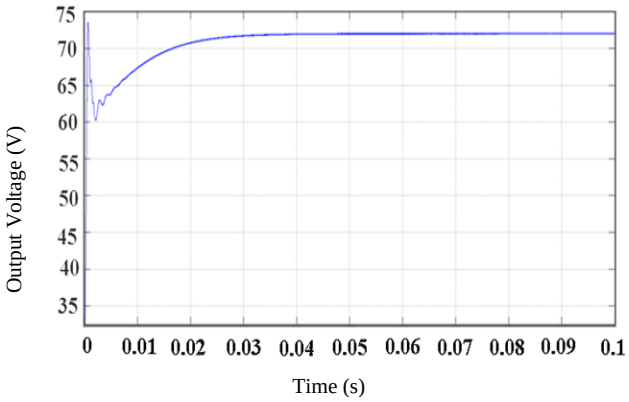


Figure 21. Output voltage when capacitors variation from 30 µF to 120µF

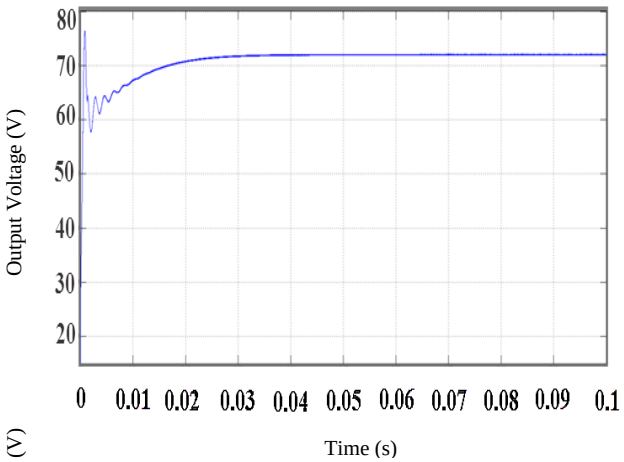


Figure 22. Output voltage when inductor varies from 100 µH to 300 µH

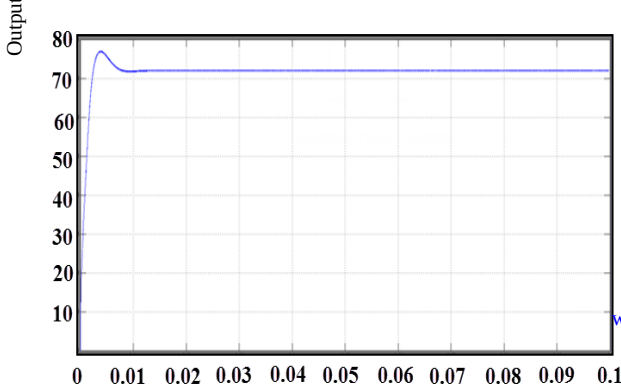


Figure 23. Output voltage when capacitors variation from 30 µF to 120µF

An interesting result has been illustrated in Figure 23, which shows response for the variation in capacitor value from 30 µF to 120 µF. There is no wide variation in the output peak overshoot and settling time. The capacitor change has no severe effect on the steady state voltage across the load. In Figure 24 shows the output voltage for inductor variation from 100 µH to 300 µH and the change has no severe effect on the converter behavior due to the efficient developed SMC control.

6. Comparison of Output Voltage in Various Topologies of DC/DC Converters

Table 3 shows the comparison of voltage transfer gain for different topologies of DC / DC converter with a varying duty cycle for an input voltage of 12 V. Graphical representation of output voltage versus duty cycle for different topology of DC / DC converter are shown in Fig 25.

Table 7.Comparison Of Voltage Transfer Gain In Various Topologies Of Dc/Dc Converters

	Duty Cycle				
Types of Converters	0.5	0.6	0.7	0.8	0.9
Boost Converter	2	2.5	3.33	5	10
Positive Output Super lift Elementary main series converter	3	3.5	4.33	6	11
Positive Output Super lift Elementary additional series converter	5	6	7.66	11	21

Split Capacitor type positive output elementary additional series super lift converter	6	7	8.66	12	22

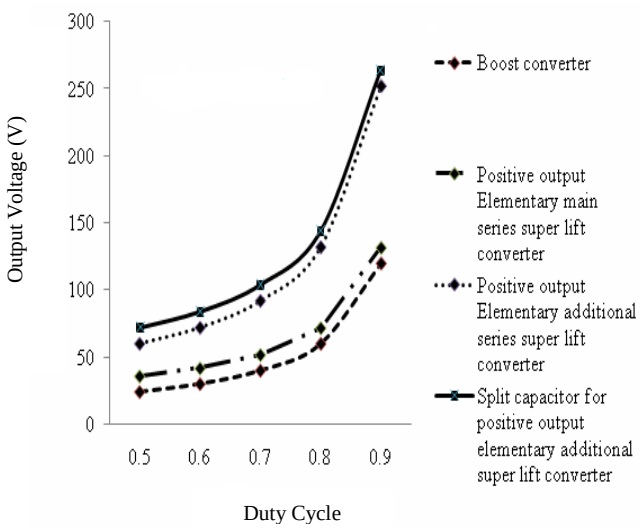


Figure 25. Graphical representation of output voltage Vs duty cycle in various topologies of DC/DC converters

7. Conclusions

The split capacitor type elementary additional series positive output super lift converter was tested in steady state region, transient region (turn on), under line variation, and under load variation. These tests where done for the POSELLC converter using two different control techniques, the traditional PI control and the SMC. In steady state both models showed similar characteristics. For dynamic tests the SMC showed to be more efficient against disturbances than the PI control. The settling time was longer in case of SMC also a higher output voltage overshoot. On the other hand, the inductor current didn't have high overshot while it had high inductor current overshoot with PI control. The reduced current overshoot is due to the additional inductor current feedback. The SMC is showing a promising future in the application of switch mode power supply because it is a non linear control and can evaluate the non linearity of the converter components. Second, it isn't operating at a constant switching frequency. Third, it's easer to design a converter with SMC than PI control.

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