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Hybrid Three Step Damping Compensator For a DC-DC Boost Converter

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***Abstract*—This paper presents a new hybrid three step damping compensator (HTSDC)for a DC-DC Boost converter. HTSDC is a feedforward compensator which removes overshoot in the step response of a lightly damped system. However the conventional control technique is very sensitive to variations in natural frequency of oscillations in the system. In order to reduce this undesirable sensitivity of system HTSDC is proposed which is operated with in the feedback loop of the system. Design of the three step damping compensator is independent of computational delay. The performance of HTSDC for BC has been investigated through simulation using MATLAB/Simulink.**

Keywords:* Hybrid three step damping compensator (HTSDC), *BC – Boost Converter, CCM (Continuous Conduction Mode).

I. INTRODUCTION

The output voltage of a DC-DC Boost Converter (BC) is controlled or regulated by using feedback control system. The converter is nonlinear lightly damped dynamics, which are described as a function of load parameters, duty cycle and make the control design difficult and challenging one [1]. Advances in signal processing technology have spurred research in new control techniques to improve converter control [3]. In this paper, a new control technique based on the **TSDC** principle is employed. Classical Posicast is a feed forward control method for lightly damped systems [2]. It has the potential to remove the oscillatory response of a lightly damped system, but the drawback is sensitivity to model uncertainty [I]. The TSDC approach can be more useful if the parametric sensitivity can be reduced. The drawback is removed by using the TSDC in a feedback loop; this reduces the sensitivity to parameter variations [5]. Research has shown that Proportional-Integral-Derivative (PID) based control of the power converter may require additional algorithm modifications to achieve a combination of good transient and steady-state performances [6]. The design of a HTSDC for a DC-DC BC operated in CCM described in this paper, which produces many of the beneficial closed loop effects over the traditional PID based controller, such as (i) good steady state and transient state performances, (ii) good damping of resonant behavior, (iii) controller gain parameters are very easy to determine, (iv) control method produces a very good response that is predictable by the small-signal averaged continuous time model (v) the key element of the PC structure is especially easy to implement in discrete-time hardware, and, (vi) the damping effect of TSDC removes the need for multiple sets of controller gains. The proposed control method does not require any of the additional modifications described earlier for PID control (dead zone, additional filtering, gain scheduling). The state space average modeling of a DC-DC converter well reported in [8]-[11]. Small signal Model with parasitic elements is also derived for the DC-DC converter in [3]-[4]. A classical TSDC has superior damping qualities, reduced sensitivity to parametric uncertainty and load change through feedback. Section II provides mathematical modeling of a DC-DC BC. Section III develops the design of Three Step Damping compensator.

II. MODELLING OF DC-DC BOOST CONVERTER

A. State Space Analysis

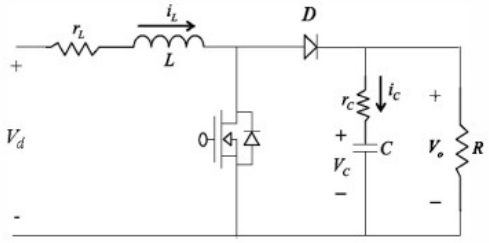

Fig. I. DC-DC Boost Converter.

Fig. I shows the circuit of DC-DC Boost Converter. It includes Vd DC input supply voltage (u), capacitor C, input inductor L, power switch (n-channel MOSFET) S, freewheeling diode D, duty cycle d , Vo output voltage (y) and load resistance R. In the description of the converter operation, it is assumed that all the components are ideal and also the DC-DC BC operated in a CCM. Figs. 2 and 3 shows the modes of operation of the DC-DC BC. The State-Space variables: Let x_1 (i_L) and X2 (V c) be the two state variables corresponding to the inductor current and capacitor voltage of DC-DC BC in fig 1.

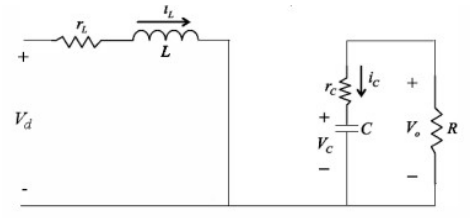

Fig 2. DC-DC Boost Converter during switch ON period.

In Fig. 2 when the switch S is closed, inductor current iL rises quite linearly, diode current D is reverse polarized, and capacitor C supplies the energy to output stage. Now, the system state-space equations during switch OFF time period

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = A\begin{bmatrix} i_L \\ V_C \end{bmatrix} + Bu$$

$$\begin{cases} \dot{X}_1 = \frac{di_L}{dt} = \frac{V_d - i_L r_L}{L} \\ \dot{X}_2 = \frac{dV_C}{dt} = -\frac{V_C}{(R + r_C)C} \end{cases} \quad (1)$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = A_1\begin{bmatrix} i_L \\ V_c \end{bmatrix} + B_1 u$$

$$V_O = C_1\begin{bmatrix} i_L \\ V_c \end{bmatrix}$$

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \end{bmatrix} = \begin{bmatrix} r_L & 0 \\ 0 & \frac{-1}{(R + r_C)C} \end{bmatrix}\begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} u \quad (3)$$

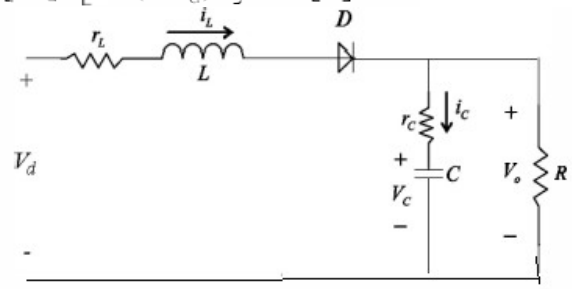

Fig3. DC-DC Boost Converter during switch OFF period.

In Fig. 3 when the switch S is open, inductor current iL is forced to flow through the diode D, capacitor C and load resistance R. The current iL decrease while capacitor is recharged. Now, the system state-space equations during switch OFF time period are

$$\begin{cases} \dot{X}_1 = \frac{di_L}{dt} = \frac{V_d - i_L r_C - V_O}{L} \\ V_O = \frac{V_C + i_L r_C}{(1 + \frac{r_C}{R})} \end{cases} \quad (4)$$

$$\begin{cases} \dot{X}_2 = \frac{dV_C}{dt} = \left(\frac{i_L - \frac{V_O}{R}}{C}\right) \\ \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = A_2\begin{bmatrix} i_L \\ V_c \end{bmatrix} + B_2 u \end{cases} \quad (5)$$

$$V_O = C_2\begin{bmatrix} i_L \\ V_c \end{bmatrix}$$

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \end{bmatrix} = \begin{bmatrix} \frac{-r_C}{L} & -\frac{r_C}{L(1+\frac{r_C}{R})} & \frac{-1}{(1+\frac{r_C}{R})} \\ \frac{\left(1 - \frac{r_C}{R(1+\frac{r_C}{R})}\right)}{C} & & \frac{-1}{CR(1+\frac{r_C}{R})} \end{bmatrix}\begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} u \quad (6)$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = A\begin{bmatrix} i_L \\ V_C \end{bmatrix} + Bu \quad (7)$$

$$V_O = C\begin{bmatrix} i_L \\ V_C \end{bmatrix}$$

Where

$$A = dA_1 + (1-d)A_2$$
$$B = dB_1 + (1-d)B_2$$
$$C = dC_1 + (1-d)C_2$$

The converter model includes parasitic elements and the boost converter parameters are Load resistance(R)-50 Ω,filter inductance(L)-100µH,filter capacitance(C)-30µF,effective series resistance of the inductor(r_L)-0.176 Ω, effective series resistance of the capacitor(r_C)-0.12 Ω,Damped natural period(T_d)-2.44ms,switching frequency(f_s)-100 KHZ ,input voltage(V_d)-12V,output voltage(Vo)-36V. For an input of 12V the output is 36V, the response is shown in Fig. 4. In the open loop response, the overshoot is high, the settling time is very high, and the response is oscillatory. The proposed control strategy is able to reduces the peak overshoot and reduce the settling time.

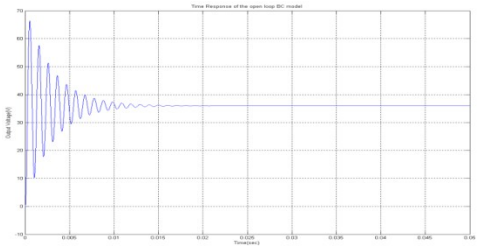

Fig 4.open loop response

III. DESIGN OF THREE STEP DAMPING COMPENSATOR

A. *Three Step Damping compensator*

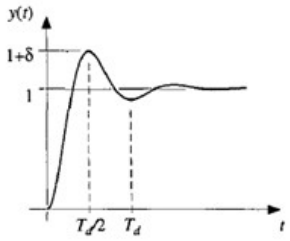

Fig 5.Step response of damped system

The step response is shown in Fig. 5. The response is characterized by damped time response period Td.

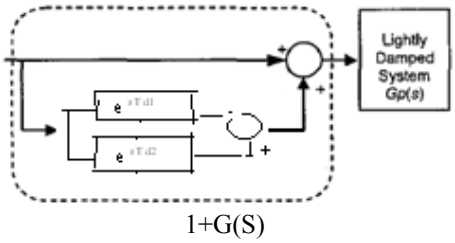

Fig 6. Three Step Damping compensator

The block diagram shown in Fig. 6 describes the structure of a classical three step damping compensator" . A classical TSDC is designed using knowledge of the step response overshoot and damped time response period T_d. Accurate knowledge of the step response parameters yields a compensator whose lowest frequency zeros cancel the dominant plant pair. The new hybrid control system structure is shown in fig 7.
The TSDC function is given by
$G_1(S)=(e^{-sTd1} + e^{-sTd2}), T_{d2}=2T_{d1}=T_d/3$

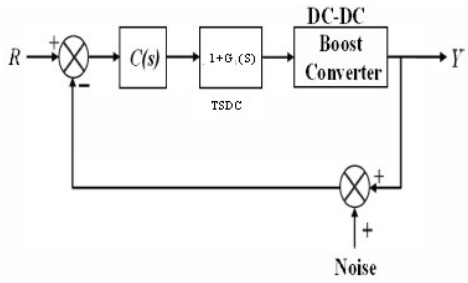

Fig 7.proposed Hybrid Feedback control using TSDC

Parameters of function $G_1(S)$ is step response of the damped response period T_d. The TSDC essentially reshapes the reference signal into three parts; initially the controller subtracts the scales amount from the reference signal, so that the peak of a lightly damped response coincides with the desired final value of the system response. The time to the peak of the step response is one third the natural damped periods. After this delay, the full value of the step reference is applied to the system G(s) so that the output remains at the desired final value.

B. *TSDC Modeling*

The key elements of the function G(S) are the scaling factor parameterized by and the time delay element parameterized by T_d. The design method for the proposed control system has two steps. First, the function G(S) is designed for the BC using (3-6). Next, the controller C(s) is designed to compensate the combined model [1 +G(S)] Gp(s). Classical frequency domain techniques are used. To counteract steady state disturbances, a pure integrator type compensator has been found suitable for the BC,
C(S)=K/s (8). The gain K is chosen as large as possible to minimize the settling time, but not so large that the overshoot is excessive. The complete hybrid controller transfer function is described by combining the compensator C(s) and the TSDC transfer function as,
$C(S)\ 1+G_1(S) = K/s\ [1+e^{-sTd1} + e^{-sTd2}]$ (9)

C. *TSDC Controller*

The key elements of function G(S) is the time delay element parameterized by T_d.
General small signal model transfer function is

$$\frac{\hat{v}_o}{\hat{d}} = C[SI - A]^{-1}\left[[A_1 - A_2]X + [B_1 - B_2]V_d\right] + [C_1 - C_2]X \quad (10)$$

By substituting (3) and (6) in above equation to obtain the transfer function of DC-DC BC is

$$G(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{1950479(1 - 1.8365e-5s)}{(s^2 + 666.67s + 2.7548e-8)} \quad (11)$$

Undamped natural frequency

$$\omega_n = \sqrt{\frac{1}{LC}} \quad (12)$$

Damped time response period

$$T_d = \frac{2\pi}{\omega_n\sqrt{1-\zeta^2}} \quad (13)$$

Controller parameter are T_d = l.le-4 .The gain K is chosen as large as possible to minimize the settling time, but not so large that the overshoot is excessive and it is chosen to be K = 7 in this paper. The resulting transfer function of the hybrid TSDC

Mathematically, the three-step compensators can be expressed as:
S-Domain Representation

$$1+G_1(jw) = 1 + (-e^{-sT_{d1}} + e^{-sT_{d2}}); \quad T_{d2} = 2T_{d1} = T_d/3, \quad (14)$$

Steady-State Representation

$$1+G_1(jw) = \{1 - \cos(\omega T_{d1}) + \cos(\omega T_{d2})\} + j\{\sin(\omega T_{d1}) - \sin(\omega T_{d2})\} \quad (15)$$

where T_{d1} and $_{d2}$ denote time delays, whose expressions are derived in [14] by formulating empirical differential

equations. The formulation of empirical equations however does not visually illustrate the effect of (14) that the effectiveness of the presented damping techniques depends on the correct tuning of T_d.

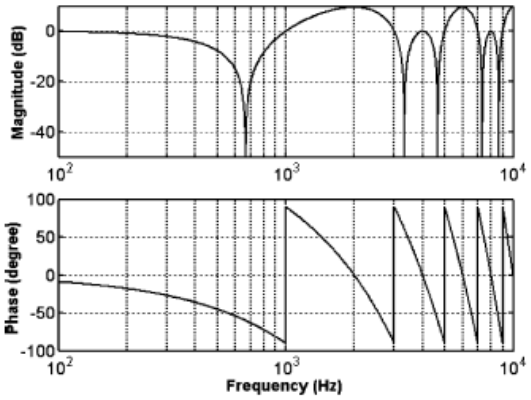

Fig 8.Bode plot of three-step compensator

A careful evaluation of the technique parametric sensitivities is therefore necessary, and can be mathematically performed by (15) for three-step damping, as follows.

$1+G_1(jw) = K$

$$K = \sqrt{\{1-\cos(\omega T_{d1})+\cos(\omega T_{d2})\}^2+\{\sin(\omega T_{d1})-\sin(\omega T_{d2})\}^2}$$
$$\sqrt{\{1-\cos(\omega T_{d1})+\cos(\omega T_{d2})\}^2+\{\sin(\omega T_{d1})-\sin(\omega T_{d2})\}^2} \quad (16)$$

IV. Design of PID Controller

The conventional controllers based on the PID approach are commonly used for DC-DC BC applications [6]. Power converters have relatively low order dynamics that can be well controlled by the PID Controller method [6] , [12]. The transfer function of the PID Controller is

$G_C(s)=0.2+500 / s + 0.95s$

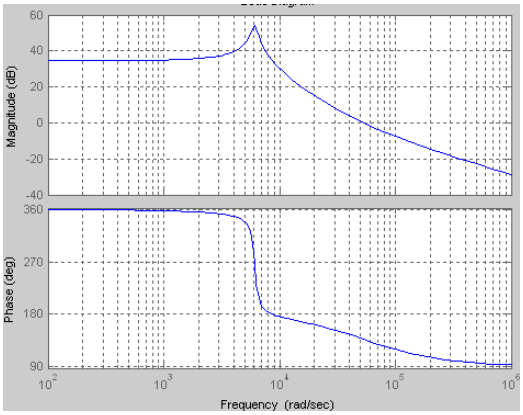

Fig.9 Frequency Response of PID Compensated system.

A. Comparison with PID control

Comparing the proposed TSDC based control to classical PID control yields useful insights. For the same phase margin, however, the TSDC compensated magnitude response is significantly suppressed at higher frequencies compared to that of the PID-compensated system. Therefore, theTSDCcompensated system suppresses high frequency noise much better than the PID approach. For identical phase margins, the TSDC compensated approach yields a larger gain margin.

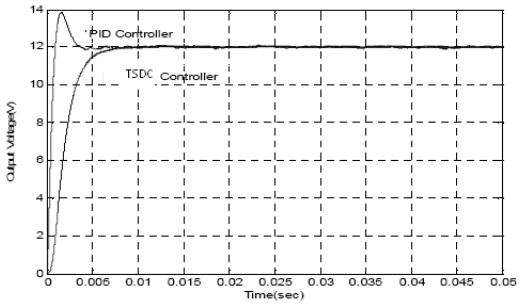

Fig 10 Comparision of PID and TSDC Controllers

V. Simulation Results

A. Line Variation

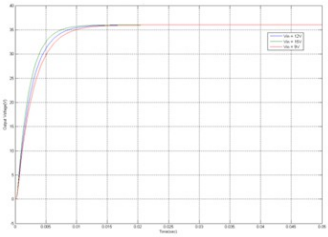

Fig. 11. Response of output voltage of a DC-DC BC for various input voltage using HTSDC

B .Load variations

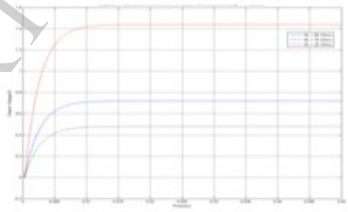

Fig. 12. Response of load current of a DC-DC BC for various load resistances using HTSDC controller

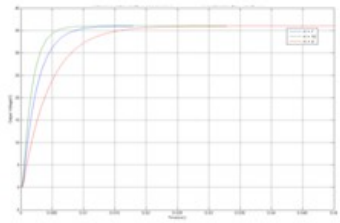

Fig. 13. Response of output voltage of a DC-DC BC for various values of compensator gain K using HTSDC controller

C. Controller Parameters Variations

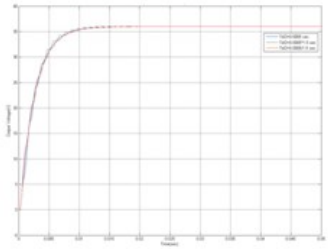

Fig. 14. Response of output voltage of a DC-DC BC using HTSDC for various time delay.

VI. CONCLUSION

The output voltage regulation of a DC-DC BC operated in CCM using htsdc has been successfully demonstrated through the MatLab/Simulink simulation in this paper. The control technique uses a TSDC element within the feedback control system to take benefit of TSDC superior damping qualities. The TSDC element parameters T_d can be directly computed from the analytical, ideal method, ideal method of a DC-DC BC converters. An integral compensator with a single gain K is used with the TSDC element to ensure the proper steady state response operation. Compared to PID controller, the proposed method has compensator gain K to tune the system. The simulation results are showed that the HTSDC is an effective approach for a DC-DC BC converter output voltage regulation over the PID controller scheme. It is suitable for common DC-DC conversion process, medical equipments and computer hardware parts. In future the HTSDC should be developed to study the parallel operation of DC-DC BC is further.

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