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Highly Stable and Adaptive All-Digital PLL for Fast Synchronization

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***Abstract* -This thesis presents the design and implementation of the All Digital Phase-Locked Loop circuit in Verilog HDL. The presented All Digital Phase-Locked Loop circuit uses a Digital Controlled Oscillator built on NAND elements and a 2-level Time-to-Digital Converter based on pulsed latches. Proposed TDC based on pulsed latches is a good choice for Low Power and area-efficient circuits. Timing problems in pulsed latches are solved by using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. Moreover, A combinational frequency multiplier can be developed and tested. And using only one low-frequency reference oscillator we can design a complete integrated system. This method will eliminate the main problem of the all-digital PLL systems which is the need for a high-frequency external clock signal for the DCO.**

Keywords— Voltage-controlled oscillator (VCO), frequency divider, phase-locked loop (PLL), Time-to-Digital Converter (TDC)

I. INTRODUCTION

Phase-locked loops are key circuits that are widely used in a variety of integrated devices, including communication system clock radio communication system frequency synthesizers. The all-digital phase-locked loop (ADPLL) uses a design based on standard library cells so that it can be easily integrated into a digital system. Besides, ADPLL is resistant to the process, voltage, and temperature (PVT) variations. The most important part of the digital PLL system is the Digitally Controlled Oscillator (DCO). It should cover the working frequency range with a small enough frequency step [1]. In most cases, the DCO is designed as a programmable frequency divider. To achieve a small enough frequency, an input frequency should be several times higher than the desired output frequency. This limitation is the main problem of the all-digital PLL systems [2]. The high input frequency to the DCO does not need to be with high stability. In most cases, a simple high-frequency RC oscillator is used for this purpose [3]. Although in some cases the complete integration of the oscillator is not possible and requires additional pins to the integrated circuit. For that purpose, a combinational frequency multiplier is developed and tested. Also, studies proved that Pulsed Laches helps in reducing area and power consumption when compared to Flip flops [4]. Multiple nonoverlap delayed pulsed clock signals can solve the timing problem between pulsed latches.

II. CONVENTIONAL ALL-DIGITAL PLL SYSTEM

All digital PLL has all digital elements, including the phase detector, loop filter & oscillator; they do not have the provision voltage limitations of analog PLLs. Advanced all-digital phase-locked loops also are fully synthesizable & customizable. All digital PLLs don't have the provision voltage limitations of their analog PLL and hybrid analog ("digital PLL") counterparts. they're also fully synthesizable, so that they are customized and implemented in processes across all foundries, moreover as non-standard process nodes during a fraction of the time of analog PLLs. Can flexibly operate at a large range of supply voltages, enabling design teams to cut back the facility consumption of the complete chip. ADPLL has more flexibility in supporting the lower supply voltage related to low-power designs. this can be because all digital circuit architectures don't require precise voltage/current biasing, and so aren't headroom limited. ADPLL takes small areas which will be up to 10 times smaller than their analog IP counterparts. This can be because they're not enthusiastic about the matching and passive elements required for analog implementations which are a dominant contributor to total area. All digital PLLs inherently have a way higher level of noise immunity than analog and hybrid analog implementations. All Digital Phase Locked Loops (ADPLLs) are more attractive than the Analog PLLs since they provide better flexibility and portability. Lock time is extremely important for portable or mobile applications since the PLL must support fast exit and entry from power management techniques. The ADPLLs has the characteristic of fast frequency locking, full digitization, and good stability. Several functional blocks form the Existing ADPLL Design [5]. It includes a Digital Phase Frequency Detector, TDC circuit, a decoder for the TDC circuit, a straightforward digital glitch filter, controller, DCO, and frequency divider. [5]

III. ARCHITECTURE PROPOSED METHOD

Fig. 1 shows the schematic of the proposed ADPLL Circuit. All-Digital PLL deals purely with a digital signal and hence offers various advantages compared to its analog counterpart. It has three main components with all its blocks digitalized. They are Digital Phase Frequency Detector, Digital Loop Filter (DLF), and Digital Controlled Oscillator (DCO) as given in [5]. Additionally, a Divide by N counter is used in the feedback path for frequency synthesis

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Applications. Basic Building Blocks of Proposed ADPLL are All Digital Phase Detector, Digital Loop Filter, Frequency Divider, Time-to-Digital Converter based on pulsed Latches, Control, Frequency Multiplier, and NAND based Digital Controlled Oscillator.

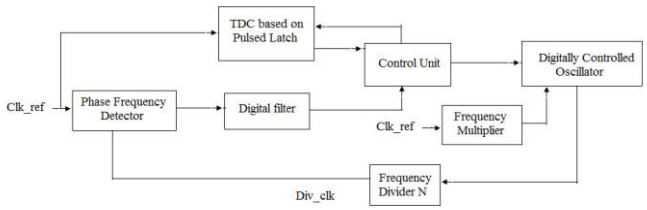

Fig. 1. Structural diagram of Proposed All-Digital PLL

A. Frequency Multiplier

To use only one external low-frequency oscillator the high-frequency clock for the DCO should be generated on the chip. To use standard digital logic circuits a combinational frequency multiplier is developed. Its working principle relies on a generation of a series of pulses on every edge of the input clock frequency. The circuit uses one 10 MHz external quartz reference oscillator. The frequency from the oscillator is divided by the coefficient M forming the input reference signal to the frequency-sensitive phase detector. The same frequency is applied to the input of the frequency multiplier where it is multiplied by the factor of 18 forming the clock frequency for the DCO. The signals from the phase detector are applied to the digital integrator and the time-to-code converter to form the integral and the proportional part of the control signal for the DCO.

B. TDC based on pulsed Latch

Fig. 2 shows the schematic of the proposed Time-To-Digital Converter based on a pulsed Latch.

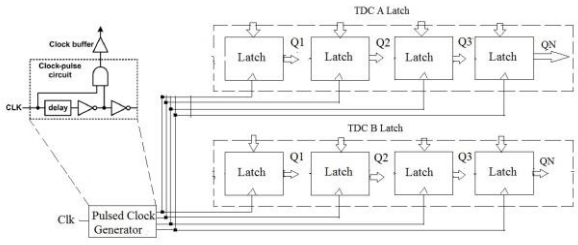

Fig. 2. TDC Based on Pulsed Latch

The TDC circuit converts timing information into digital code. The period of the reference clock can be calculated by dividing it into segments with a length equal to TDLY_UNIT.

Fig. 2 shows a two-level TDC circuit. Part A includes a chain of NA Big_Delay elements, and Flash TDC A. Part B includes a chain of NB Delay elements, Flash TDC B, and Path Mux for choosing a delay path from part A.

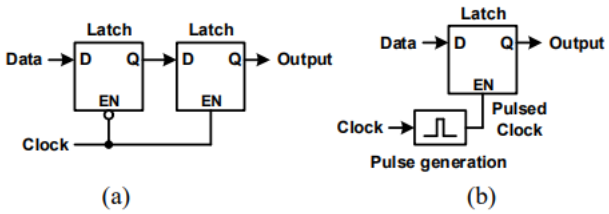

Fig. 3. (a) Master-slave flip-flop (b) Pulsed-latch

The conventional TDC uses master-slave D flip-flops consisting of two latches, shown in Fig. 3(a). Its area and power consumption are reduced by replacing the master-slave flip-flops with pulsed latches consisting of a latch and a pulsed clock signal, as shown in Fig. 3(b). We cannot use the pulsed latch directly in TDC because of the timing problem. One solution for the timing problem is to use multiple non-overlap delayed pulsed clock signals. The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal employed in its next latch. Therefore, each latch updates the information after its next latch updates the information. As a result, each latch contains a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.

IV. PERFORMANCE COMPARISON

a. Existing System

Performance Comparison of Existing and proposed systems is given in Fig. 4, 5, 6 & 7, 8, 9 respectively. Timing Summary of Existing system is given in Fig. 4. Device Utilization Summary of Existing System is given in Fig. 6. The Current (mA) and Power (mW) summary of the Existing system is given in Fig.6.

```
Timing Summary:
---------------
Speed Grade: -6

   Minimum period: 6.647ns (Maximum Frequency: 150.444MHz)
   Minimum input arrival time before clock: 6.462ns
   Maximum output required time after clock: 9.630ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk_ref'
  Clock period: 6.647ns (frequency: 150.444MHz)
  Total number of paths / destination ports: 161 / 28
-------------------------------------------------------------------------
Delay:               6.647ns (Levels of Logic = 1)
  Source:            u1/up_c_3 (FF)
  Destination:       crs_tune_0 (FF)
  Source Clock:      clk_ref rising
  Destination Clock: clk_ref rising

  Data Path: u1/up_c_3 to crs_tune_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
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Fig. 4. Timing Summary of Existing system

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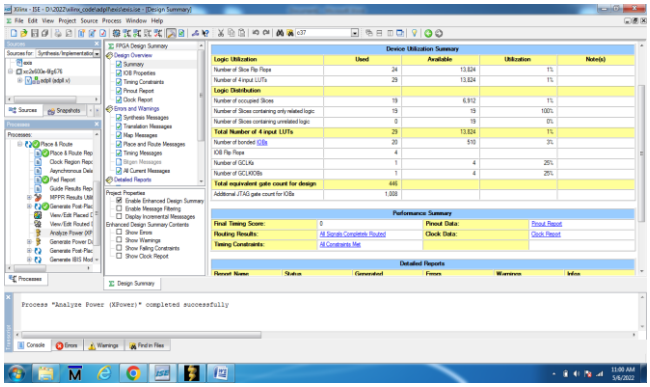

Fig. 5. Device Utilization Summary of Existing System

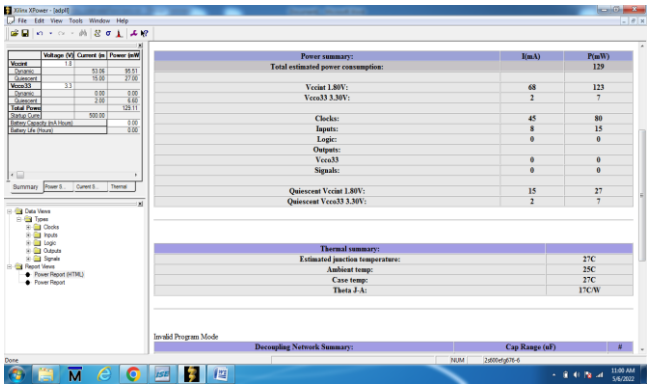

Fig.6. The Current (mA) and Power (mW) summary of the Existing system

b. *Proposed System*

The timing Summary of the Proposed system is given in Fig. 7. The device Utilization Summary of the Proposed system is given in Fig. 8. The proposed system's current (mA) and Power (mW) summary are given in Fig.9.

```
Timing Summary:
---------------
Speed Grade: -6

   Minimum period: 6.647ns (Maximum Frequency: 150.444MHz)
   Minimum input arrival time before clock: 6.462ns
   Maximum output required time after clock: 9.630ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk_ref'
  Clock period: 6.647ns (frequency: 150.444MHz)
  Total number of paths / destination ports: 161 / 28
-------------------------------------------------------------------------
Delay:               6.647ns (Levels of Logic = 1)
  Source:            u1/up_c_3 (FF)
  Destination:       crs_tune_0 (FF)
  Source Clock:      clk_ref rising
  Destination Clock: clk_ref rising

  Data Path: u1/up_c_3 to crs_tune_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

Fig.7. The timing Summary of the Proposed system

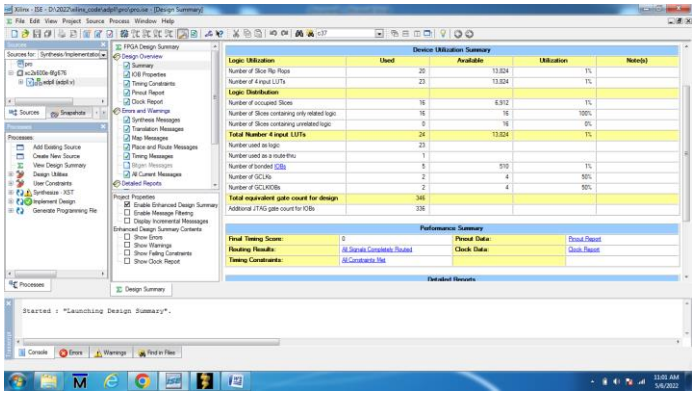

Fig.8. The device Utilization Summary of the Proposed system

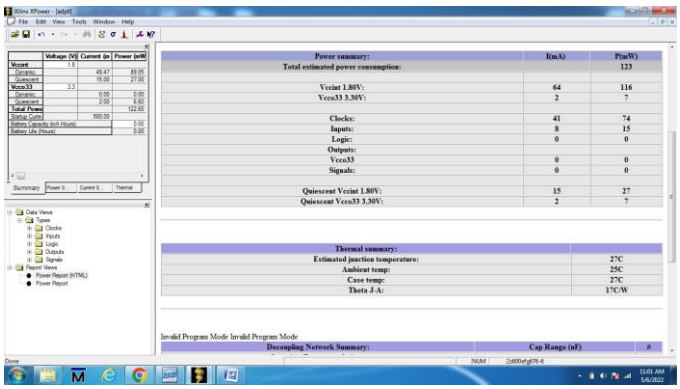

Fig.9. The Current (mA) and Power (mW) summary of the Proposed system

V. EXPERIMENTAL RESULTS

In this section, the proposed architecture of the ADPLL has been simulated and synthesized using Xilinx and ModelSim SE 6.3f. The complete simulation result of the ADPLL has been shown in Fig. 10. This result shows the improved performance of the proposed design.

a.

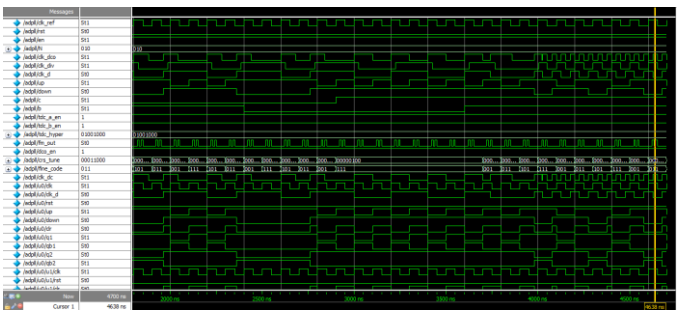

Fig.10. The complete simulation result of the ADPLL

Figure 11 shows the simulation result of the clock pulse generation unit of the Latch circuit used in TDC. Figure 12 shows the simulation results of the TDC Latch unit.

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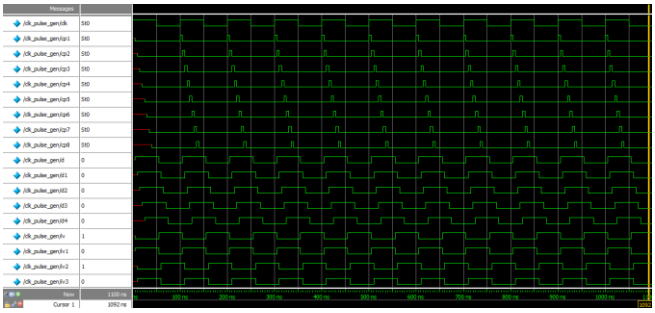

Fig.11. The simulation result of the clock pulse generation unit.

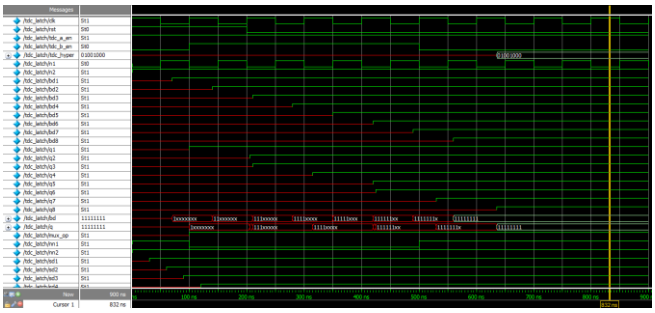

Fig.12. The simulation result of the TDC Latch Unit.

VI. CONCLUSIONS

The proposed an all-digital phase-locked loop (ADPLL)-with TDC based on pulsed latches and frequency multiplier is presented in this paper. Comparisons among existing systems and proposed systems are reported in detail. The design proposed offers superior performance in terms of area, locking time, and power consumption. The multiplication factor can be varied in a short locking time. The entire design is described in Verilog HDL and is synthesized and parameterized. Its use can significantly simplify the process of designing a timing circuit for SoC in digital flow. A new type of delay cell TDC can be designed, or the multiplication factor can be decreased to minimize the overall power consumption.

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