High Speed Multipliers and Complex Summers

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***Abstract*-Adders are basic digital circuits that perform binary addition. There are wide range of applications of adders depending upon the way they are implemented. Considering the fact that multiplication is successive addition, a multiplier is synthesised by multiplication of least significant bit (LSB) of multiplier with the multiplicand, binary addition of the product gives the result. Complex summers are designed by adding individual terms (real & imaginary) separately to give out the sum in terms of real and imaginary.**

Keywords- Adders, multiplier, summer, Xilinx tool

I. INTRODUCTION

Adders are of two kinds. Half adders and full adders, half adders are used when there are two inputs are of single bit. Full adders are used when there are three inputs of single bit. The truth table of half adder is shown in table1.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 1: Half adder truth table

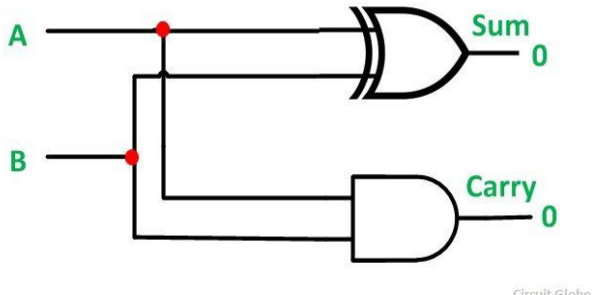

Figure 1: Half Adder circuit

The truth table of full adder is shown in table2.

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2: Full adder truth table

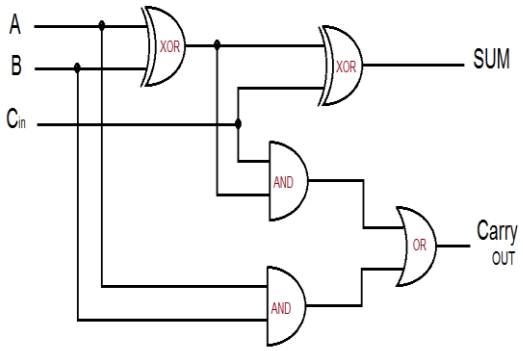

Figure 2: Full adder circuit

When the number of inputs increases the speed of calculation decreases. To improve the speed Carry Look Ahead adders are considered wherein the amount of time required to calculate the carry bit is less. A carry look adder uses the concept of generator and propagator. Its advantage is wide variety of applications (multiplier and complex summer) that can be realised and implemented on a suitable hardware. The major disadvantage is as the number of variables increases the complexity of the circuit increases. The circuit is costlier as it involves a greater number of hardware. Multiplication is considered as successive addition, based on this logic a multiplier is designed using a carry look ahead adder.

A. Carry look ahead adder

A carry look ahead adder circuit consists of full adders in cascade and carry generation circuit. Each full adder generates a sum, generator and propagator expression simultaneously without a delay. The generator and propagator of each full adder is taken for the calculation the carry bit. A generator and propagator are given by,

Consider two inputs A, B of size 1 bit. A generator is given by G (A, B) =A&B.

A propagator is given by P (A, B) =A^B.

These two equations are used for the calculation of the carry bit given by the formula -

$C_{i+1} = G_i + (P_i * C_i)$.

Consider i=0 then, $C_1=G_0+(P_0*C_0)$

i=1 then, $C_2=G_1+(P_1*C_1)$

i=2 then, $C_3=G_2+(P_2*C_2)$

i=3 then, $C_4=G_3+(P_3*C_0)$
i=4 then, $C_5=G_4+(P_4*C_4)$
i=5 then, $C_6=G_5+(P_5*C_5)$
i=6 then, $C_7=G_6+(P_6*C_6)$
i=7 then, $C_8=G_7+(P_7*C_7)$
i=8 then, $C_9=G_8+(P_8*C_8)$
Figure 3 shows the block diagram of Carry Look Ahead Adder.

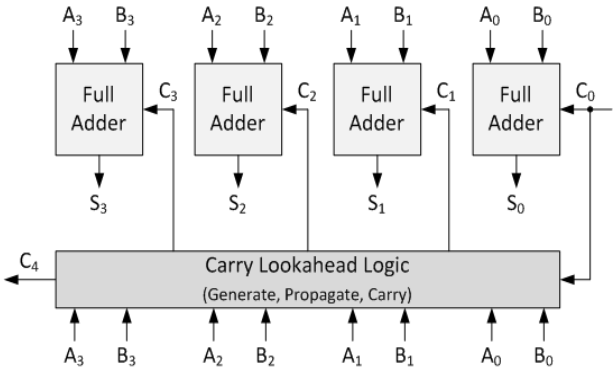

Figure 3: Block diagram of Carry Look AheadAdder

In carry look ahead adder's carry-in(C_0) is always initialised to zero.
Past findings- Carry look ahead adders were implemented for 4-bits, 8-bits, 16-bits, 32-bits and 64-bits. Multipliers were implemented for 8-bits, 16-bits, 32-bits using different adders. [1] [4] [5] [6] [8] [10] [12] [14] [15].
Based on this concept carry look ahead adders are implemented of 128-bits. A Verilog code is written to simulate carry look ahead adder. The Verilog code is written based on dataflow modelling. The sum and carry are calculated using the formula's specified. The Register Transfer Level (RTL) view of carry look ahead adders is shown in figure 4.

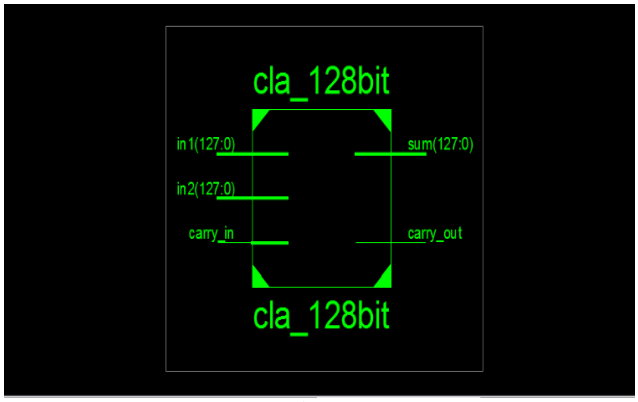

Figure 4: RTL view of Carry Look Ahead Adder

Simulation result is shown in figure 5.

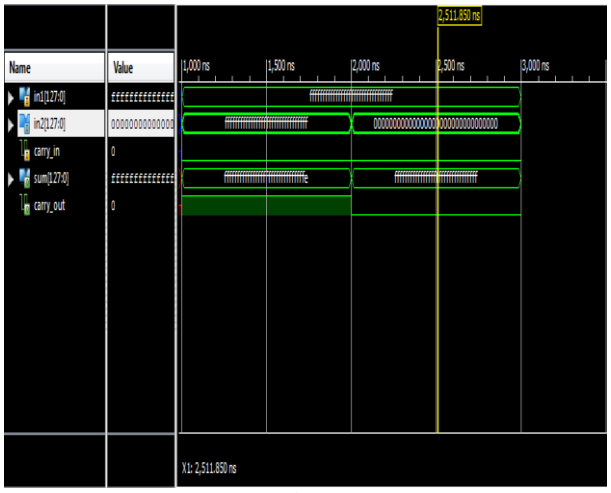

Figure 5: Simulation result of 128-bit carry look ahead adder

Example: 1] Consider two inputs,
0001 (this is binary equivalent of 1)
+ 0010 (this is binary equivalent of 2)
0011 (this is binary equivalent of 3)

2] consider two inputs of 128-bits,
32'd FFFF (this is binary equivalent of 128)
+ 32'd 0000
~~32'd FFF~~F (this is binary equivalent of 128)

3] consider two inputs,
32'd FFFF (this is binary equivalent of 128)
+ 32'd FFFF (this is binary equivalent of 128)
~~32'd FFF~~E (this is binary equivalent of 256)

B. Carry look ahead Multiplier

A multiplier is a digital circuit that multiplies two binary numbers. It is built using adders. A carry look ahead multiplier of n-bits gives a 2n-bits product. A Verilog code is written for a carry look ahead multiplier by instantiating a carry look ahead adder. To elaborate first the multiplier's LSB bit is multiplied with the multiplicand the result is stored in a temporary variable. Further the next bit of multiplier is multiplied with multiplicand and result is stored by shifting 1 bit. This process is continued until all the bits of multiplier is multiplied with multiplicand. The intermediate product results obtained are added to give out the final product.
Example- 1] Consider two inputs of 4-bits,
0011(this is binary equivalent of 3)

X 0010(this is binary equivalent of 2)

0000

0011 (Procedure of successiveaddition)

0000

0000

00000110 (this is binary equivalent of 6)

2] consider two inputs of 128-bits,

32'd FFFF (this is binary equivalent of 128)

X 32'd FFFF (this is binary equivalent of 128)

32'd 0B400000 (this is binary equivalent of 16384)

3] consider two inputs,

32'd FFFF (this is binary equivalentof128)

X 32'd 0000

32'd 00000000

The RTL view of carry look ahead multiplier is shown in figure 6

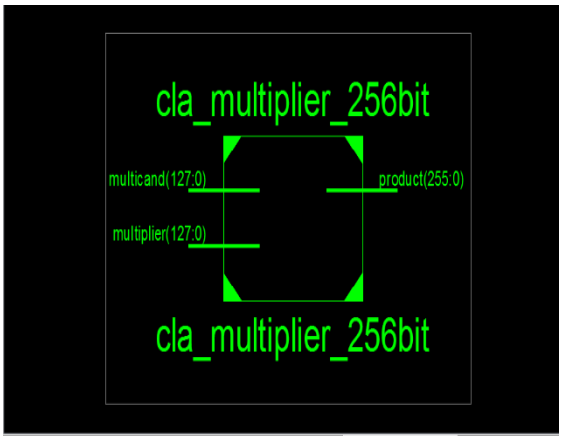

Figure 6: RTL view of Carry Look Ahead Multiplier (High speed Multipliers)

The simulation results of carry look ahead multiplier is shown in figure 7

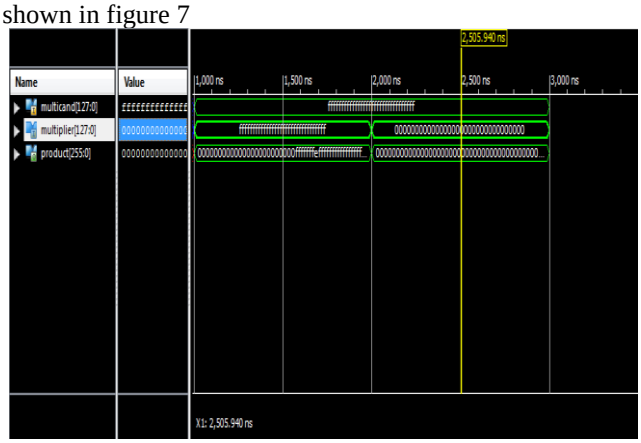

Fig 7: Simulation result of a 256-bit carry look ahead multiplier (high speed multipliers)

A multiplier is basically used to reduce the number of operations thereby reducing the dynamic power which is a major part of the total power consumption so the need of multipliers in increased. As designers mainly.

C. Complex summer

A complex summer is a circuit that is defined to add two complex numbers. A Verilog code is written by instantiating carry look ahead adders. The real part and imaginary part are calculated separately and finally the result is shown together. The simulation result for the Verilog code is shown in figure 6.

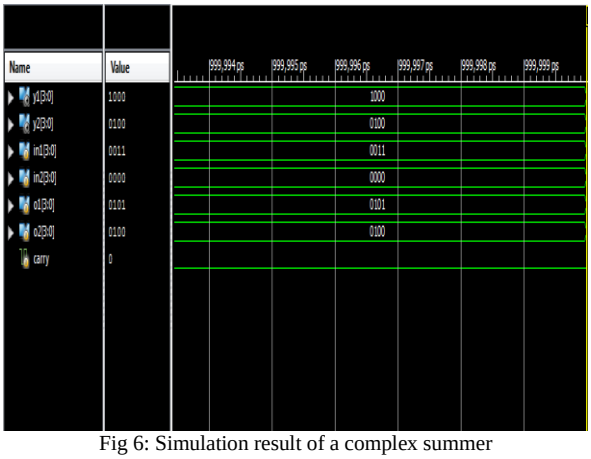

Fig 6: Simulation result of a complex summer

Example: 1] Consider two inputs, 3+j2 and 4+j5

0011 (this is binary equivalent of 3)

\+ 0100 (this is binary equivalent of 4)

0111 (this is binary equivalent of 7)

0010 (this is binary equivalent of 2)

\+ 0101 (this is binary equivalent of 5)

0111 (this is binary equivalent of 7)

Hence the final result is 7+j7.

2] Consider two inputs, 11+j5 and 4+j7.

1011 (this is binary equivalent of 11)

\+ 0100 (this is binary equivalent of 4)

1111 (this is binary equivalent of 15)

0101 (this is binary equivalent of 2)

\+ 0111 (this is binary equivalent of 5)

1100 (this is binary equivalent of 7)

Hence the sum is 15+j7.

II. CONCLUSION

Design of high-speed multipliers and complex summers using carry look ahead adders is simulated. Verilog code is used to simulate the multiplier and complex summer. Using the carry look ahead adder it improved the overall speed of the multiplier. The experiment shows significant increase

in speed over conventional multipliers. Reduced propagation time and faster addition logic is ideal for calculation of very large numbers (hundreds or even thousands of bits). As for large numbers the logic for carry does not become any complex. Hence it can be adopted for multiplication of very large numbers. Similarly, a complex summer can also be used for addition of large complex numbers required in scientific calculations. The codes written in Verilog are simulated on Xilinx tool.

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