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High Performance Look-Ahead Binary Counter based on Partitioning

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***Abstract*— A synchronous binary counter is one in every of the essential components widely utilized in VLSI design, and it's required to be fast and support a large bit-width in many applications. However, most of the previous counters are related to a limited counting rate because of large fan-outs and long carry chains, especially when the counter size isn't small. within the proposed work, a brand-new fast structure for synchronous binary counting, which includes a minimal counting period for practical counter sizes starting from 8 to 128 bits is meant supported partitioning. We first adopt an 1-bit Johnson counter to scale back the hardware complexity, and so duplicate the 1-bit Johnson counter to decrease the propagation delay caused by large fan-outs. within the proposed counter architecture, an N-bit counter is realized by partitioning it into three subcounters, C1, C2, and C3. Subcounter C1 is an 1-bit counter that toggles between 0 and 1 every clock. Subcounter C2 is an (n-1)-bit counter that works supported the backward carry propagation, and therefore the last subcounter C3 is an (N-n)-bit binary counter supported look ahead logic. The state look-ahead path prepares the counting path's next counter state before the clock edge such the clock edge triggers all modules simultaneously, thus concurrently updating the count state with the same delay in the least counting path modules/stages with relation to the clock edge. Implementation results show that the proposed design may be realized with a little number of flip-flops, which is nearly linear to the counter size, and it can operate at a high clock frequency.**

Keywords*— *Back ward carry propogation , Prescaled Counters, State lookahead logic

I. INTRODUCTION

Counter is one of the essential components actively employed in many applications like measurement systems, analog-to-digital converters, frequency dividers, phase-locked -loop frequency synthesizers, and so on. ecause of recent advances within the applications, it's commonly required to implement a quick, wide counter supporting continuing counting rate independent of the counter size. However, the counting rate and therefore the size conflict with one another, because the carry propagation from a low-order bit to a high-order bit becomes longer because the counter size gets larger.

To obtain a stable binary output, a synchronous binary counter can be used. The simplest synchronous counter is the ripple carry counter in which the carry-out of an one-bit adder is connected to the carry-in of the succeeding stage. The chain of carry signals is called a ripple carry chain, as the carry signal is continually rippled into the next stage. The main limiting factor of the speed of a synchronous counter is the long carry propagation caused by the carry chain. There have been many techniques developed to derive fast counters. The ripple carry chain in the traditional binary counter was replaced with a carry-lookahead circuit in order to achieve a significant speedup [1].

In addition, a state-lookahead topology was used in [3] to break the carry chain by adding D F/Fs, avoiding the rippling. In [4], the carry chain was constructed with employing a tree structure. However, regarding a counter as a combination of an adder and a state register is not effective in achieving a constant clock period, since the lower bound of the adder delay is not constant. There have been other efforts to speed up the counter by improving the F/F. For example, high-speed synchronous counters were developed by using the F/F based on the true single-phase clock [1], [5]. To accomplish both constant delay and binary sequence, another carry propagation method called backward carry propagation was presented in [7]. It exploits the characteristics of a binary sequence that the more significant bits become high earlier than the less significant bits. This approach can be applied to achieve a constant-delay counter since the carry propagation is only determined by the least significant bit (LSB).

Another synchronous binary counter based on prescaling was presented in [8]. A wide counter is partitioned into subblocks. The high-order block is enabled by a prescaled enable (PEN) signal generated from the low-order block, and the clock period of a prescaled counter is determined by the least significant block. However, there are still issues related to the large fan-out and the wide distribution of a PEN signal that is necessary to drive a large number of inputs of the F/Fs in the next block. The huge fan-out is in fact the critical issue to be solved in realizing a fast binary counter. As the counter size increases, the fan-out issue becomes more severe, leading to the longer propagation delay.

In this paper, we present a binary synchronous counter that operates with a constant delay for practical counter sizes ranging up to 128 bits. In the proposed counter, the large fan-out issue is mitigated by duplicating the one-bit Johnson counter and by applying the backward carry propagation method to get rid of the additional delay induced by the ripple carry propagation. And further delay is reduced by applying state lookahead logic that prepares the counting path's next counter state prior to the clock edge such that the clock edge triggers all modules simultaneously. The proposed counter achieves the highest counting rate, and the counting rate is

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determined only by the least-significant 1-bit counter regardless of the counter size.

II. EXISTING COUNTERS

Some previous works in which concepts that are relevant to the proposed counter are described below. The backward carry propagation presented in [7] is an important concept in implementing a fast synchronous counter. What makes it work is the fact that a more significant bit of the counter becomes high earlier than the least significant bit due to the characteristics of the binary number system. Instead of a single chain used in the conventional binary counter, each counter bit has a separate AND chain connected in the backward direction. In a carry chain, the early arriving signals are evaluated in advance before the lately available signals arrive. Therefore, the propagation delay is mainly determined by the delay of the last AND gate and a T F/F.

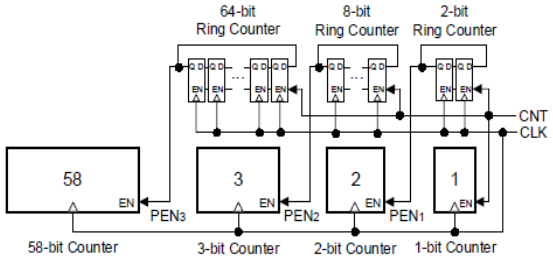

Fig.1. 64-bit prescaled counter that generates prescaled enable signals with ring counters.

The constant-delay binary counter based on prescaling was presented in [8], which is depicted in Fig. 1. A wide counter is partitioned into subblocks of different sizes, and the high-order subblock operates at the lower frequency than the low-order subblock. The main concept is to make a high-order block add one according to the PEN signal generated from the low-order block called a prescaler. The frequency of a PEN is much slower than that of the clock signal. This is possible because the high-order block is incremented much less frequently than the low-order block. The typical method to generate the PEN is to use a ring or twisted-tail counter [8]. The ring counter connects the output of the last F/F to the input of the first one, making a circular structure. When the n-bit ring counter reaches $2n-1$ value, the PEN signal becomes 1. Similarly, the n-bit twisted-tail counter or the Johnson counter, in which the inverted output of the last F/F is connected to the input of the first one, activates the PEN signal when the count value becomes 2_{n-1}. They can operate at a high frequency, as there is no combinational circuit between adjacent F/Fs, allowing the PEN to be synchronous with the clock. However, the approach is not efficient, as it needs N F/Fs to traverse N states, increasing the hardware complexity. Moreover, the PEN signal needs to drive all the F/Fs in the next partition, leading to a high fan-out and increasing the propagation delay and thus decreasing the overall counting speed. Moreover, the PEN signal needs to drive all the F/Fs in the next partition, leading to a high fan-out and increasing the propagation delay and thus decreasing the overall counting speed.

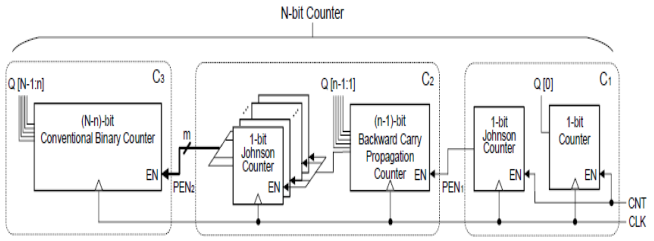

Fig.2. Detailed structure of the existing N-bit counter

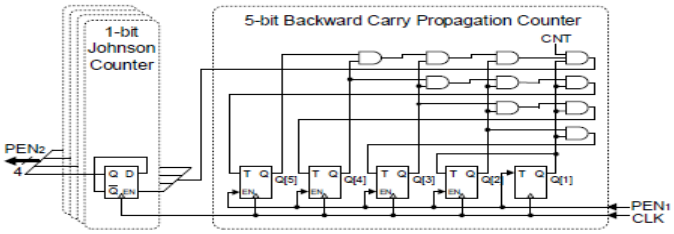

Fig.3 Prescaled enable signal generation with redundant 1-bit Johnson counters.

An N-bit counter is partitioned into three different subcounters was presented in [2] in order to take advantage of prescaling. In this counter architecture, an N-bit counter is realized by partitioning it into three subcounters, $C1$, $C2$, and $C3$, as shown in Fig. 2. Subcounter $C1$ is an 1-bit counter that toggles between 0 and 1 every clock. Subcounter $C2$ is an (n-1)-bit counter that works based on the backward carry propagation, and the last subcounter $C3$ is an (N-n)-bit conventional binary counter. Here m 1-bit Johnson counters are employed to generate m PEN signals to be used for the last subcounter. we assume that $n = \lfloor \log 2\ N \rfloor$ and $m = \lceil (N - n)/L \rceil$, where L is the maximum fan-out to be determined by conducting simulations The Johnson counter is initialized to 0, and the PEN signal is generated to enable the counting of the next subcounter when the Johnson counter undergoes a state change from 0 to 1.

The basic principle of the partitioned counter is to prescale the high-order block by considering the low-order block. An N-bit counter is divided into 3 subcounters such that the propagation delay of the (N-n)-bit synchronous ripple carry binary counter $C3$, which consists of (N-n-1) AND gates, is smaller than the period of PEN2 generated in $C2$. And subcounter $C2$ is an (n-1)-bit backward carry propagation counter and enabled by the 1-bit counter $C1$. Observing that the delay of the long carry chain is reduced to only one AND gate by employing the backward carry propagation, we can guarantee that the carry propagation of $C2$ is shorter than the period of PEN1 generated in $C1$.

To deal with the fan-out issue, a $2n$-bit ring counter is replaced with an 1-bit Johnson counter as illustrated in Fig. 2, where a 5-bit backward carry propagation counter and a PEN generator are exemplified for $N = 64$, $n = 6$ and $m = 4$. The 1-bit Johnson counter changes its state when enabled after being initialized to 0 at the beginning. Our goal is to make PEN2 have a pulse every $2n$ cycles, 64 cycles in this example. For the purpose, the enable signal should be high at the $(2_n - 2)$th and $(2_n - 1)$th cycles, the 62nd and 63rd cycles

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in the example, in order to make PEN2 being 1 at the $(2n-1)$th cycle, or 63rd cycle in the example. Such a signal can be generated by exploiting the backward carry propagation method depicted in Fig. 3. The AND operation of Q[5], Q[4], Q[3] and Q[2] can be realized by employing backward AND chains. The Q[5]&Q[4]&Q[3]&Q[2] signal becomes high when Q[2] undergoes a transition from low to high and lasts for four cycles. The late arriving signal Q[1] is connected to the last AND gate to make the output of the AND chain high for two cycles. The enable signal is equivalent to the result of &Q[5:1], and the computation takes only one AND gate as &Q[5:2] is already computed in advance thanks to the backward carry propagation. The enable signal is high at the 62nd and 63rd cycles and repeats periodically every 64 cycles. The PEN2 is inverted one clock cycle after the enable signal is asserted. However, the performance of module C3 is slow due to the long carry propagation caused by the carry chain in the conventional counter. So, there is a scope to improve the design of subcounter C3.

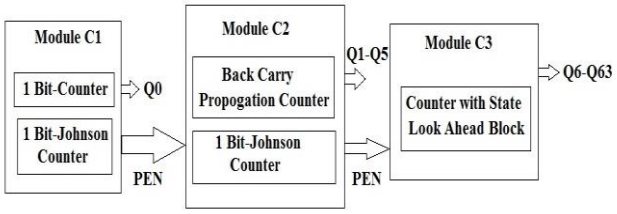

Fig.4 Detailed structure of the proposed N-bit counter.

III. PROPOSED COUNTER ARCHITECTURE

In proposed counter, we improve counter operating frequency by employing a unique parallel counting architecture in conjunction with a state look-ahead path and pipelining to eliminate the carry chain delay of subcounter C3 is depicted in figure.4. The state look-ahead path bridges the expected overflow states to the counting modules, which are exploited within the counting path. The counting modules are partitioned into smaller 2-bit counting modules split by pipelined DFF latches. The state look-ahead path is partitioned using the identical pipelined alignment paradigm because the counting path and thereby provides the proper predicted overflow states for all counting stages. Thereby, all counting states and each pipelined DFFs are triggered concurrently on the clock edge, enabling the count state in modules of most significance to be predicted by the count state in modules of lower significance. This cooperation between the counting path and state look-ahead paths enables every counting module to be triggered concurrently on the clock edge with none rippling effect.

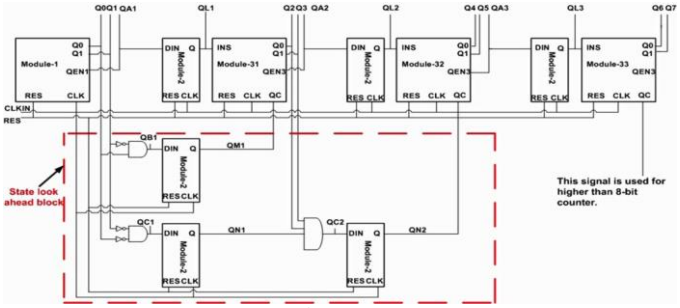

Fig.5 Functional block diagram of our proposed 8-bit parallel counter with state look-ahead logic and counting logic.

A. Parallel Counter Architecture

Figure.5 represent a sample 8-bit parallel counter architecture that is utilized in our proposed counter. This structure consists of the counting path (all logic not encompassed by the dashed box) and therefore the state look-ahead path (all logic encompassed by the dashed box) .We construct our counter as a singular mode counter, which sequences through a hard and fast set of preassigned count states, of which each next count state shows the following counter value in sequence. The counter is separated into steady 2-bit synchronous up counting modules. Next state transitions in counting modules of upper significance are enabled on the clock cycle preceding the state transition using stimulus from the state look-ahead path. Then at the rising clock edge (CLKIN) all counting modules concurrently transition to their next states. The counting path controls counting operations and therefore the state look-ahead path anticipates future states and thus prepares the counting path for these future states. Three types of modules are there, module-1, module-2, and module-3 S, where S=1, 2, 3, etc. and represents the position of module-3 accustomed construct both paths.

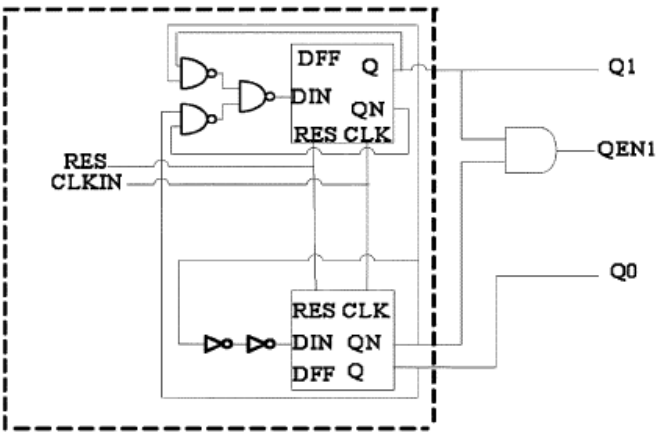

Fig.6 Module-1 hardware schematic.

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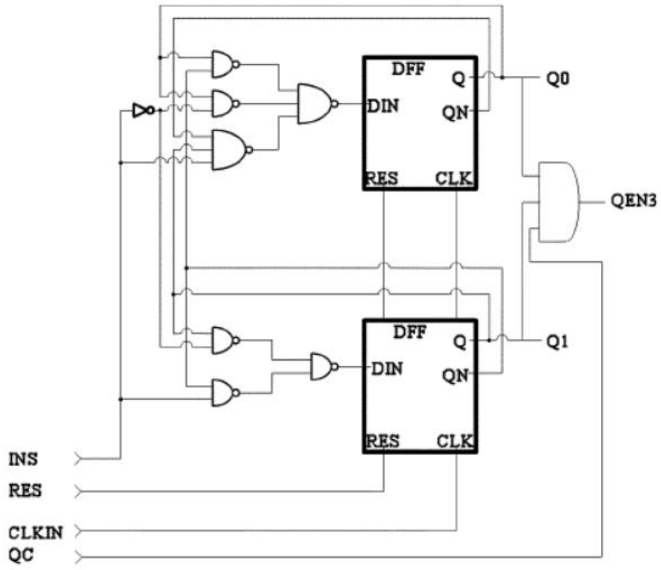

Fig.7 Module-3 hardware schematic.

1) Counting Path: Fig. 6 shows the hardware schematic of Module-1. it's a parallel synchronous binary 2-bit counter, which is chargeable for low-order bit counting and generating future states for all module-3 S's within the counting path by pipelining these future states through the state look-ahead path. Module-1 and module-3 are exclusive to the counting path and every module represents two counter bits. within the counting path, each module-3 is preceded by an associated module-2. The output of module-1 is Q1Q0 and QEN1 connects to the module-2's DIN input. Module-2 could also be a standard positive edge triggered DFF and is present in both paths. within the counting path.

Module 2 act as a pipeline between the module-1 and module-3 1 and subsequent module-3S with in the counting path. In state look-ahead logic module -2 placement increases counter operating frequency by eliminating the lengthy AND-gate rippling and large computer circuit fan-in and fan-out present in large width parallel counters. instead of the modules of upper significance are enabled by the module-3S and state look-ahead logic. Thus, the module-2s within the counting path provide a 1-cycle look-ahead mechanism for triggering the module-3S's, and enabling the module-2s to stay up a unbroken delay for all stages.

Module-3S's serve two main purposes. Their first purpose is to come back up with all counter bits associated with their ordered position and the second purpose is to enable future states in module-3S's in conjunction with stimulus from the state lookahead path. Fig. 7 shows the hardware schematic of module3S. And it is a parallel 2-bit binary counter whose count is enabled by INS, that connects to the Q output of the preceding module-2. It also provides one-cycle look ahead mechanism.

2) State Look-Ahead Path: The state look-ahead logical operation avoids the utilization of an overhead delay detector circuit that decodes the low order modules to get the enable signals for higher order modules and enables all modules to be triggered concurrently on the clock edge, thus avoiding delay and rippling. The state look-ahead logic is principally adoring the one-cycle look-ahead mechanism within the counting path. To enabling the subsequent state's high order bits depends on early overflow pipelining across clock cycles through the module-2S within the state look-ahead path.

For example, in a 4-bit counter constructed of two 2-bit counting modules, the counting path's module-2 decodes the low-order state Q1Q0=10 and carries this decoding across one clock cycle and enables Q3Q2=01 at module-3 1 (see Fig. 1) on the next rising clock edge. This operation is equivalent to decoding Q1QO=11 and enabling Q3Q2=01 on the next immediate rising clock edge. The state look-ahead logic expands this principle to an X-cycle look-ahead mechanism.

IV. PERFORMANCE COMPARISON

Performance analysis of existing counter and proposed counter has been carried out using Xilinx ISE Design suit.It is observed that minimum input time arrival before clock is 6.214ns in existing system and 6.014ns in proposed system. And the maximum output required time after clock for existing system is 11.02ns and that of proposed system is 7.744ns.The average time delay of proposed system is 5.822ns , It is fewer than existing system.

Fig. 8 depicts the device utilization summary of existing system and Fig. 9 depicts the device utilization summary of proposed system. It is also noticed that power consumption is reduced to 141 P(mW) in this proposed design from 186 P(mW) in existing system.

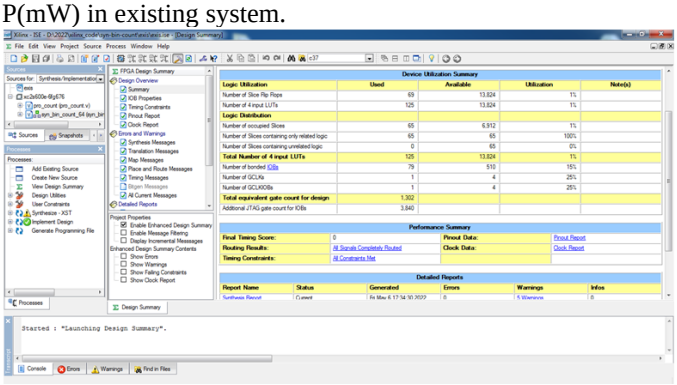

Fig.8 Device Utilization Summary of Existing System

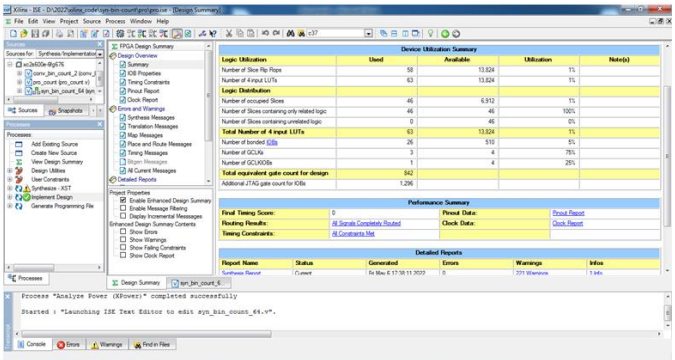

Fig.9 Device Utilization Summary of Proposed System.

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The counting frequency of the proposed counter is almost constant, 2GHz, and almost independent of the counter size up to 128 bits and the hardware complexity is mainly determined by the counter size and the duplicated 1-bit Johnson counters have a little effect on the overall complexity.

V. SIMULATION RESULTS

The proposed synchronous binary counter based on partitioning is implemented in Verilog and simulated using ModelSim SE 6.3f. Fig.10 shows the simulated result of 8-bit parallel counter (called one by one in subcounter C3) and fig.11 depicts the simulated output of proposed binary counter realized with subcounter C1, subcounter C2 and subcounter C3.

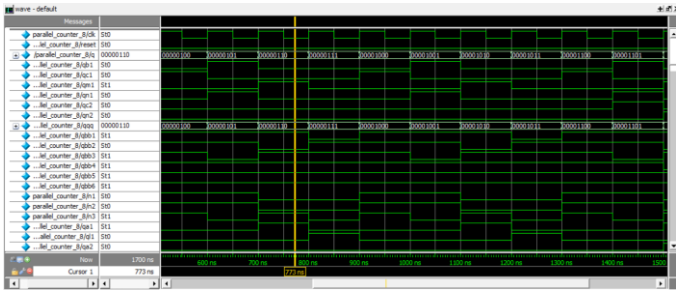

Fig.10 Simulated result of parallel counter

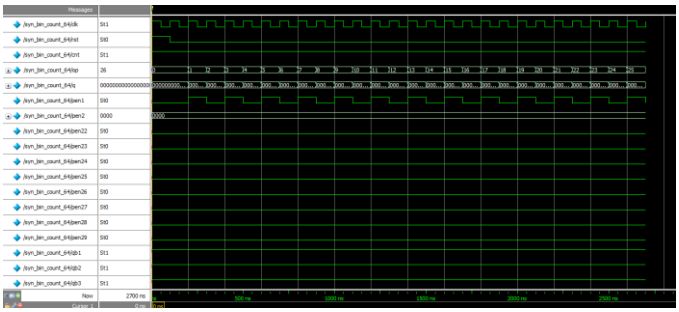

Fig.11 Simulated result of proposed counter

The simulated counter output is also analysed in radix form without any further decodings techniques using ModelSim SE 6.3f.

VI. CONCLUSION

In this brief, we presented a high-performance binary counter supported state look ahead logic. The counter structure's main features are a pipelined paradigm and state look-ahead path logic whose interoperation activates all modules concurrently at the system's clock edge, thereby providing all counter state values at the precise same time without rippling affects. Other than that, the proposed counter design has used backward carry propagation and exploited redundant 1-bit Johnson counters to cut back the quantity of flip-flops and therefore the unwanted propagation delay caused by large fan-out nodes. This structure avoids employing a long chain detector circuit typically required for big counter widths. additionally, this structure uses well-ordered VLSI topology, that's designed in parallel counter architecture in subcounter C3, which is attractive for continued technology scaling because of two repeated module types (module-2s and module-3s) forming a ideal pattern and there is no increase in fan-in or fan-out because the counter width increases, leading to a uniform frequency delay that's attractive for parallel designs. Our proposed system is one step ahead than existing system in terms of number of gate count, delay, and power.

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