High Performance & Improved 8T SRAM Cell

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***Abstract*-The Static Random Access Memory (SRAM) is very essential memory device for storing the data on chip. The SRAM takes a large fraction of total power therefore low power SRAM design is very important. In these days the SRAM sizing has been scaled down due to the increase density of SRAM in system on chip (SOC) and other integrated component, which works on lower supply voltage this leads to significant amount of power saving. However, the scaling of lower supply voltage is also being affected the stability and performance of SRAM cell. Because of the stability of SRAM cell depends on the static noise margin which is reduced by the lower supply voltage. The delay of SRAM of cell increases considerably with lower V_{dd} and also lowers the speed of the SRAM. In this paper, The proposed improved 8T SRAM memory cell reduced power consumption 24.17% and delay 9.1% compared to conventional 6-T SRAM cell. And it also improves the cell stability by increasing the static noise margin 35.02% compared to conventional 6-T SRAM cell.**

Keywords− Static Noise Margin, Power Consumption, Delay.

I. INTRODUCTION

These days the computers, super computers, low-power processors and workstations are using fast SRAMs, and in the future will require larger density memories with faster access time. The Low-power and High-density SRAMs are needed for applications such as hand-held terminals, IC memory cards, notebooks and laptops, since these devices frequently use battery as power source ,thus, it should consume power as low as possible and it is necessary also for maintaining low cooling and packing costs for these devices. The Scaling in CMOS technology continues because of the demand of battery operated devices. But as the technology scaling continues, power consumption has become a major concern to designers of the circuits. According to Moore's Law, in every two years, the number of transistors built on a single chip gets doubled. If the power consumption due to each individual transistor does not scale down with the transistor's size then the power consumption of the whole chip will continue to increase and it leads to higher chip temperature and thus degrades performance due to low electron/hole mobility at high temperature [9]. Power consumption in SRAMs is not only due to power supply voltage reduction but also by the use of low-power circuit techniques. An SRAM cell must be designed to provide a non-destructive read operation and a reliable write operation. The nanoscale CMOS SRAM memory design faces many challenges like reducing noise margin and increasing power consumption because of the continuous technology scaling. In this paper the design of 6T SRAM cell with low delay, low power consumption and improved static noise margin is presented.

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II. CONVENTIONAL 6T SRAM CELL DESIGN

A. Construction

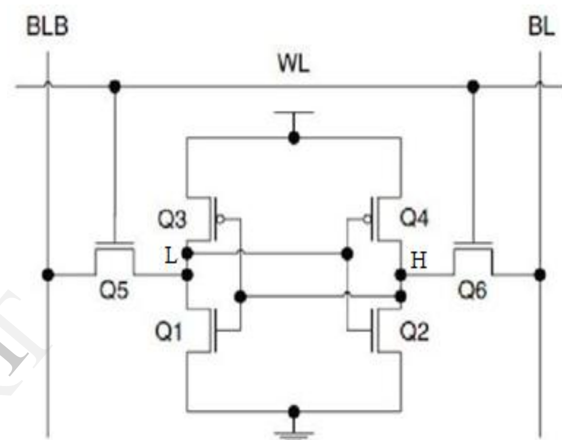

Figure1. Conventional 6-T SRAM Cell.

The SRAM cell is the key component for storing the binary information. By the use of two cross-coupled inverters, a typical SRAM cell forms a latch and access transistors. The access transistors enable access to the cell during read and write operations and provide cell isolation during the not-accessed state. SRAM cell is designed to provide write capability, non-destructive read access and data storage (or data retention) for as long as cell is powered. An analysis and design of different SRAM cells are: Conventional 6T and improved 8T. They are compared with respect to power, delay and speed. Normally, the cell design must strike a balance between delay, speed, durability, cell area and leakage but power reduction is one of the most important design objectives. However, power cannot be reduced indefinitely without compromising the other parameters. As an example, low-power can compromise the cell area and also the speed of operations. The mainstream six-transistor (6T) CMOS SRAM cell is shown in Figure -1, here four transistors (Q1−Q4) comprise cross-coupled CMOS inverters and two NMOS transistors Q5 and Q6 provide read and write access to the cell. The most popular SRAM cell is a 6T CMOS SRAM cell due to its superior robustness, low-voltage and low power operation [8].

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B. Operation of SRAM

The Static Random Access memory device can perform the operation which is as follows: hold, read and write.

a. Hold: The access transistors Q5 and Q6 disconnect the cell from the bit lines, if the word line is not asserted. The two cross coupled inverters formed by Q1 – Q4 will continue to reinforce each other as long as they are connected to the supply.

b. Read:

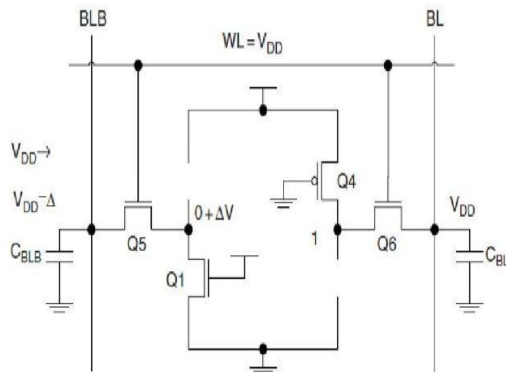

Figure2. Read Operation of 6-T SRAM Cell.

The bit lines are pre-charged to V_{DD} prior to initiating a read operation. The read operation is initiated by enabling the word line (WL) and connecting the pre-charged bit lines (BL and BLB) to the internal nodes of the cell. On read access, the bit line voltage V_{BL} remains at the pre-charge level as shown in Figure-2. The complementary bit line voltage V_{BLB} is discharged through transistors Q1 and Q5 connected in series. Conclusively, transistors Q1 and Q5 form a voltage divider whose output is now no longer at zero volt and is connected to the input of inverter Q2−Q4 (as in Figure -1). The sizing of Q1 and Q5 should ensure that inverter Q2−Q4 do not switch causing a destructive read [8].

c. Write:

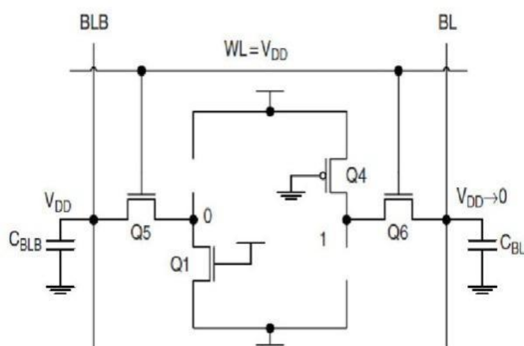

Figure3. Write Operation of 6-T SRAM Cell.

While the write operation one of the bit lines i.e. BL in Figure-3, is driven from pre-charged value (V_{DD}) to the ground potential by a write driver through transistor Q6. The cell is flipped and its data is effectively overwritten if transistors Q4 and Q6 are properly sized. A statistical measure of SRAM cell write ability is defined as write margin. The write margin is defined as the minimum bit line voltage required to flip the state of an SRAM cell. Write margin value and variation is a function of the process variation, SRAM array size and cell design. A cell is considered not writeable if the worst-case write margin becomes lower than the ground potential. The write operation is applied to the node storing a '1'. It is necessitated by the non-destructive read constraint that ensures that a '0' node does not exceed the switching threshold of inverter Q2−Q4. The only function of pull-up transistors is to maintain the high level on the '1' storage node and prevent its discharge by the off-state leakage current of the driver transistor during data retention and to provide the low-to-high transition during overwriting [8].

III. PROPOSED CIRCUIT

The proposed SRAM cell is shown in Figure 4; it is made of conventional 6T SRAM with two additional PMOS and NMOS transistor. Over pull up & pull down network of two cascade inverter. In this new circuit NMOS transistor is connected to the pull down network of SRAM cell and other PMOS is connected to the Pull up network of the SRAM cell. The input of the gate of NMOS transistor of pull down network of the SRAM cell is connected V_{dd} and the input gate of PMOS transistor of pull up network of the SRAM cell is connected to ground which keep turn ON the transistor M7 & M8 throughout all operation of the SRAM. This whole modification in the circuit of the SRAM offers better improvement in comparison of 6T. A conventional 6T SRAM consumed more power due to its leakage problem but in the proposed circuit by the adding two transistor at pull up and pull down network leakage is reduced therefore the power consumption of the proposed circuit become less. , The proposed improved 8T SRAM cell shows maximum reduction in power consumption of 24.17%, maximum reduction in delay of 9.1% and maximum SNM of 35.02% increases compared with conventional 6T SRAM cell.

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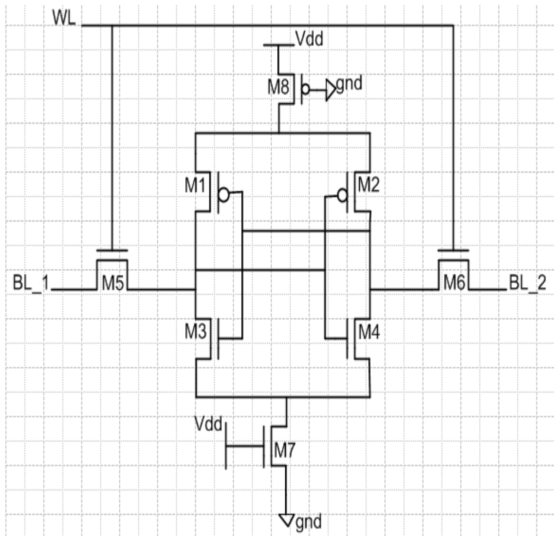

Figure4. Improved 8T SRAM cell

IV. SIMULATION AND RESULT

The Simulation and result of the proposed SRAM design is presented in Table 1. In the following subsections, three important metrics of an SRAM design: Static noise margins, power, and delays are explaining.

1. STATIC-NOISE-MARGIN (SNM)

The stability of SRAM circuit depends on the Static Noise Margin. The basic SNM is obtained by drawing and mirroring the inverter characteristics and finding the maximum possible square between them. It is a graphical technique of estimating the SNM.

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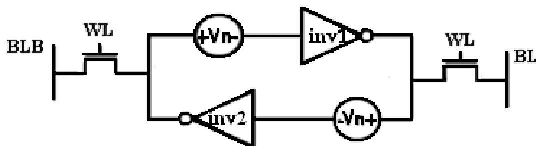

Figure5. The standard setup for SNM definition

The Figure-6 shows a common way of representing the SNM graphically for a bit-cell holding data. This figure plots the Voltage Transfer Characteristic (VTC) of Inverter 2 (inv2) and the inverse VTC-1 from Inverter 1(inv1). Resulting two-lobed curve is called a 'butterfly curve' and is used to determine the SNM. The length of the side of the largest square that can be embedded inside the lobes of the butterfly curve is defined as the SNM. Consider the case when the value of the noise sources with value Vn are introduced in the bit cell at each of the internal nodes. When the value of Vn increases from 0, it causes the VTC-1 for first inverter in Figure-5 to move downward and the VTC for the second inverter to move to the right. The values of SNM vary in different operation modes. SNM is becoming important factor to check the stability during read operation. SRAM cell immunity to static noise is measured in terms of SNM that quantifies the maximum amount of voltage noise that can be tolerated at the cross-inverters output nodes without flipping the cell. The value of the SNM during cell operation changes with any change in the noise. Although the SNM is important during hold, the cell stability during active operation represents a more significant limitation to SRAM operation [7].

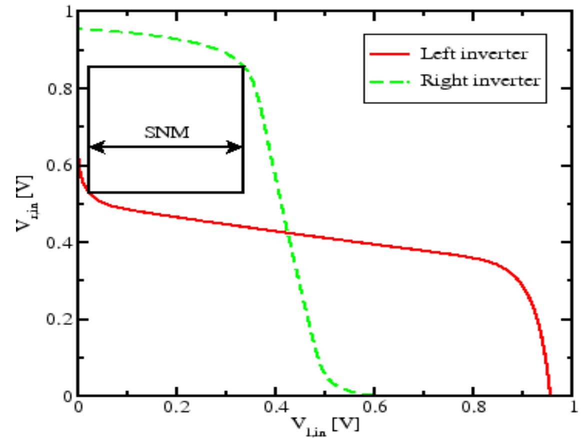

Figure6. General SNM characteristics during Hold operation

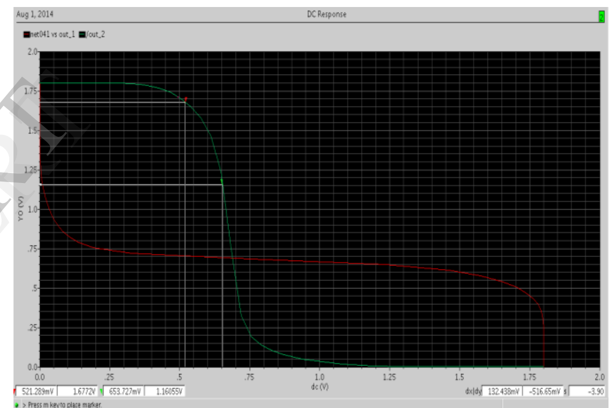

Figure7. Butterfly curve for SNM of Conventional 6T SRAM cell.

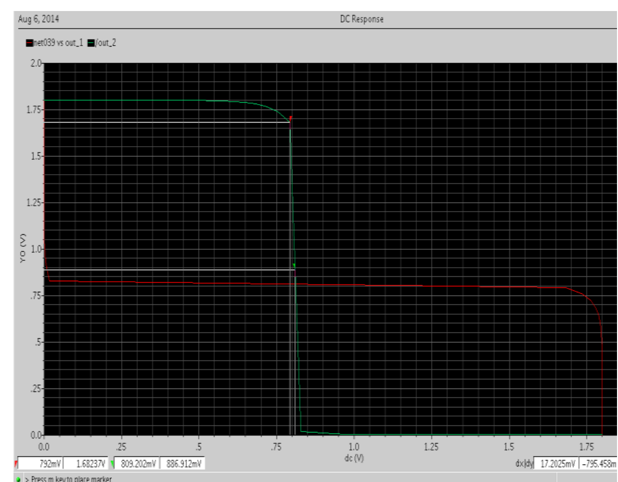

Figure8. Butterfly curve for SNM of improved 8T SRAM cell

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5.2- DELAY

The delays of SRAM are usually defined as the time it takes to read or write a value from an SRAM cell. While a node is switching, the delay is measured as the time difference between 10% and 90% of the voltage swing. As an example - if we are trying to bring node A from 0V to 1V then the delay is the time it takes for node A to go from 0.1V to 0.9V. In case of a write operation, write delay is defined as the time required for writing '0'to storage node 'L' from the time when word Line is activated to the time when 'L' falls to 10% of its initial high level. In the same way, writing '1' to 'L' is defined from the time when word Line is activated to the time when 'L' rises to 90% of its full swing from its intial low level. Write delay is approximately equal to the propagation delay of inv2 and invl [2].

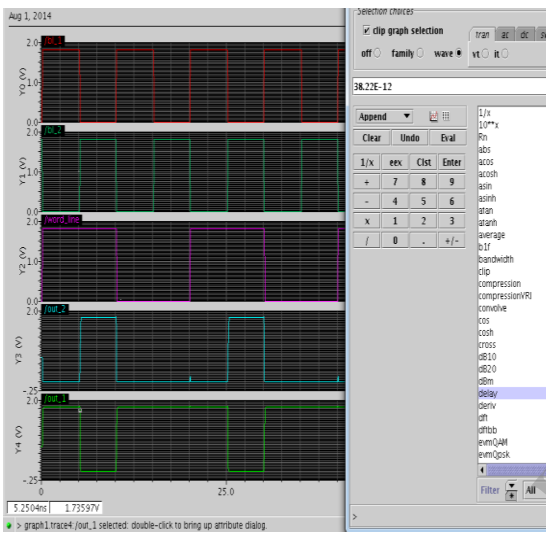

Figure9. Simulated result for delay of Conventional 6T SRAM cell

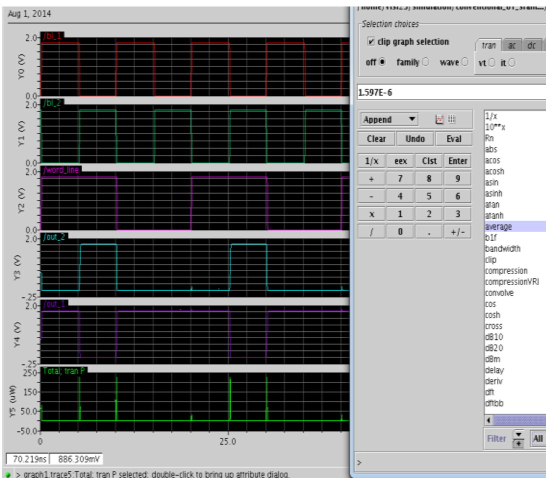

Figure10. Simulated result for delay of improved 8T SRAM cell

5.3- POWER CONSUMPTION

The power consumption of Static Random Access Memory cell depends on consumption of the power which used to perform the operation of the transistor [4]. Dynamic power consumption in SRAMs is consumed due to the charging and discharging capacitances during read and write operation and during each cycle of SRAM particular amount of Energy is drawn from the power supply and dissipated. For each cycle the power consumption is depended on the type of operation (read or write). Also, when the capacitor charged from GND to VDD and then discharged VDD to GND, the amount of energy drawn from the power supply and dissipated equals $C_L V_{DD}^2$. The stored energy on the capacitor C_L with voltage V_C equals ½ $C_L V_C^2$. Therefore, each time the capacitor C_L is charged from V_C to V_{DD} and then discharged V_{DD} to V_C [3]. A average power dissipation of any device over one period can be obtained by following expression [5].

$$P_{av} = [(1/T)\ {}_0\!\int^T I\ dt] \times V$$

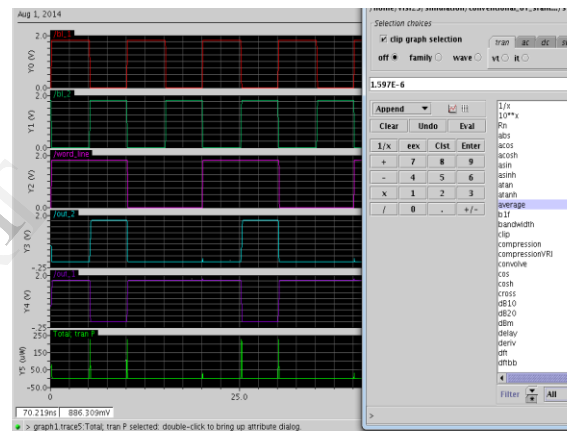

Figure11. Simulated result for Power Consumption of Conventional 6T SRAM cell.

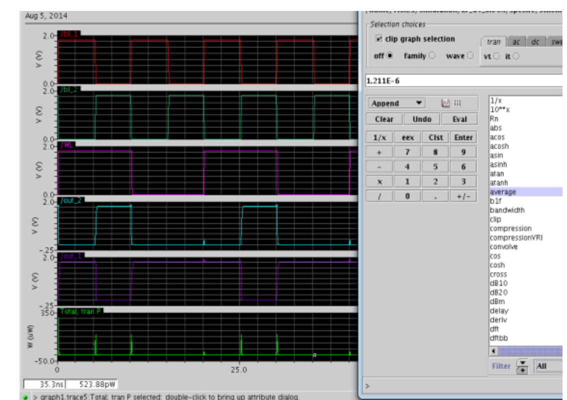

Figure12. Simulated results for power consumption of improved 8T SRAM cell

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Table 1 Comparison of power consumption, delay and SNM.

Parameter	Conventional 6T SRAM	Improved 8T SRAM
Power consumption (μW)	1.597	1.211
Delay(ps)	38.22	34.74
SNM (in hold mode)	0.731	1.125

6. CONCLUSION:

In this paper, we have design and implemented a low power and high SNM SRAM cell. We have also analyzed the power consumption of conventional SRAM cell as well as proposed 8T SRAM cell. The proposed SRAM cell consumes 24.17% less power as compare to conventional 6T SRAM cell and proposed SRAM cell is reducing the delay to 9.1% and Static Noise Margin (in hold mode) of proposed SRAM cell is high 35.02% in compare to conventional 6T SRAM cell. Therefore, proposed SRAM cell is useful for high-speed and low power applications.

REFERENCES

[1] 1-Ajoy C A, Arun Kumar, Anjo C A, Vignesh Raja: "Design and Analysis of Low Power Static RAM Using Cadence Tool in 180nm Technology", IJCST Vol. 5, SPL - 1, Jan - March 2014.

[2] 2-A. Islam, Member, IEEE, and M. Hasan, Member, IEEE: "Leakage Characterization of 10T SRAM Cell", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 59, NO. 3, MARCH 2012.

[3] 3-Sushil Bhushan, Shishir Rastogi, Mayank Shastri, Asso. Professor Shyam Akashe and Dr. Sanjay Sharma: "HIGH DENSITY FOUR-TRANSISTOR SRAM CELL WITH LOW POWER CONSUMPTION", IJCTA | SPT-OCT 2011.

[4] 4-Shyam AKASHE, Sushil BHUSHAN, Sanjay SHARMA: "High Density and Low Leakage Current Based 5T SRAM Cell Using 45 nm Technology", ROMANIAN JOURNAL OF INFORMATION SCIENCE AND TECHNOLOGY Volume 15, Number 2, 2012.

[5] 5-Kang S.-M., Leblebici Y., CMOS Digital Integrated Circuits-Analysis and Design, third edition, WCB McGraw-Hill, 2003.

[6] 6-Ramy E. Aly, Md I. Faisal and Magdy A. Bayoumi: "NOVEL 7T SRAM CELL FOR LOW POWER CACHE DESIGN", 0-7803-9264-71051$20.002005 IEEE.

[7] 7-Nahid Rahman, B. P. Singh: "Design of Low Power Sram Memory Using 8t Sram Cell", International Journal of Recent Technology and Engineering, Volume-2, Issue-1, March 2013.

[8] 8-Sunil Kumar Ojha & P.R. Vaya: "A Novel Architecture of SRAM Cell for Low-Power Application", ISSN (Print): 2278-8948, Volume-2, Issue-4, 2013.

[9] 9-Michael C. Wang: "Low Power Dual Word Line 6-Transistor", Proceedings of the World Congress on Engineering and Computer Science 2009 Vol 1 WCECS 2009, October 20-22, 2009, San Francisco, USA.

[10] 10-K. Dhanumjaya, Dr. MN. Giri Prasad, Dr. K. Padmaraju , Dr. M. Raja Reddy: "Design of Low Power SRAM in 45 nm CMOS Technology", International Journal of Engineering Research and Applications (IJERA), Vol. 1, Issue 4, pp.2040-2045.

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