High-performance and Low transition Carry Skip Adder for adaptive supply voltage

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Abstract - In this paper, we at hand a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. Adders are a key building block in arithmetic and logic units (ALUs) and hence rising their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. In this paper, we present a carry skip adder (CSKA) structure that has a superior speed yet lower energy consumption compared with the conventional one. The speed improvement is achieved by applying concatenation and incrementation schemes to improve the effectiveness of the conventional CSKA (Conv-CSKA) structure. In addition, in place of utilize multiplexer logic, the projected configuration makes use of AND-OR-Invert (AOI) , OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both stable stage size and variable stage size styles, wherein the latter additional improves the speed and energy parameters of the adder. Finally, a hybrid variable latency expansion of the projected structure, which lowers the power consumption without considerably impacting the speed, is presented. This expansion utilizes a modified parallel structure for rising the slack time, and hence, enabling further voltage reduction. The proposed structures are assessed by comparing their speed, power, and energy parameters with those extra adders by means of a 45-nm fixed CMOS technology for a open range of supply voltages. In addition, the power–delay product was the lowly among the structures considered in this paper, while its energy–delay product was almost the same as that of the Kogge–Stone parallel prefix adder with considerably smaller area and power consumption. Simulations on the projected hybrid variable latency CSKA reveal reduction in the power consumption compared with the latest works in this field while having a practically high speed.

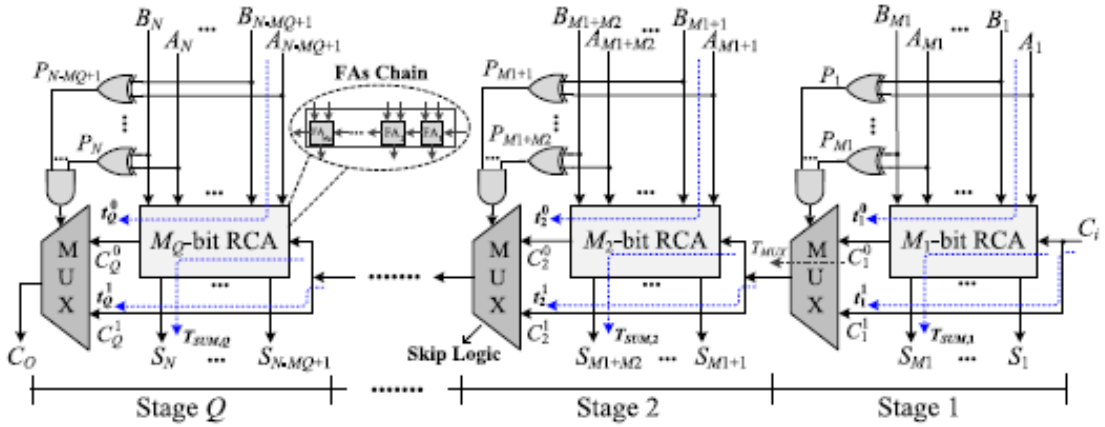
INTRODUCTION

This paper is mainly focused on the low power/energy usage, increasing the speed of access and in hardware side implementations it reduces the area usage and also reduces the complexity of the circuit. One of the effective techniques to lower the power Consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the witching energy on the voltage. In addition, the sub threshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through the Drain-induced barrier lowering effect.

Modifying CSKAs for Improving Speed

The conventional structure of the CSKA consists of stages contain chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The RCA blocks are connected to each one through 2:1 multiplexers, which can be placed into one or more level structures. The CSKA configuration (i.e., the number of the FAs per stage) has a great impact on the speed of this type of adder. Many methods have been suggested for finding the optimum number of the FAs . The techniques presented in make use of VSSs to minimize the delay of adders based on a single level carry skip logic. In , some methods to increase the speed of the multilevel CSKAs are proposed. The techniques, however, cause area and power amplify considerably and less regular layout. The propose of a static CMOS CSKA where the stages of the CSKA have a variable sizes was suggested in . In addition, to lower the transmission delay of the adder, in each stage, the carry look-ahead logics were utilized. Again, it had a complex layout as well as great power consumption and area usage. In addition, the design approach, which was presented only for the 32-bit adder, is not general to be applied for structures with different bits lengths.

Alioto and Palumbo propose a simple strategy for the design of a single-level CSKA. The method was to be based on the VSS technique where the near-optimal numbers of the FAs are firm based on the skip time (delay of the multiplexer), and the ripple time (the time required for a carry to ripple all the way through a FA). The goal of this method is to decrease the Critical path delay by considering a non-integer ratio of the skip time to the ripple time on contrary to most of the previous works, which considered an integer ratio17:20.



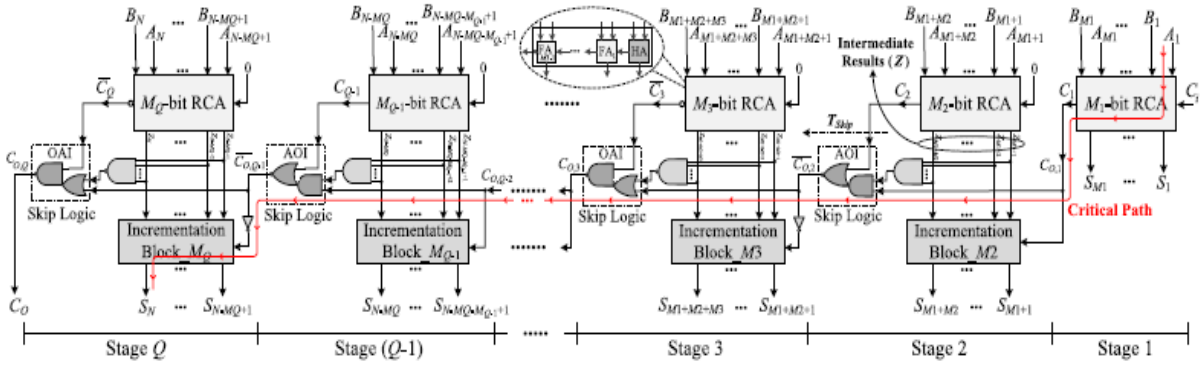
Ripple Carry Adder Method

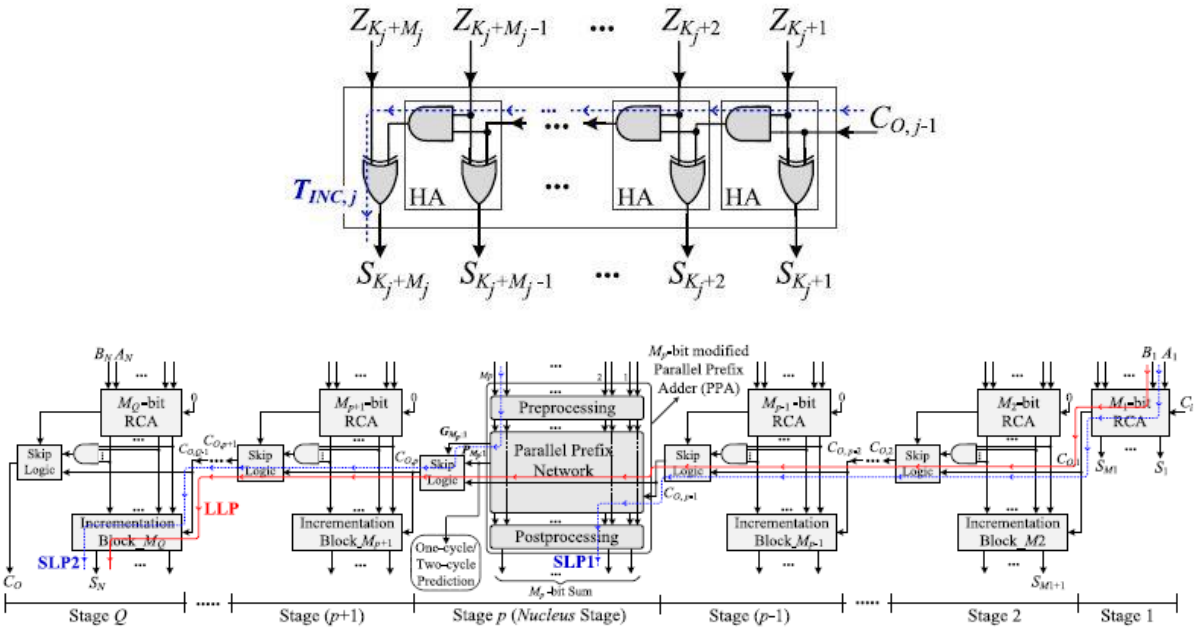
The RCA has the simplest construction with the smallest area and power spending but with the worst critical path delay.

In the CSLA, the speed, power consumption, and area usages are significantly larger than those of the RCA. The PPAs, which are also called carry look-ahead adders, use direct parallel prefix structures to generate the carry as fast as possible. There are different types of the parallel prefix algorithms that lead to special PPA structures with different performances. As an example, the Kogge–Stone adder (KSA) is one of the fastest structures but results in large power spending and area usage.

Proposed Carry Skip Adder

In this paper we suggest a novel variable latency speculative adder based on Han-Carlson parallel-prefix topology. The Han-Carlson topology uses one more stage than Brent-Kung adder, while require a reduced number of cells and simplified wiring. Thus it is can achieve similar speed performance compared to Brent-Kung adder, at lower power spending and area. Han-Carlson speculative adder has compact number of cells , simplified wiring match up to with speculative Brent-Kung adder. Speed of error detection network in Han-Carlson adders is faster than the Brent-Kung architecture. Han-Carlson speculative adder exhibits a lower error possibility than Brent-Kung adder.





Conventional Carry Skip Adder

The structure of an *N*-bit Conv-CSKA, which is based on blocks of the RCA (RCA blocks). In addition to the chain of FAs in each stage, there is carry skip logic. For RCA that contains *N* cascade FAs, the worst propagation delay of the summation of two *N*-bit

Numbers, *A* and *B*, belongs to the case where all the FAs are in the propagation mode. It means that the worst case delay belongs to the case where

$Pi = Ai \oplus Bi = 1$ for $i = 1. . . N$ where *Pi* is the spread signal related to *Ai* and *Bi*. This shows that the delay of the RCA is linearly related to *N* . In the case, where group of cascaded FAs are in the propagate mode, the carry output of the chain is equal to the carry input. In the CSKA, the carry skip logic detects this situation, and

Makes the carry ready for that next stage without waiting for the operation of the FA chain to be completed. The skip operation is performed using the gates , the multiplexer shown in the figure. Based on this details, the *N* FAs of the CSKA are grouped in *Q* stages. Each stage contains an RCA building block with *Mj*

FAs ($j = 1, . . . , Q$)

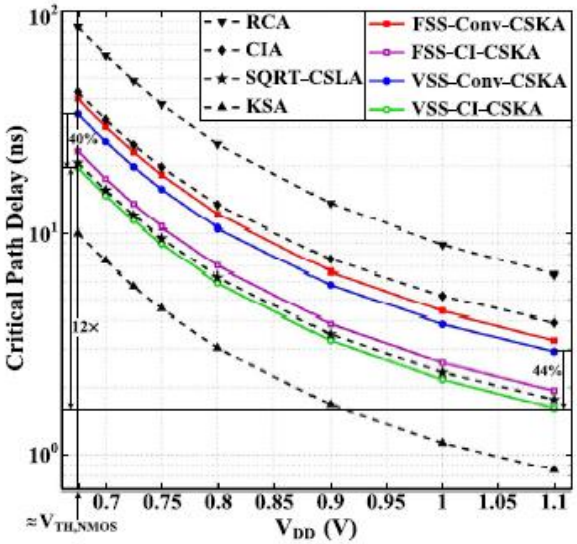
and a skip logic. In each stage, the

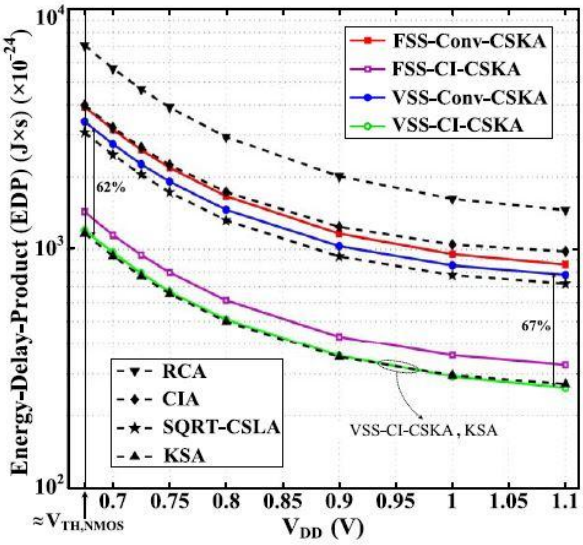
Inputs of the multiplexer (skip logic idea is implemented) are the carry input of the stage and the carry output of its RCA block (FA chain). In addition, the product of the propagation signals (*P*) of the stage is used as the selector signal value of the multiplexer. The CSKA may be implemented using FSS and VSS where the highest speed may be obtained for the VSS structure. Here, the stage size is the same as RCA block size. In this Sections III-A and III-B, these two different implementations are of the CSKA adder they are also described in more detail.

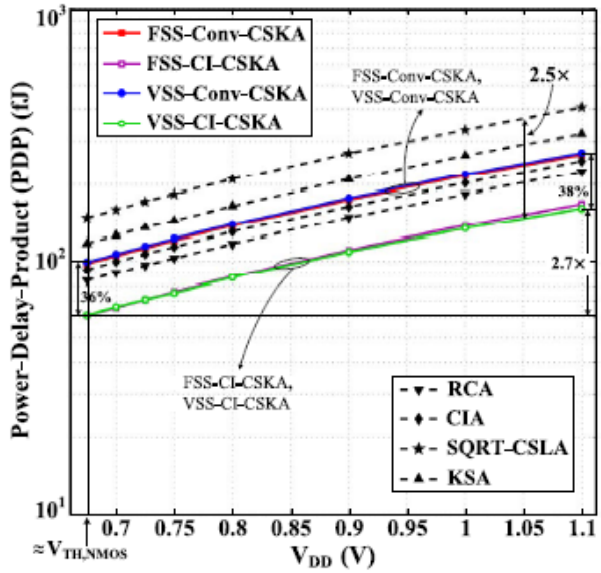
AREA USAGES AND NUMBER OF TRANSISTORS OF THE ADDERS

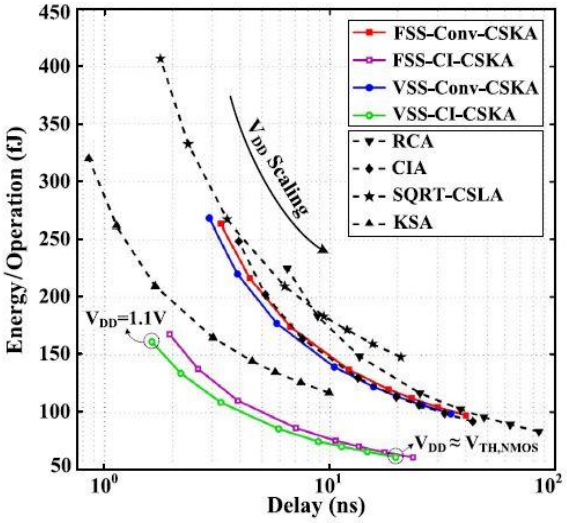
Adder Structure	Area (μm^2)	# of Transistors
RCA	151.3	896
CIA	230.0	1402
SQRT-CSLA	357.4	2096
KSA	403.2	2010
FSS-Conv-CSKA	254.2	1456
FSS-CI-CSKA	246.3	1370
VSS-Conv-CSKA	253.1	1464
VSS-CI-CSKA	241.5	1332

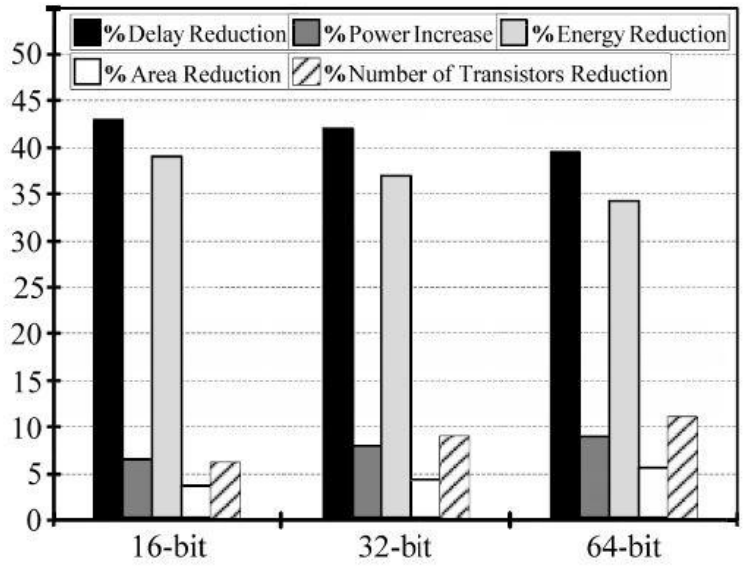
RESULTS


RCA
CIA
SQRT-CSLA
KSA
FSS-Conv-CSKA
FSS-CI-CSKA
VSS-Conv-CSKA
VSS-CI-CSKA
Critical Path Delay (ns)
40%
12×
44%
≈V_TH,NMOS
V_DD (V)


FSS-Conv-CSKA
FSS-CI-CSKA
VSS-Conv-CSKA
VSS-CI-CSKA
Energy-Delay-Product (EDP) (J×s) (×10^-24)
62%
67%
RCA
CIA
SQRT-CSLA
KSA
VSS-CI-CSKA, KSA
≈V_TH,NMOS
V_DD (V)


FSS-Conv-CSKA
FSS-CI-CSKA
VSS-Conv-CSKA
VSS-CI-CSKA
FSS-Conv-CSKA, VSS-Conv-CSKA
2.5×
38%
2.7×
36%
FSS-CI-CSKA, VSS-CI-CSKA
RCA
CIA
SQRT-CSLA
KSA
Power-Delay-Product (PDP) (fJ)
≈V_TH,NMOS
V_DD (V)


FSS-Conv-CSKA
FSS-CI-CSKA
VSS-Conv-CSKA
VSS-CI-CSKA
RCA
CIA
SQRT-CSLA
KSA
V_DD Scaling
V_DD=1.1V
V_DD ≈ V_TH,NMOS
Energy/Operation (fJ)
Delay (ns)



Applications

- Real-time signal processing.
- ALU system design.
- Video/image processing.

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