High K Oxides as an Alternative Gate Oxide in CMOS Technology and Its Corresponding Effects

[1]Alekhya Duba, [2]Vidhi Jaggi, [3]Mr. Abhishek Verma, [4] Dr. Anup Mishra

[1,2]B.E Scholar, [3]Assistant Professor, [4]Professor

Bhilai Institute of Technology, Durg (C.G.)

Abstract

Recent years have seen myriads of drastic transformations in the field of metal oxide semiconductors. Beginning from using oxy- nitride in 2001 as a gate oxide to SiO_2 in 2007, gate oxides has been a topic of constant research. However the present focus is to reduce the leakage current which is amplified due to constant scaling of the device. Reduction of the leakage current can be done by replacing SiO_2 with a physically thicker layer of metal oxides with a higher relative permittivity (K) such as HfO_2, Al_2O_3 and La_2O_3. These oxides are inferior to SiO_2 in properties such as they have a high defect density and their inability to remain in amorphous form. This review covers the choice of high-K oxides, requisites of a material to serve a better gate oxide than SiO_2, mobility and leakage current of the present materials under consideration.

Keywords – *High K oxides, CMOS scaling, Leakage current, Mobility.*

1. Introduction

In advancement of integrated circuit technology, scaling of gate dielectric thickness to reduce size of MOSFETs is a big challenge. MOSFET has been continually scaled down in size to increase drive current, for higher switching speed and to have more number of transistors on a single chip. The rate of scaling viz. doubling of the number of transistors integrated per unit area after every 18 months was an observation of Gordon E Moore. The minimum feature size in a transistor has decreased exponentially with year. The semiconductor Roadmap defines how each design parameter will scale in future years to continue this, as shown in Figure 1 and Table 1.

Aggressive scaling of CMOS technology in recent years has reduced the silicon dioxide (SiO_2) gate dielectric thickness to few nm. However the scaling cannot go forever, and there is a limit to Moore's law. Major cause for further reduction of the SiO_2 thickness is increased gate leakage current. The thickness of the SiO_2 layer presently used as the gate dielectric is becoming so thin that the gate leakage current due to direct tunnelling of electrons through the SiO_2 will be so high that the circuit power dissipation will increase to unacceptable values. Variation of leakage current with reduced thickness of SiO_2 is shown in figure 2.
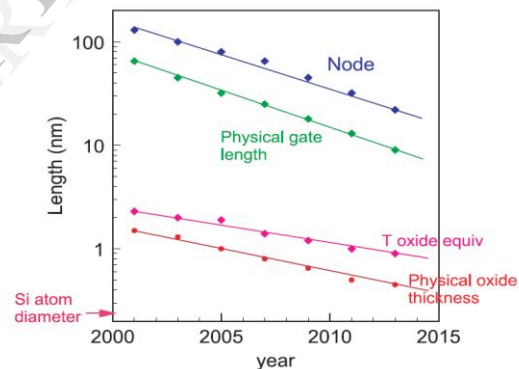

Fig 1 :Scaling of feature size, gate length and oxide thickness according to 2003 Semiconductor Roadmap[1]
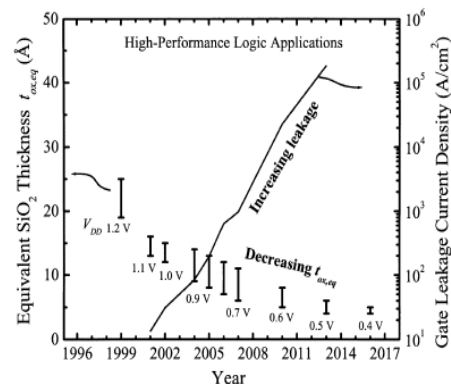

Fig 2: Scaling trend of MOSFET gate dielectric thickness [2].

Table 1. Summary of 2003 Roadmap. Node, gate length, equivalent oxide thickness of high power(CPU) and low standby power devices(mobile), gate oxide material [1].

Year	2001	2003	2005	2007	2009	2012	2016	2018
Node	130	100	80	65	45	32	22	18
ASIC 1/2 Pitch	150	107	80	65	45	32	25	18
Physical gate length	65	45	32	25	20	13	9	7
T_{ox} high power	1.5	1.3	1.1	0.9	0.8	0.6	0.5	0.5
T_{ox} low power		2.2	2.1	1.6	1.4	1.1	1.0	0.9
Gate oxide	oxynitride			HfO_x ; Si,N			$LaAlO_3$	
Gate metal	poly Si			metal gate, e.g. $TaSiN_x$				

Tunnelling currents decreases exponentially with increasing distance.FET is a capacitance-operated device, where the source-drain current of the FET depends on the gate capacitance, given by:

$$C = \varepsilon_0 \, KA/t \qquad (1)$$

Where, ε_0 is the permittivity of free space, K is the relative permittivity, A is the area and t is the SiO_2 thickness. Hence, the solution to the tunnelling problem is to replace SiO_2 with a physically thicker layer of a new material of higher dielectric constant K. This will keep the same capacitance, but will decrease the tunnelling current. These new gate oxides are called 'high K oxides'. The thickness of a high-K film ,in order to achieve the same capacitance as SiO_2 film of thickness t_{ox} can be written as [1]:

$$t_{eq} = T_{ox}(\varepsilon_{high\,K}/\varepsilon_{ox}) \qquad (2)$$

This implies that the thickness of a film with a dielectric constant higher than that of SiO_2 can be kept higher, thus achieving a reduction in gate leakage current. There are some problems identified for the use of high-K oxides. These are
 (1) the ability to continue scaling to lower EOTs,
(2) the loss of carrier mobility in the Si when using high K oxides,
(3) the shifts of the gate voltage threshold, and finally
(4) the instabilities caused by the high concentration of electronic defects in the oxides.

2. Effects of Scaling:

Aggressive scaling of CMOS technology in recent years has reduced the silicon dioxide (SiO_2) layer used as dielectric becoming too thin (<1.4nm).Major causes for concern in further reduction of the SiO_2 thickness include increased poly-silicon (poly-Si) gate depletion, gate dopant penetration into the channel region, and high direct-tunnelling gate-leakage current, exceeding $1A/cm^2$ at 1V.

This leakage arises from quantum effects. At 1.4 nm, the quantum nature of particles starts to play a dominant role. At such thickness, electron behaves more like a wave, defining the probability of finding the electron in a particular location. This wave extends all the way to the other side of the dielectric, increasing the probability of electron to appear on channel side having tunnelled through the energy barrier.

The leakage current can be given by the following equation [3]:

$$I_{gate} = W.\,L.\,A.\,(\frac{V_{ox}}{t_{ox}})^2 . \exp\left(\frac{-B\left(1 - \left(1 - \frac{V_{ox}}{t_{ox}}\right)^{\frac{3}{2}}\right)}{\frac{V_{ox}}{t_{ox}}} \right) \qquad (3)$$

Where W and L are the effective transistor width and length respectively,

$A = q^3/16\pi^2 h\varphi_{ox}$,

$B = 4\pi\sqrt{2m}(\varphi_{ox})^{3/2}/3hq$,

m_{ox} is the effective mass of the tunnelling particle,

φ_{ox} is the tunnelling barrier height,

t_{ox} is the oxide thickness,

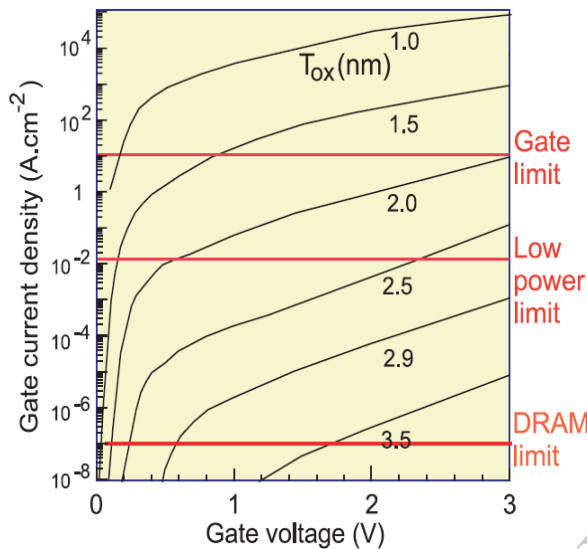h is $1/2\pi$ times Planck's constant and

q is the electron charge.

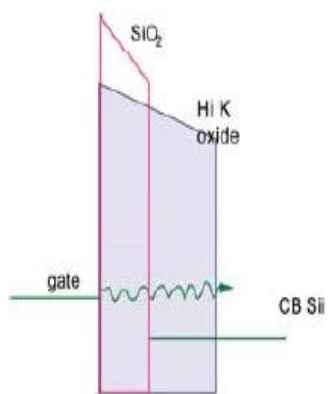**Fig 3: Leakage current vs. voltage for various thicknesses.[1]**

Fig 4: Schematic of direct tunnelling through a SiO$_2$ layer and the more difficult tunnelling through a thicker layer of high K oxide. [1]

This increased leakage current results in increased leakage power dissipation, which dominates the total chip power consumption as technology advances to nano scale. Most of the battery operated applications such as cell phones, Laptops etc requires a longer battery life, which can be made possible by controlling leakage current flowing through the CMOS gate.
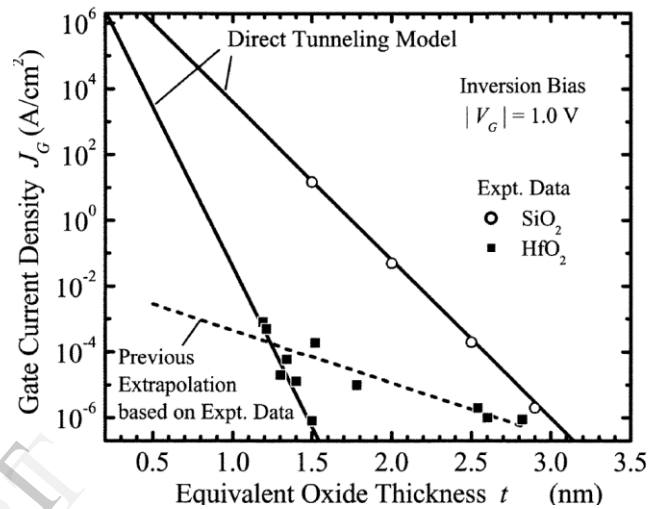

Fig 5: Variation in gate current density with thickness of oxide [2].

Presently a processor chip contains about 100 million transistors and each gives high leakage current which leads to heating effect. The advantage of scaling without increase in leakage current can be achieved by use of high K oxides as an alternative of SiO$_2$. The thickness of a high K film in order to achieve the same capacitance as an SiO$_2$ film of thickness t_{ox} can be written as

$$t_{eq} = t_{ox} (\varepsilon_{high-k}/\varepsilon_{ox}) \qquad (4)$$

From the above equation we can infer that by using high K oxide material instead of SiO$_2$ for insulation we can increase the thickness of the film, and can effectively reduce leakage current. Some of the high K elements investigated are silicon nitride (Si$_3$N$_4$) or oxynitride (SiO$_x$N$_y$) ,zirconium oxide (ZrO$_2$),hafnium oxide (HfO$_2$) ,aluminium oxide (Al$_2$O$_3$),and lanthanum oxide (La$_2$O$_3$).Variation of gate voltage and leakage current density with different oxides are as shown in figure 6.
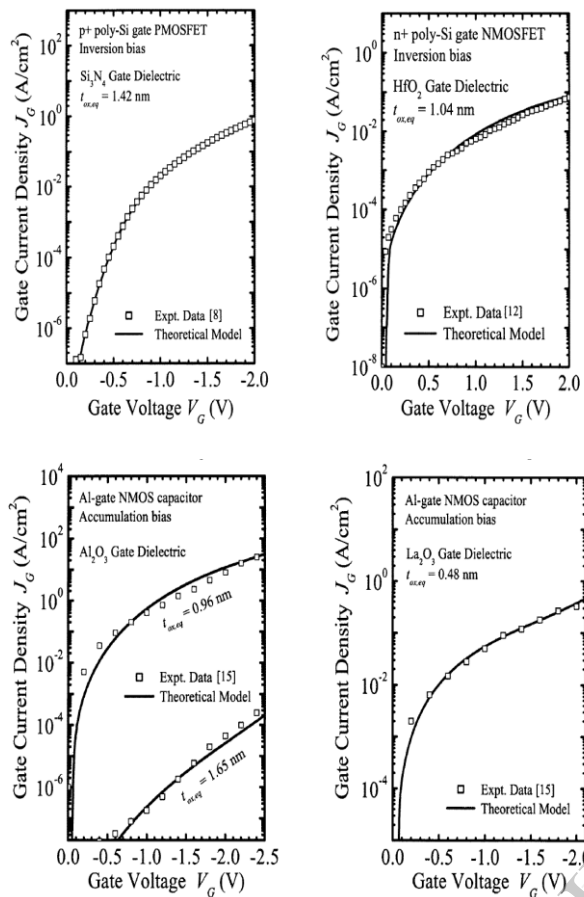
Fig 6: Variation of parameters with a) Si_3N_4 b) HfO_2 c) Al_2O_3 d) La_2O_3.[2]

By replacement of SiO_2 with high-K oxides, scaling can be done without sacrificing performance.

3. Choice of High K Oxides

Since it becomes necessary to replace the SiO2 with a physically thicker layer of oxides of higher dielectric constant (K), there are various oxides under consideration for this purpose such as hafnium oxide (HfO_2), hafnium silicate, zirconium oxide (ZrO_2),$SrO,CaO,Ta_2O_5,TiO_2,BaO,Al_2O_3,Y_2O_3,La_2O_3$, and various lanthanides and it was found that in many respects they have inferior electronic properties than SiO_2, such as a tendency to crystallize and a high concentration of electronic defects. New high quality electronic materials developed from these oxides are on the way of extensive research.

There are also some problems associated with high K such as increased threshold voltage and decreased mobility. These problems can be solved by replacing poly Si gates with doped metal gates which improves mobility.

The key reason for using Si in microelectronics technology is that SiO_2 is an excellent insulator. SiO_2 can be made from Si by thermal oxidation where as other semiconductor such as Ge, GaAs, GaN, SiC etc has a poor native oxide. The only problem of SiO_2 is that, when very thin, it is possible to tunnel across it. Hence we must start to use a new oxide of high K which we can choose from large part of periodic table.

The requirements of a new oxide to replace SiO_2 are as follows:

1) The metal oxide must have a permittivity higher than Si, industry targets values nearly between 15 to 20.
2) Aiming towards less leakage of current, the material should allow less leakage current.
3) Density of defects must be less
4) The oxide is in constant contact with Si and hence must be thermodynamically stable with it. [1]

5) High breakdown field and low loss factor .

3.1 K Value

The first requirement for the candidate oxide is that K should be over 10, preferably 25-30.From the table and figure it can be seen that the value of K vary inversely with the band gap. So we must accept a relatively low K value. There are oxides with very large K values such as $SrTiO_3$ but this has low band gap i.e 3.2eV. In fact we cannot use a huge K oxide in CMOS design because they cause undesirably strong fringing fields at source and drain electrode.

3.2 Thermodynamic Stability

The second requirement for oxide material is that it must not react with Si to form either SiO_2 or a silicide .This is because the EOT will increase due to resulting SiO_2 layer and the effect of using the new oxide will be negative. Also if silicide is formed then it would generally be metallic and would short out the field effect.

Table 2: Different oxides with their parameters.[4]

Dielectric	Dielectric Constant (Bulk)	Bandgap(eV)	Conduction offset(eV)
Silicon dioxide (SiO_2)	3.9	8.9	3.15
Silicon nitride (Si_3N_4)	7-7.8	5.3	2.1
Aluminium Oxide (Al_2O_3)	9-10	8.8	
Tantulum pentoxide (Ta_2O_5)	25	4.4	0.36
Lanthana (La_2O_3)	~27	5.8	2.3
Yttrium oxide (Y_2O_3)	~15	6	2.3
Hafnia (HfO_2)	~20	5.6-5.7	1.3-1.5
Zirconia (ZrO_2)	~23	4.7-5.7	0.8-1.4

This condition requires that the oxide used in place of SiO_2 should have high heat of formation than SiO_2.This restricts the possible oxides to very few, from columns II,III,AND IV of the periodic table. Some of these are SrO, CaO, BaO, Al_2O_3 ,ZrO_2, HfO_2,Y_2O_3 ,La_2O_3, and lanthanides. The group II oxides SrO etc are not favourable for use because they are reactive with water but they can be accepted as a transition layer. Hence we are now available with oxides like Al_2O_3,ZrO_2,HfO_2,Y_2O_3,La_2O_3, and various lanthanides. Zr and Hf belongs to group IV .It is also a fact that thermodynamic data for many oxides was not so

accurate .HfO_2 is presently preferred high K oxide over ZrO_2 because it was found that ZrO_2 is slightly unstable and react with Si to form silicide,$ZrSi_2$.HfO_2 in conjunction with metal gates improves leakage current, gate capacitance and speed. By replacing SiO_2 with HfO_2,transistors will be able to continue to shrink without sacrificing performance.

La_2O_3 has slightly higher K value than HfO_2 but it is more hygroscopic. Y_2O_3 also has lower K than La_2O_3. Al_2O_3 also has disadvantage of lower K value.

3.3 Kinetic Stability

The third condition to choose the oxide is that it should be compatible with existing process conditions. Suppose we choose an amorphous oxide, this requires that the oxide remain amorphous when annealed to upto 1000°C for 5 seconds. In this condition, SiO_2 is best as it is an excellent glass former but other high K oxides are not.Al_2O_3 is a reasonably good glass former and considered to be the next best in this respect.Ta_2O_5 is moderately good glass former but it cannot be used because it is reactive. Many other oxides crystallize well below 1000°C.

This problem can be avoided upto great extent by alloying the desired oxides with glass former SiO_2 or Al_2O_3 which gives either a silicate or aluminate. This then retains the stability against crystallisation to close to 1000°C.Under this condition, aluminates would be preferable to silicates as they have higher K value. Hf silicates can just pass this criterion as addition of some nitrogen is found to raise the crystallisation temperature.

The use of nano-crystalline oxides is found to be poor choice because the grain boundaries would cause higher current leakage paths.

3.4 Band Offset

The high K oxide must act as an insulator. This requires that the energy gap must be over 1eV so that the conduction by the Schottky emission of electrons or holes into the oxide bands can take place as shown schematically in figure. SiO_2 has gap of 9eV which forms large barriers for both electrons and holes. The

bands of narrower band gap oxides like SrTiO$_3$ which is only 3.3eV must be aligned almost symmetrically with respect to those of Si for both barriers to be 1eV.In practice, the valence band offset is usually larger than conduction band offset. Due to this the choice of oxide is limited to those with band gaps over 5eV.

Various oxides such as Al$_2$O$_3$,ZrO$_2$,HfO$_2$,Y$_2$O$_3$,La$_2$O$_3$ and various lanthanides and their silicates and aluminates satisfy this criterion. The reason for this is that high heat of formation correlates with a wide band gap in ionic compounds. Al$_2$O$_3$ is a highly desirable gate dielectric not only because it has high band gap, but also it has a high breakdown field(5-10 MV/cm).[5]The plot for leakage current versus EOT for various high K oxides is shown in fig 7.
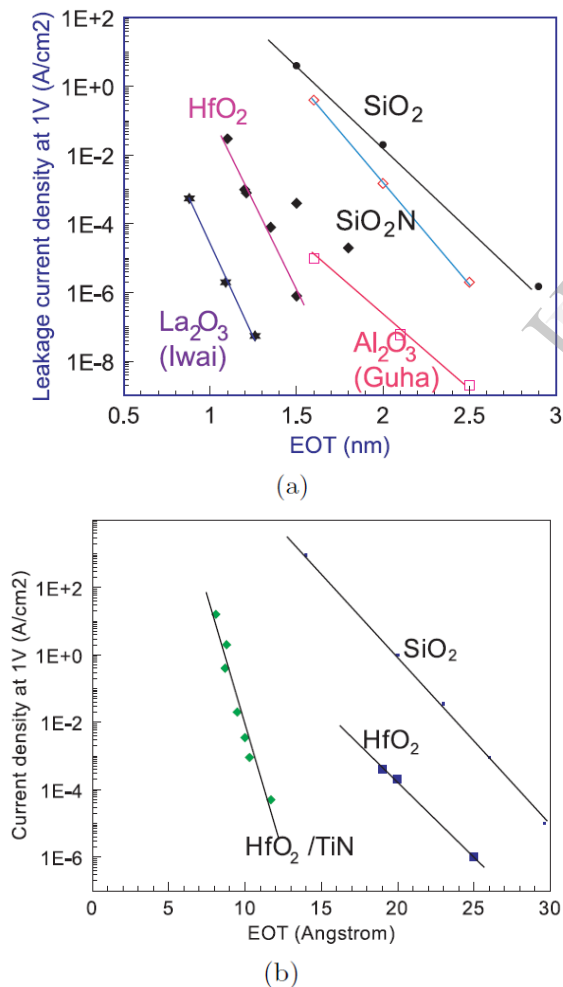

(a)

(b)

Fig 7: Leakage Current vs EOT.[1]

Lanthanides have the lowest leakage in figure and has the highest figure of merit because they have highest CB offset. However as La oxides are hygroscopic, Hf alloys are preferred.

4. Effects of High K oxides on Mobility:

The objective of using high K oxides in place of silicon dioxide is to create smaller, faster devices. The speed of the device follows source to drain current, which in turn depends on the carrier mobility. Carriers in FET behave like a two-dimensional electron gas. The carrier density is determined by the vertical gate field which induces them, by Poisson's equation.

The observations made by Takegi et al.[6] suggested that the mobility of electrons and holes depends only on the effective gate field and Si face,[100],[110] or [111].
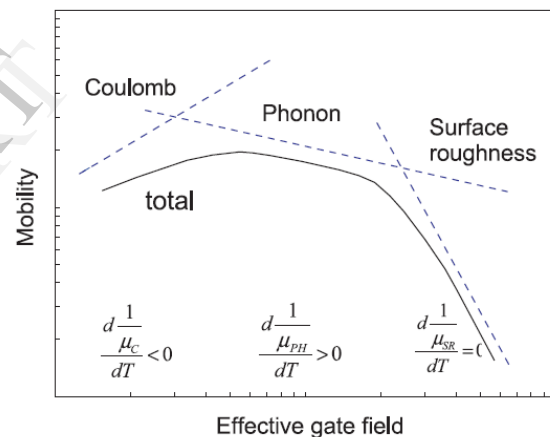

Fig.8. Carrier mobility vs. Vertical field in FETs in the universal mobility model, showing the mechanisms which limit the mobility, and their temperature dependences.[1]

The individual components of mobility add according to Matthiessen's rule,

$$\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}}$$

(5)

The mobility is limited by different mechanisms at different fields, as each obeys a different power law with field. At low fields, mobility is limited by Coulombic scattering(C) by trapped charges in the oxide, channels and gate electron interface; at moderate field it is limited by phonon scattering (PH), and at high fields by scattering by surface roughness (SR).

CMOS devices with SiO_2 gate oxide have a mobility close to 300 cm/V-s for the electric field and doping concentration used. The mobility is primarily limited by interface roughness over the range of interest. However the mobility offered by the high K oxides is well below this value. Figure 9 shows the mobility of various high K oxides. In NMOS devices this reduction is more pronounced as compared with that of PMOS, in which the reduction in mobility is fractionally less. This paper explores the cause of this lowered mobility and ways to overcome the same.

The cause of this mobility degradation can be described by the following two effects. First, high K oxides have much more trapped charge than SiO_2, these excessive amounts of trapped charges and interface states results in scattering[8]. Secondly, there is a possibility of remote scattering by low lying polar phonon modes as noted by Fischetti et al.[9]. The dielectric layer is made up of dipoles. These dipoles vibrate and lead to strong oscillations in the crystal lattice, called phonons. Oscillating dipoles interact with channel carriers when gate oscillations and phonons in high-K dielectric are in resonance. This resonance condition leads to significant degradation of channel carrier mobility and subsequently the operating speed of the device[5].
Resonance occurs when gate carrier density is $1 \times 10^{19}/cm^3$.

Fischetti [9] modelled the effect for various oxides and SiO_2. ZrO_2 and HfO_2 showed more pronounced reduction. The effect is smaller in $ZrSiO_4$ or $HfSiO_4$ which are covalently bonding without soft modes. It is also small in Al_2O_3 which has no soft modes. These oxides have intrinsic effect on mobility as compared to the higher K oxides such as HfO_2. However by using $HfSiO_4$, or by including SiO_2 as interfacial layer to separate the HfO_2 away from channel the mobility degradation can be minimised. Both the methods are undesirable as they increase EOT.
However this problem was soon overcome by substituting the polysilicon gate electrode with metal gate having free carrier density more than $1 \times 10^{20}/cm^3$, making it possible to dynamically screen the longitudinal soft optical phonon modes arising from

high K dielectric materials. The influence of dipole vibrations on the channel electrons can be reduced significantly by increasing the density of electrons in the gate electrode.
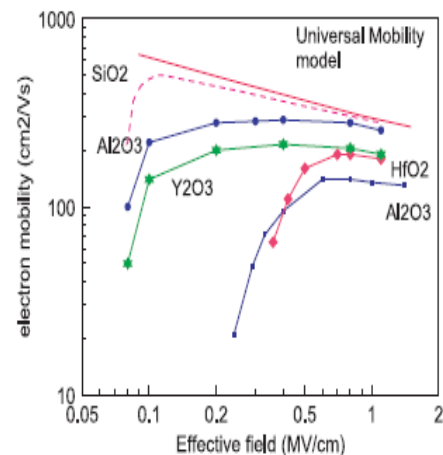

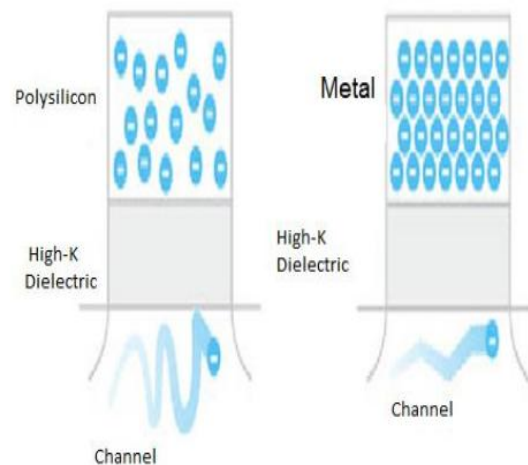**Fig.9. Carrier mobility of n-type Si, for various gate oxides, After Gusev et at.[7]**

Fig 10. Increase in channel mobility by replacing polysilicon gate with a metal gate[10].

The mobility of the channel carriers can be further increased considerably by using a combination of tin and HfO_2 as depicted in figure 11.
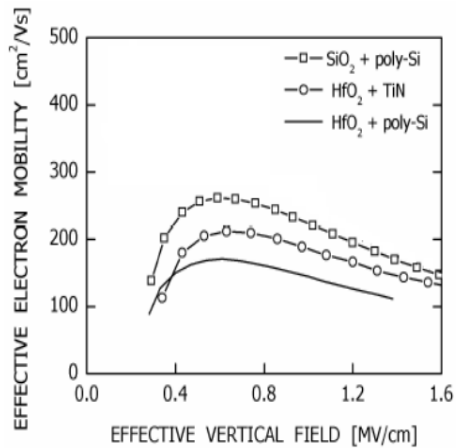
Fig .11 Effective electron mobility for a) HfO_2 with poly- Si b) HfO_2 with Tin c) SiO_2 with poly-Si.[11]

5. Conclusion

This paper has reviewed the choice of materials which could replace silicon dioxide. Leakage current as a result of scaling is explained and leakage current values for various thickness of SiO_2 is illustrated. The cause of mobility degradation due to defects and phonon scattering is also covered. Presently, Lanthana (La_2O_3) is used as an oxide in the mosfet channel. Though it has higher thermal stability and a high–K value, its moisture absorption capacity is large and hence is not stable with SiO_2. Further research can be carried in finding methods to reduce the problem of higher absorption of moisture.

6. References

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