High Efficiency Hybrid Switched Capacitor Sepic PFC Rectifier

Mrs. K Preetha
Assiatant Ptofessor
M. Pradeepa, R. Sasikala, G. Vasanthakumari
Final Year EEE
Dhanalakshmi Srinivasan Engineering College
Perambalur

***Abstract*:- A switched-capacitor concept is extended to the voltage-doublers discontinuous conduction correction rectifiers able to provide lower voltage stress on the semiconductor and higher staic gain, which can be easily increased with additional switched capacitor cells, is proposed. Hence, these rectifiers could be employed in applications that require higher output voltage. In addition, the converters provide a high power factor and reduced total harmonic distortion in the input current. This topology employs a three-state switch, and three different implementations are described, two being bridgeless versions, which can provide gains in relation to efficiency..**

INTRODUCTION

The market demand for power supplies with high dc output voltage for use in distributed generation, renewable energy, energy storage, dc–dc smart grids, electrical vehicles, UPS, X-ray systems, and motor drivers has increased. In these applications, the power supply can be used to directly feed a load or as an input stage of another power converter. In both cases, the system is commonly fed by an ac grid. Hence, a converter with power factor correction (PFC) is required to provide a high power factor (PF) and reduce the total harmonic distortion (THD) in accordance with the regulations and standards Due to the current-source characteristic at the input, structures derived from boost converters are normally employed in stages with PFC. Some boost rectifiers suitable for applications with high output voltage are proposed .

These topologies are referred to as voltage-doublers rectifiers and provide, when compared to the conventional boost rectifier, gain since relation to cost and efficiency and supply twice the output voltage (hence, the term “voltage doublers”) or a lower voltage stress on the semiconductors. Other examples of PFC rectifiers available for application with higher output voltage are the voltage-double SEPIC converters addressed and These converters operate in discontinuous conduction mode (DCM), because in this operation mode, the input current naturally has the same shape (if the high-frequency ripple of this current is neglected) and phase of the input voltage .Hence, the rectifier does not require a current-control loop, which simplifies its control system. Furthermore, in the case of these rectifiers, the input current does not have the third harmonic, do not need additional bulk filters and impose reduced voltage stress on the semiconductors. On the other hand, recent publications describe a new class of PFC rectifiers, referred to as hybrid (pulse-width-modulated + switched–capacitor (SC)) rectifiers. This class integrates conventional rectifiers with the switched-capacitor converters (SCC), which are able to divide or multiply a voltage without increasing the voltage stress across the semiconductors. Hence, this new class of PFC rectifiers can be employed in applications that require higher dc output voltage (above 400 V). Although the concept of hybrid rectifiers is recent.

It has already provided opportunities for new lines of research. In this context, based on the voltage-doublers SEPIC rectifier in, multiplier SEPIC dc–dc converter in, SC cell in hybrid rectifiers in and studies described in, this paper proposes set of single-phase hybrid voltage-doubler SEPIC rectifiers. These rectifiers provide a high power factor, reduced THD, reduced voltage stress on the semiconductors, and higher dc output voltage values (above 800 V). The boost converters integrated to SCcells approached in contrast to the proposed rectifiers in this paper, operate .Therefore, these structures require a control oopto regulate the input current, which makes the control system of the converter more complex. Furthermore, the boost rectifiers operate with variable duty cycle, which increases the losses in the SC.

The converters addressed in use the conventional ladder SC cell in dc–dc and ac–ac conversion and the same cells are applied in and.The conventional ladder SC cell does not work in the SEPIC rectifier. Hence, in, a modified ladder SC cell that allows the integration between SCC and classical SEPIC rectifier was proposed. Despite employing an additional semiconductor, this modified cell allows the rectifier to work properly and it preserves the high quality of the input current, which is an important characteristic of the SEPIC rectifiers that operate in DCM. However, only a partial analysis of the SC integrated to the classical SEPIC rectifier is approached.

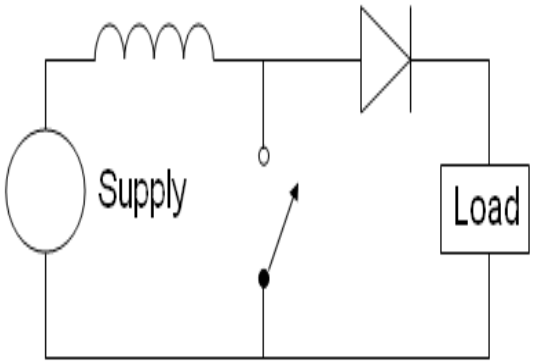
1.2. OBJECTIVE

The main objective of this project is to get high efficiency using hybrid switched capacitor SEPIC PFC rectifiers.

2.1. EXISTING SYSTEM

Conventional step-up converters, such as the boost converter and flyback converter, cannot achieve a high step-up conversion with high efficiency because of the resistances of elements or leakage inductance; also, the voltage stresses are large. A boost converter (step-up converter) is a DC-to-DC power converter with an output voltage greater than its input voltage. It is a class of switched-mode power supply (SMPS) containing at least two semiconductors (a diode and a transistor) and at least one energy storage element, a capacitor, inductor, or the two in combination. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple.

2.1.2. CIRCUIT DIAGRAM



DRAWBACK

- High step-up single-switch converters are unsuitable to operate at heavy load given a large input current ripple, which increases conduction losses.
- The step-up gain is limited, and the voltage stresses on semiconductor components are equal to output voltage.
- *PROPOSED SYSTEM*

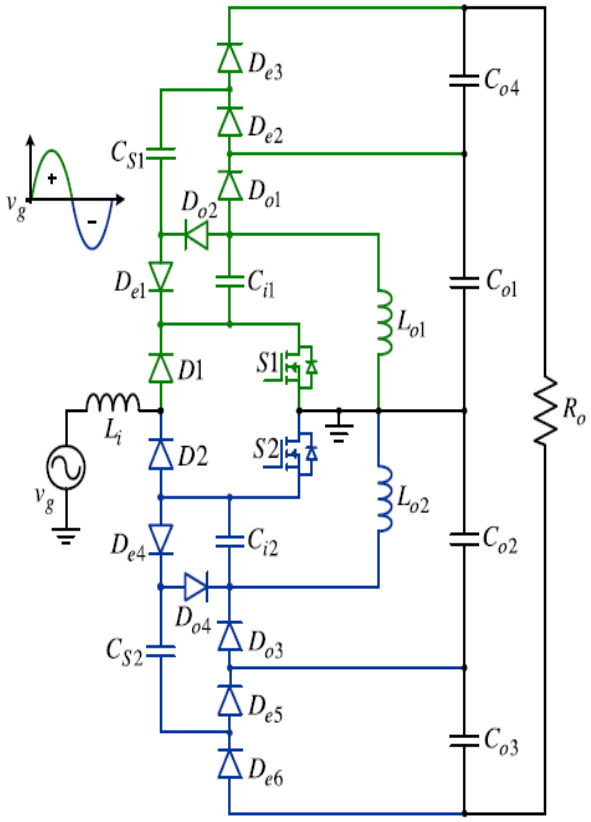
3.1. INTRODUCTION

The structure of the hybrid voltage-doubler SEPIC rectifier requires a three-state switching cell. These cells can be used in applications that require a static gain (*M*) less than, equal to, or greater than 1 (M _ 1, M _ 1). It is important to highlight that regardless of the cell employed; the main topological states of the circuit are not changed.

The proposed structure increases the static gain of the voltage doubler SEPIC rectifier by adding of ladder-type SC cells. The elements CS1 , CS2 , Co3 , Co4 , De1 , De2 , De3 , De4 , De5 , De6 , Do2 , and Do4 integrate the first- and second-modified SC cells. These two cells have two extra diodes (De1–Do2 and De4–Do4) (when compared to the conventional SC cell) which allow the charge and discharge of the SC CS1 and CS2, without changing the voltage in Ci1 and Ci2 (this modified cell was proposed for the conventional SEPIC rectifier). The resulting structure is able to provide a high-quality input current, and, thus, the SC can be applied in the SEPIC rectier.

charging purpose then it move to the voltage doubler to increase the voltage level and fed to the sepic rectifier it is a dc to dc converter then it moves to switches for conduction process and it move to rectifier and power factor control that can be connected to the rectifier output for control the output power

3.3. CIRCUIT DIAGRAM



3.3.1. MODES OF OPERATION

Stage 1(a): This stage starts when the switch S1 is turned ON. The diodes D1, De1, and De2 are forward biased, while all other diodes are reversed biased. The elements S1, De1, and De2 connect the capacitors Co1 and CS1 in parallel. However, the charge current of CS1 does not flow through Ci1 duetothemodifiedSCcell.TheSCCS1 ischargedbyCo1 from S1, D e1, and De2 and it presents voltage equal to vCo1 which, in turn, is equivalent to vo/(2+ n).The current in the inductors Li and Lo1 increases linearly in agreement with the vg/Li and vg/Lo1 ratios, respectively.

The load Ro is fed by the capacitors Co1, Co2, Co3, and Co4.

Stage 2 (b): This state is initiated when the switch S1 is turned OFF. Diodes D1, Do1, Do2, and De3 are forward biased and all other diodes are blocked. The elements Do2, Do1, and De3 connect CS1 and Co4 in parallel. Hence, the voltages on theses capacitors are equal to Vo/(2+ n). The current that flows through these elements is provided by inductors Li and Lo1. The current in the inductors Li and Lo1 decreases accordingly with relations [−Vo/(2+ n)]/Li and[−Vo/(2+ n)]/Lo1, respectively. The load Ro and output capacitosuppliedbyenergy previously stored in Li and Lo1 in the firststage.

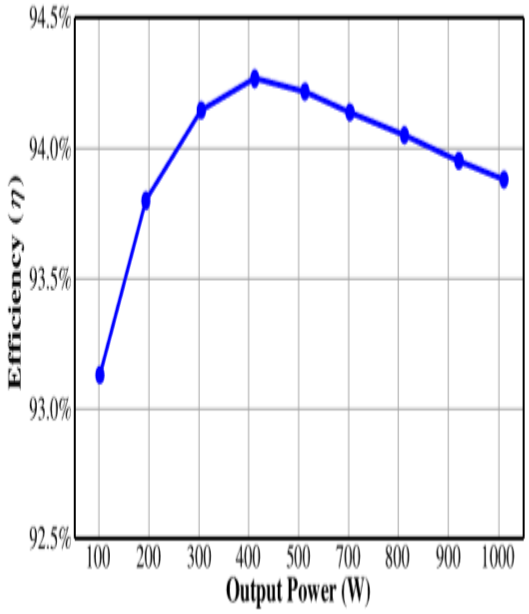
Stage 3 (c): During this stage, the switch S1 remains turned OFF and the diodes D1, Do2, and De3 are forward biased. Diode Do1 and all other semiconductors are blocked. The capacitors CS1 and Co4 remain connected in parallel through the diodes Do2, Do1, and De3. The energy stored in the inductors Li and Lo1 flows through Do2, CS1, and De3 to the load Ro and the output capacitors.

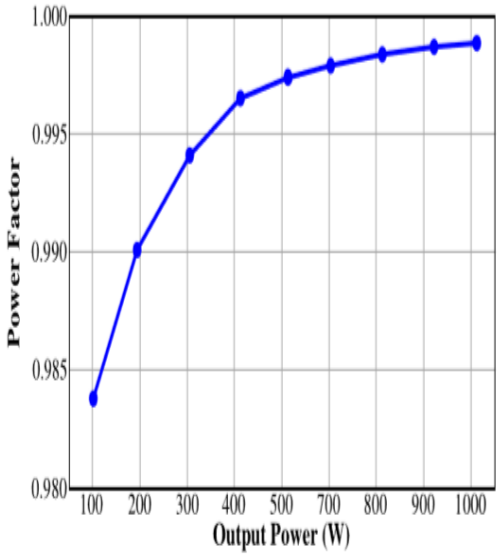
Stage 4: (This subinterval is the traditional discontinuous stage of the SEPIC converter. During this stage, all of the semiconductors are turned off and the current in the inductors andLo1 is constant.Hence, the voltage across these inductors is zero. The voltage on the capacitors CS1, CS2, Co1, Co2, Co3, and Co4 is equal to Vo/ (2+ n). The load Ro is fed by the output capacitors

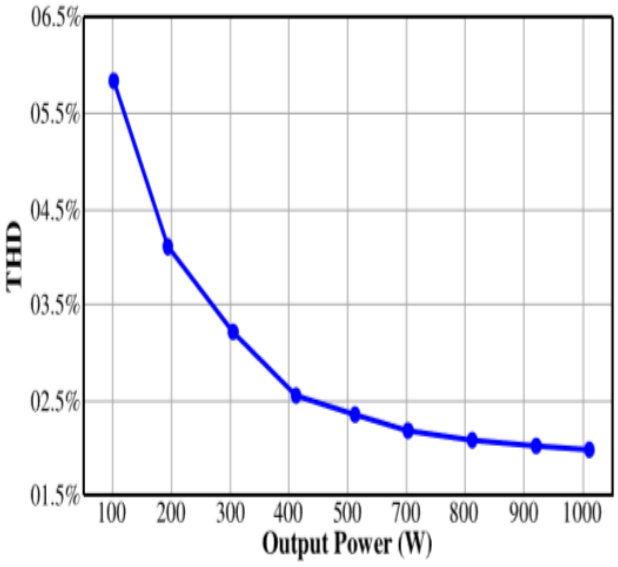
Advantages:

- These rectifiers improve the static gain of the voltage-doubler SEPIC converter without increasing the voltage stress on the semiconductors, making them suitable for applications that require high output voltage levels.
- The rectifiers operate with a fixed duty cycle, which reduces the losses from the SC cell.
- **Applications:**
- Distributed generation,
- Renewable energy,
- Energy storage, dc–dc smart grids,
- Electrical vehicles, ups, x-ray systems, and motor driver

4.5. SIMULATION AND OUTPUT







HARDWARE REQUIREMENT

5.1. HYBRID VOLTAGE-DOUBLER

SEPIC RECTIFIERS

The structure of the hybrid voltage-doubler SEPIC rectifier requires a three-state switching cell, which can be implemented in three modes: the first (1S) employs one active switch, as seen in the second (2S) and uses two active switches; and the third (4S) and employs four active switches. These cells can be used in applications that require a static gain (M) less than, equal to, or greater than 1 (M 1, M 1). It is important to highlight that regardless of the cell employed; the main topological states of the circuit are not changed. The proposed structure increases the static gain of the voltage doublers SEPIC rectifier by adding of ladder-type SC cells. The elements CS1, CS2, Co3, Co4, De1, De2, De3, De4, De5, De6, Do2, and Do4 integrate the first- and second-modified SC cells.

These two cells have two extra diodes (De1–Do2 and De4–Do4) (when compared to the conventional SC cell which allow the charge and discharge of the SC CS1 and CS2, without changing the voltage in Ci1 and Ci2 (this modified cell was proposed for the conventional SEPIC rectifier in The resulting structure is able to provide a high-quality input current, and, thus, the SC can be applied in the SEPIC rectifier. The other cells, seen in (CS n −De n−De n+1−Co n, and CS n+1−De n+2−De n+3−Co n+1), are conventional ladder SC cells and are added to increase the static gain of the Battery Energy Storage system

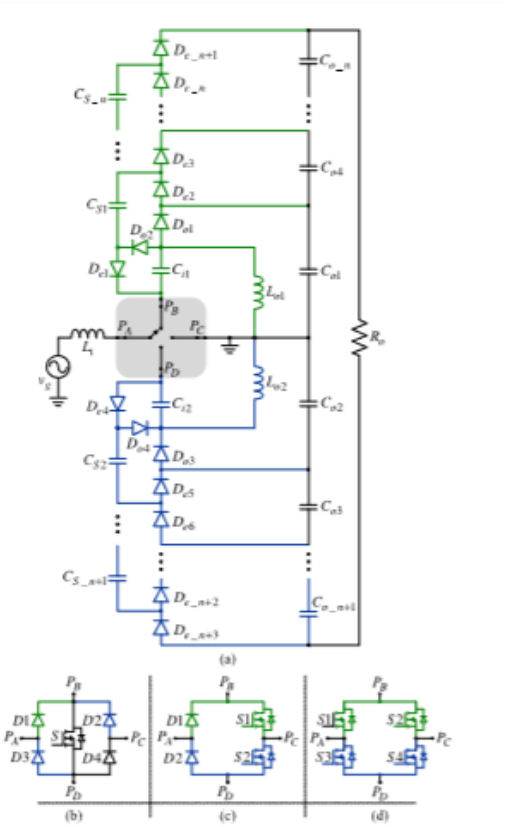


Figure 5.1: (a) single-phase hybrid voltage-doubler SEPIC rectifier with three-state generic active switching cell and generic SC cell, (b) three-state switch with one active switch (1S),

(c) three-state switch with two active switches (2S—bridgeless version), and

(d) three-state switch with four active switches (4S—bridgeless version).

SWITCHED CAPACITOR

A **switched capacitor** is an electronic circuit element implementing a filter. It works by moving charges into and out of capacitors when switches are opened and closed. Usually, non-overlapping signals are used to control the switches, so that not all switches are closed simultaneously. Filters implemented with these elements are termed "switched-capacitor filters", and depend only on the ratios between capacitances. This makes them much more suitable for use within integrated circuits, where accurately specified resistors and capacitors are not economical to construct.

A circuit methodology, typically implemented in CMOS integrated circuits, that uses clocked switches and capacitors to transfer charge from node to node such that a resistor function is realized. The effective resistance is governed by capacitor size and switching clock frequency.

Another basic concept is the charge pump, a version of which is shown schematically. The charge pump capacitor, C_P, is first charged to the input voltage. It is then switched to charging the output capacitor, C_O, in

series with the input voltage resulting in $C_O$eventually being charged to twice the input voltage. It may take several cycles before the charge pump succeeds in fully charging C_O but after steady state has been reached it is only necessary for C_P to pump a small amount of charge equivalent to that being supplied to the load from C_O. While C_O is disconnected from the charge pump it partially discharges into the load resulting in ripple on the output voltage. This ripple is smaller for higher clock frequencies since the discharge time is shorter, and is also easier to filter. Alternatively, the capacitors can be made smaller for a given ripple specification. The practical maximum clock frequency in integrated circuits is typically in the hundreds of kilohertz

CONCLUSION

This project proposed the integration of the single-phase voltage-doubler SEPIC rectifier with the SC concept. As a result, a set of hybrid rectifiers was generated. These rectifiers improve the static gain of the voltage-doubler SEPIC converter without increasing the voltage stress on the semiconductors, making them suitable for applications that require high output voltage levels (above 800 V). The structures, a theoretical analysis, and the experimental validation of this integration are the main contributions of the paper. The SC cell integrated to the voltage-doubler SEPIC rectifier has extra diodes, which contribute to obtain a high-quality input current. The static gain of the proposed converters can be easily increased through the insertion of additional SC cells, and in this paper, it is generalized for n cells. Additionally, the rectifiers operate with a fixed duty cycle, which reduces the losses from the SC cell.

FUTURE WORK:

The converter implemented was tested at rated power (1 kW) and it provided a current with a THD of 1.96%, PF of 0.999, and efficiency of 93.9%. These results are significant because the rectifier does not use the soft commutation technique and operates in DCM

REFERENCES

[1] A. D. B. Lange, T. B. Soeiro, M. S. Ortmann, and M. L. Heldwein, “Three-level single-phase bridgeless PFC rectifiers,” IEEE Trans. Power Electron., vol. 30, no. 6, pp. 2935–2949, Jun. 2015.

[2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, “A review of single-phase improved power quality ACDC converters,” IEEE Trans. Ind. Electron., vol. 50, no. 5, pp. 962–981, Oct. 2003.

[3] C.Jung,“Powerupwith800-Vsystems:Thebenefitsofupgradingvoltage powerforbattery-electricpassengervehicles,”IEEEElectrificationMag., vol. 5, no. 1, pp. 53–58, Mar. 2017.

[4] D. F. Cortez and I. Barbi, “A family of high-voltage gain single-phase hybrid switched-capacitor PFC rectifiers,” IEEE Trans. Power Electron., vol. 30, no. 8, pp. 4189–4198, Aug. 2015.

[5] D. D.-C. Lu and W. Wang, “Bridgeless power factor correction circuits with voltage-doubler configuration,” in Proc. IEEE 9th Int. Conf. Power Electron. Drive Syst., 2011, pp. 1037–1042.

[6] E. H. Ismail, “Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses,” IEEE Trans. Ind. Electron., vol. 56, no. 4, pp. 1147–1157, Mar./Apr. 2009. [7] M. T. Zhang, J. Yimin, F. C. Lee, and M. M. Jovanovic, “Single-phase three-level boost power factor correction converter,” in Proc. Appl. Power Electron. Conf., 1995, pp. 434–4s39.

[7] I. C. Kobougias and E. C. Tatakis, “Optimal design of a half-wave Cockcroft–Walton voltage multiplier with minimum total capacitance,” IEEE Trans. Power Electron., vol. 25, no. 9, pp. 2460–2468, Sep. 2010.

[8] J. C. Salmon, “Circuit topologies for single-phase voltage-doubler boost rectifiers,” IEEE Trans. Power Electron., vol. 8, no. 4, pp. 521–529, Oct. 1993.

[9] P.J.S.Costa, C.H.IllaFont, andT.B.Lazzarin,“Afamilyofsingle-phase voltage-doubler high-power-factor SEPIC rectifiers operating in DCM,” IEEE Trans. Power Electron., vol. 32, no. 6, pp. 4279–4290, Jun. 2017.